Introduction

This reference manual targets application developers.

It provides complete information on how to use the SPC2168 microcontroller memories and peripherals. For device mechanical and electrical characteristics please refer to the SPC2168 datasheet document.

SPINTROL

Contents

1 MEMORY AND BUS ARCHITECTURE 47

1.1 System architecture 47

1.2 Dual-core resource access 48

1.3 Clock tree 49

1.4 Memory map 50

1.4.1 Embedded Flash Memory 55

1.4.2 Embedded SRAM 55

1.5 Boot configuration 58

2 POWER 59

2.1 Single power domain 59

2.2 Analog power 59

2.3 Brown-out detectors 60

2.4 Deep-sleep mode 62

2.5 Registers 63

2.5.1 Power register map 63

2.5.2 Power registers 64

3 CLOCKS AND RESET 76

3.1 Reset architecture 76

3.2 Pin reset 76

3.3 POR reset 77

3.4 Clock architecture 77

3.5 High frequency RC oscillator 78

3.6 On-chip crystal oscillator and external clock 78

3.7 PLL clock 80

3.7.1 Reference input and divider 81

3.7.2 Output divider 81

3.7.3 Feedback divider 81

3.7.4 PLL unlock detection 81

3.8 Regulator for PLL and RC Oscillator 82

3.9 Clock multiplexers and dividers 82

3.9.1 Clock smooth Mux 82

3.9.2 HCLK 82

3.9.3 APB clock 83

3.9.4 GPIO deglitch clock 83

SPINTROL

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3.9.5 Communication peripheral clock 84
3.9.6 Watchdog timer clock 84
3.9.7 General-purpose timer clock 85
3.9.8 ADC clock 85
3.9.9 PWM clock 85
3.9.10 ECAP clock 86
3.9.11 SIO clock 86
3.10 Clock safety 86
3.11 Registers 88
3.11.1 Clock register map 88
3.11.2 Clock registers 89

4 GENERAL-PURPOSE I/O (GPIO) 114
4.1 Overview 114
4.2 Pin multiplexing (PINMUX) 115
4.2.1 Schmitt control 116
4.2.2 Deglitch control 116
4.2.3 I/O alternate functions 117
4.3 GPIO function IP (GPIO) 119
4.3.1 GPIO edge-triggered interrupt 119
4.3.2 GPIO level-triggered interrupt 120
4.4 Registers 122
4.4.1 PINMUX register map 122
4.4.2 PINMUX registers 124
4.4.3 GPIO register map 126
4.4.4 GPIO registers 128

5 INTERRUPTS AND EVENTS 149
5.1 Nested vectored interrupt controller (NVIC) 149
5.1.1 Features 149
5.1.2 Interrupt and exception vectors 149
5.1.3 NVIC interrupt configuration 151
5.2 SysTick Timer 152

6 AES 153
6.1 AES overview 153
6.2 Functional description 153
6.2.1 AES operation flow 153
6.2.2 AES configuration 154

SPINTROL

6.2.3 Data access method 155
6.2.4 Starting the AES engine 156
6.2.5 Interrupt request 156
6.2.6 Partial code support 156
6.2.7 Error status check 156
6.2.8 Output vector 157
6.3 Registers 158
6.3.1 AES register map 158
6.3.2 AES registers 159

7 CRC 176
7.1 CRC overview 176
7.2 Main features 176
7.3 CRC operation flow 177
7.4 Registers 178
7.4.1 CRC register map 178
7.4.2 CRC registers 179

8 GENERAL-PURPOSE TIMERS 184
8.1 Timer overview 184
8.2 Functional description 184
8.3 Initialization sequence 185
8.4 Registers 186
8.4.1 TIMER register map 186
8.4.2 TIMER registers 187

9 WATCHDOG TIMERS 192
9.1 Watchdog overview 192
9.2 Functional description 192
9.3 Initialization sequence 193
9.4 Registers 194
9.4.1 WDT register map 194
9.4.2 WDT registers 195

10 PWM 200
10.1 PWM overview 200
10.2 Time-Base (TB) sub-module 203
10.3 Counter Compare (CC) sub-module 206
10.4 Action-Qualifier (AQ) sub-module 208
10.5 Dead-Band (DB) sub-module 211

SPINTROL

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10.6 Trip-Zone (TZ) sub-module 214
10.7 Digital Compare (DC) sub-module 217
10.8 Event-Trigger (ET) sub-module 220
10.9 Global reload 220
10.10 Simultaneous write 221
10.11 Registers 222
10.11.1 PWM register map 222
10.11.2 PWM registers 224
10.11.3 PWMCFG register map 316
10.11.4 PWMCFG registers 317
11 ECAP 333
11.1 Introduction 333
11.2 Description 334
11.3 Capture and APWM operating mode 335
11.4 Capture mode description 336
11.4.1 Event prescaler 337
11.4.2 Edge polarity select and qualifier 338
11.4.3 Continuous/one-shot control 338
11.4.4 32-bit counter and phase control 339
11.4.5 CAP0-CAP3 registers 339
11.4.6 Interrupt control 340
11.4.7 Shadow load and lockout control 342
11.5 APWM mode operation 342
11.6 Application of the ECAP module 343
11.7 Registers 352
11.7.1 ECAP register map 352
11.7.2 ECAP registers 353
12 ADC 368
12.1 ADC overview 368
12.2 ADC architecture 369
12.3 SOC principle of operation 370
12.3.1 Trigger operation 374
12.3.2 ADC sampling mode and channel selection 375
12.3.3 Averaging control 378
12.3.4 ADC sample and convert window 379
12.4 ADC conversion priority 381
12.5 Simultaneous sampling mode 384

SPINTROL

12.6 EOC and interrupt operation 387
12.7 ADC post-processing units 388
12.7.1 PPU reference error calculation 389
12.7.2 PPU zero-crossing and threshold detection 390
12.7.3 Sample delay capture 391
12.8 ADC timing 392
12.9 Power-up sequence 393
12.10 ADC calibration 393
12.10.1 Factory settings and hardware calibration 393
12.10.2 Channel calibration 393
12.11 ADC result 394
12.11.1 Quantization range 394
12.11.2 ADC result calculation formula 394
12.12 ADC safety feature 395
12.12.1 Analog disconnection detection 395
12.12.2 Input short detection 397
12.13 Registers 398
12.13.1 ADC register map 398
12.13.2 ADC registers 403

13 PGA 555

13.1 PGA overview 555
13.2 PGA architecture 555
13.3 PGA channel selection 557
13.4 PGA mode and gain 558
13.5 PGA single-ended application in current sensing 561
13.6 PGA differential application in current sensing 562
13.7 PGA offset calibration 563
13.8 Resistive level shifter offset calibration 565
13.9 Power-up sequence 566
13.10 Registers 567
13.10.1 PGA register map 567
13.10.2 PGA registers 568

14 COMPARATOR 581

14.1 Comparator overview 581
14.2 Comparator architecture 581
14.3 Comparator MUX selection 582
14.4 Digital filter 583

SPINTROL

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14.5 Power-up sequence 584
14.6 Registers 585
14.6.1 Comparator register map 585
14.6.2 Comparator registers 587

15 BUFFERED 10-BIT DAC 664
15.1 Buffered DAC overview 664
15.2 Buffered DAC architecture 664
15.3 Ramp generator 666
15.4 Power-up sequence 667
15.5 Registers 668

16 TEMPERATURE SENSOR 669
16.1 T-sensor overview 669
16.2 Transfer function 669
16.3 Power-up sequence 670
16.4 Precision improvement 670
16.5 Registers 670

17 UART 671
17.1 UART overview 671
17.2 UART features 671
17.3 UART signal descriptions 672
17.4 UART operation 673
17.4.1 Reset 674
17.4.2 FIFO operation 674
17.4.3 Auto-baud-rate detection 676
17.4.4 Programmable baud-rate generator 676
17.4.5 Serial infrared asynchronous interface 677
17.5 Registers 679
17.5.1 UART register map 679
17.5.2 UART registers 680

18 I2C 696
18.1 I2C overview 696
18.2 I2C features 696
18.3 I2C signal description 696
18.4 I2C operation 696
18.4.1 START and STOP generation 697
18.4.2 Combined formats 697

SPINTROL

18.5 I2C protocols 698
18.5.1 START and STOP conditions 698
18.5.2 Address formats 698
18.5.3 Transmitting and receiving protocol 699
18.6 Registers 701
18.6.1 I2C register map 701
18.6.2 I2C registers 703

19 SSP 738

19.1 SSP overview 738
19.2 SSP features 739
19.3 SSP signal description 739
19.4 SSP function description 739
19.4.1 Introduction to operation 739
19.4.2 Baud rate generation 740
19.4.3 FIFO operation 740
19.4.4 Frame formats 742
19.4.5 SSP interrupts 744
19.5 Registers 746
19.5.1 SSP register map 746
19.5.2 SSP registers 747

20 FLASH MEMORY 756

20.1 Features 756
20.2 Flash module organization 757
20.3 Read operation 759
20.3.1 Read through XIP module 759
20.3.2 Read through Flash Controller 760
20.4 Program and erase operation 760
20.4.1 Enable Flash controller 761
20.4.2 Flash memory programming 761
20.4.3 Flash memory erase 763
20.5 Protections 765
20.5.1 Multi-zone protection 765
20.5.2 Write protection 765
20.6 Setup Flash timing 765
20.7 Configuration Words description 766
20.8 Registers 769
20.8.1 Flash register map 769

SPINTROL

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20.8.2 Flash registers 770

21 SIO 790

21.1 Overview 790

21.2 SIO Initialization 791

21.3 Registers 791

22 SYSTEM CONTROL 792

22.1 Overview 792

22.2 Unique device ID register (64 bits) 792

22.3 Memory error interrupt control registers 792

22.4 Memory ECC enable register 792

22.5 Memory lock status register 792

22.6 Reset event control registers 792

22.7 System information register 792

22.8 CAU control register 793

22.9 Registers 794

22.9.1 System register map 794

22.9.2 System registers 795

23 DIRECT MEMORY ACCESS CONTROLLER (DMA) 818

23.1 DMA Introduction 818

23.2 DMA features 818

23.3 DMA operation 820

23.3.1 Basic definitions 820

23.3.2 Hardware Handshaking interface 820

23.3.3 Memory-to-memory transfer operation 821

23.3.4 Memory-to-peripheral and Peripheral-to-memory transfer operation 823

23.3.5 Peripheral-to-peripheral transfer operation 825

23.6 Registers 830

23.6.1 DMACH register map 830

23.6.2 DMACH registers 831

23.6.3 DMAC register map 838

23.6.4 DMAC registers 839

24 MAILBOX 853

24.1 Mailbox overview 853

24.2 Mailbox architecture 853

24.2.1 Message RAMs 853

24.2.2 Software Interrupts 853

SPINTROL

24.3 Mailbox operation flow 855
24.4 Registers 856
24.4.1 Mailbox register map 856
24.4.2 Mailbox registers 857

25 DEBUG BEHAVIOR 859

25.1 Watchdog timers 859
25.2 General-purpose timers 859
25.3 PWM 859
25.4 ECAP 859
25.5 UART 860
25.6 SSP 860
25.7 I2C 860

SPINTROL

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List of Figures

Figure 1-1: Block diagram of SPC2168 47
Figure 1-2: Block diagram between the Main CPU and CAU 48
Figure 1-3: SPC2168 clock tree 49
Figure 1-4: SPC2168 memory map with Cache disabled and CAU stopped (Used as single core) 50
Figure 1-5: SPC2168 memory map with Cache enabled and CAU stopped (Used as single-core) 51
Figure 1-6: SPC2168 memory map with Cache disabled and CAU running (Dual core) 52
Figure 1-7: SPC2168 memory map with Cache enabled and CAU running (Dual core) 53
Figure 1-8: XIP Cache Disabled, SRAM Address Allocation with CAU Disabled 55
Figure 1-9: XIP Cache Disabled, SRAM Address Allocation with CAU Enabled 56
Figure 1-10: XIP Cache Enabled, SRAM Address Allocation with CAU Disabled 56
Figure 1-11: SPC2168 SRAM Allocation Options 57
Figure 2-1: Power supply overview 59
Figure 2-2: 3.3V domain brown-out detector diagram 60
Figure 2-3: 1.2V domain brown-out detector diagram 60
Figure 2-4: DVDD thresholds 61
Figure 2-5: VCAP12 thresholds 62
Figure 3-1: Active-low POR reset signal diagram 76
Figure 3-2: Active-low POR reset signal timing diagram 77
Figure 3-3: Clock overview 78
Figure 3-4: On-chip crystal oscillator 79
Figure 3-5: External clock 80
Figure 3-6: PLL clock overview 80
Figure 3-7: PLL unlock detection timing diagram example (FREF > FDIV) 82
Figure 3-8: HCLK control diagram 83
Figure 3-9: PCLK control diagram 83
Figure 3-10: GPIO deglitch clock diagram 83
Figure 3-11: Communication peripheral clock diagram 84
Figure 3-12: Watchdog timer clock diagram 84
Figure 3-13: General-purpose timer clock diagram 85
Figure 3-14: ADC clock diagram 85
Figure 3-15: PWM clock diagram 85
Figure 3-16: ECAP clock diagram 86
Figure 3-17: SIO clock diagram 86
Figure 3-18: Clock cross-detection 87
Figure 4-1: Structure diagram of I/O control 114
Figure 4-2: PINMUX structure diagram 115
Figure 4-3: Schmitt input mode 116
Figure 4-4: Input deglitching 116
Figure 4-5: GPIO structure diagram 119
Figure 4-6: GPIO edge-triggered interrupt 120
Figure 4-7: GPIO level-triggered interrupt 121
Figure 6-1: AES operation flow diagram 154
Figure 7-1: CRC block diagram 176
Figure 8-1: General-purpose timer structure 184

SPINTROL

Figure 8-2: GPT run flow diagram 185
Figure 9-1: Watchdog operation flow 192
Figure 10-1: PWM overview 200
Figure 10-2: PWM architecture 201
Figure 10-3: Time-Base sub-module signals 203
Figure 10-4: Time-base counter waveform 204
Figure 10-5: Time-base phase synchronization waveform 205
Figure 10-6: Counter-Compare sub-module structure 206
Figure 10-7: Counter-Compare sub-module waveform 207
Figure 10-8: Action-Qualifier sub-module inputs and outputs 208
Figure 10-9: Up-Down-Count, dual edge symmetric waveform of Action-Qualifier 210
Figure 10-10: Up-Down-Count, dual edge asymmetric waveform of Action-Qualifier 210
Figure 10-11: Dead-Band sub-module structure 211
Figure 10-12: Typical Dead-Band waveform 212
Figure 10-13: Dual-edge delay Dead-Band waveform 213
Figure 10-14: Trip-Zone sub-module logic 214
Figure 10-15: Trip-Zone interrupt generation 216
Figure 10-16: Digital Compare sub-module structure 217
Figure 10-17: Event filtering logic 218
Figure 10-18: Blank window timing diagram 218
Figure 10-19: Event processing 219
Figure 10-20: Event-Trigger sub-module structure 220
Figure 10-21: Global reload structure 221
Figure 11-1: Basic operation of enhanced capture 334
Figure 11-2: Capture and APWM modes of operation 335
Figure 11-3: Capture function diagram 336
Figure 11-4: Event prescale control 337
Figure 11-5: Prescale function waveforms 337
Figure 11-6: Details of the continuous/one-shot block 338
Figure 11-7: Details of the counter and synchronization block 339
Figure 11-8: Interrupts in ECAP module 341
Figure 11-9: Active and shadow register when APWM mode 342
Figure 11-10: PWM waveform details Of APWM mode operation (active High) 343
Figure 11-11: Capture sequence for absolute time-stamp and rising edge detect 344
Figure 11-12: Capture sequence for period and duty without counter reset 346
Figure 11-13: Capture period with counter reset 348
Figure 11-14: Capture duty and period with counter reset 350
Figure 12-1: ADC block diagram 369
Figure 12-2: SOC block diagram 370
Figure 12-3: ADC channel selection for Example 12.3.1 371
Figure 12-4: ADC2, ADC4 and ADC6 simultaneous sampling 378
Figure 12-5: Averaging control for ADC result 379
Figure 12-6: ADCx input pin model 380
Figure 12-7: Round ring priority example 382
Figure 12-8: High priority example 383
Figure 12-9: SOC0 simultaneous sampling signal flow and configuration 385
Figure 12-10: Interrupt structure 387

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Figure 12-11: Post-processing unit topology 388
Figure 12-12: Timing example for sequential mode interrupt 392
Figure 12-13: Timing example for simultaneous mode interrupt 392
Figure 12-14: ADC core description 394
Figure 12-15: ADC transfer curve 394
Figure 12-16: Detect the disconnection of ADC input pin (Discharge) 395
Figure 12-17: Detect the disconnection of ADC input pin (Precharge) 396
Figure 13-1: Block architecture for PGA0 ~ PGA2 555
Figure 13-2: Block architecture for PGA3 ~ PGA5 556
Figure 13-3: PGA input and output 558
Figure 13-4: Single-ended sensing of driver FET currents 561
Figure 13-5: PGA0 sample ADC4 in single-ended mode 562
Figure 13-6: Motor sensing arrangement (differential gain = 8) 562
Figure 13-7: Three-pin differential sensing of three currents (diffential gain = 8) 563
Figure 13-8: PGA offset 563
Figure 13-9: Offset behavior with input common-mode voltage 564
Figure 13-10: Level-shifting with resistor mismatch 565
Figure 14-1: Comparator 0 block diagram 581
Figure 14-2: Digital filter behavior 583
Figure 15-1: Buffered DAC block diagram 665
Figure 15-2: Ramp generator diagram 667
Figure 15-3: Ramp generator waveform 667
Figure 16-1: Temperature sensor transfer function 669
Figure 17-1: UART block diagram 672
Figure 17-2: Example UART data frame 673
Figure 17-3: Example NRZ bit Encoding – 0b0100_1011 673
Figure 17-4: IR transmit and receive example 678
Figure 17-5: Pulse of a zero bit 678
Figure 18-1: Data transfer on the I2C bus 697
Figure 18-2: START and STOP condition 698
Figure 18-3: 7-bit address format 698
Figure 18-4: 10-bit address format 699
Figure 18-5: Master-transmitter protocol 699
Figure 18-6: Master-receiver protocol 700
Figure 19-1: SSP block diagram 738
Figure 19-2: SSP master-slave connection 740
Figure 19-3: FIFO packed and non-packed mode 741
Figure 19-4: SSP clock format 0 (PHS = 0) 743
Figure 19-5: SSP clock format 1 (PHS = 1) 743
Figure 19-6: Motorola SPI frame protocol (multiple transfers) 744
Figure 20-1: Flash memory access interfaces 756
Figure 20-2: Logical structure of the Flash module 758
Figure 20-3: Flash memory reading procedure 760
Figure 20-4: Flash memory programming procedure 762
Figure 20-5: Flash memory Sector Erase procedure 763
Figure 20-6: Flash memory Chip Erase procedure 764
Figure 21-1: SIO architecture diagram 790

SPINTROL

Figure 21-2: SIO initialization flow 791
Figure 23-1: DMA block diagram 819
Figure 23-2: Breakdown of DMA transfer for memory 821
Figure 23-3: DMA transfer between two DRAM regions 822
Figure 23-4: Breakdown of DMA transfer for non-memory peripherals 823
Figure 23-5: DMA transfer between DRAM and UART/SSP 824
Figure 23-6: DMA interrupt generation 827
Figure 23-7: Pseduo-code for DMA ISR 827
Figure 23-8: Scenario DMA interrupt events for multiple channels 828
Figure 24-1: Mailbox architecture 854
Figure 24-2: Mailbox operation flow – Main CPU send data to CAU 855

SPINTROL

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List of Tables

Table 1-1: Peripheral Module Base Address 54
Table 1-2: Boot modes 58
Table 2-1: POWER Module Base Address 63
Table 2-2: POWER Register Map 63
Table 2-3: Power Status Register (PWRSTS) Layout 64
Table 2-4: Power Status Register (PWRSTS) Field Description 64
Table 2-5: LDO Control Register (LDOCTL) Layout 65
Table 2-6: LDO Control Register (LDOCTL) Field Description 65
Table 2-7: Low Power POR Control Register (PORCTL) Layout 66
Table 2-8: Low Power POR Control Register (PORCTL) Field Description 66
Table 2-9: BOD Interrupt Flag Register (BODIF) Layout 67
Table 2-10: BOD Interrupt Flag Register (BODIF) Field Description 67
Table 2-11: BOD Interrupt Clear Register (BODIC) Layout 68
Table 2-12: BOD Interrupt Clear Register (BODIC) Field Description 68
Table 2-13: BOD Interrupt Enable Register (BODIE) Layout 69
Table 2-14: BOD Interrupt Enable Register (BODIE) Field Description 69
Table 2-15: BOD Control Register (BODCTL) Layout 70
Table 2-16: BOD Control Register (BODCTL) Field Description 70
Table 2-17: 3.3V BOD Control Register (BOD33CTL) Layout 71
Table 2-18: 3.3V BOD Control Register (BOD33CTL) Field Description 71
Table 2-19: 1.2V BOD Control Register (BOD12CTL) Layout 73
Table 2-20: 1.2V BOD Control Register (BOD12CTL) Field Description 73
Table 2-21: Deep Sleep Enable Key Register (DPSLPKEY) Layout 75
Table 2-22: Deep Sleep Enable Key Register (DPSLPKEY) Field Description 75
Table 2-23: Power Register Write-Allow KEY Register (PWRREGKEY) Layout 75
Table 2-24: Power Register Write-Allow KEY Register (PWRREGKEY) Field Description 75
Table 3-1: Pin reset glitch filter window size options 77
Table 3-2: Input dividing ratio configuration 81
Table 3-3: Output dividing ratio and clock frequency 81
Table 3-4: CLOCK Module Base Address 88
Table 3-5: CLOCK Register Map 88
Table 3-6: Clock Status Register (CLKSTS) Layout 89
Table 3-7: Clock Status Register (CLKSTS) Field Description 89
Table 3-8: Clock Regulator Control Register (CLKREGCTL) Layout 91
Table 3-9: Clock Regulator Control Register (CLKREGCTL) Field Description 91
Table 3-10: RCO0 Control Register (RCO0CTL) Layout 92
Table 3-11: RCO0 Control Register (RCO0CTL) Field Description 92
Table 3-12: RCO1 Control Register (RCO1CTL) Layout 93
Table 3-13: RCO1 Control Register (RCO1CTL) Field Description 93
Table 3-14: Crystal Oscillator Control Register (XOCTL) Layout 94
Table 3-15: Crystal Oscillator Control Register (XOCTL) Field Description 94
Table 3-16: PLL Control Register 0 (PLLCTL0) Layout 95
Table 3-17: PLL Control Register 0 (PLLCTL0) Field Description 95
Table 3-18: PLL Control Register 1 (PLLCTL1) Layout 96

SPINTROL

Table 3-19: PLL Control Register 1 (PLLCTL1) Field Description 96
Table 3-20: Clock Detection Control Register (CLKDETCTL) Layout 97
Table 3-21: Clock Detection Control Register (CLKDETCTL) Field Description 97
Table 3-22: Clock Detection Counter Threshold Register (CLKDETCTH) Layout 98
Table 3-23: Clock Detection Counter Threshold Register (CLKDETCTH) Field Description 98
Table 3-24: Clock Detection Counter Register (CLKDETCNT) Layout 99
Table 3-25: Clock Detection Counter Register (CLKDETCNT) Field Description 99
Table 3-26: Clock Interrupt Flag Register (CLKIF) Layout 100
Table 3-27: Clock Interrupt Flag Register (CLKIF) Field Description 100
Table 3-28: Clock Interrupt Clear Register (CLKIC) Layout 101
Table 3-29: Clock Interrupt Clear Register (CLKIC) Field Description 101
Table 3-30: Clock Interrupt Enable Register (CLKIE) Layout 102
Table 3-31: Clock Interrupt Enable Register (CLKIE) Field Description 102
Table 3-32: Clock Trip-Zone Event Enable Register (CLKTZE) Layout 103
Table 3-33: Clock Trip-Zone Event Enable Register (CLKTZE) Field Description 103
Table 3-34: SYSCLK0 Control Register (SYSCLK0CTL) Layout 104
Table 3-35: SYSCLK0 Control Register (SYSCLK0CTL) Field Description 104
Table 3-36: HCLK Control Register (HCLKCTL) Layout 104
Table 3-37: HCLK Control Register (HCLKCTL) Field Description 104
Table 3-38: ADC Clock Control Register (ADCCLKCTL) Layout 105
Table 3-39: ADC Clock Control Register (ADCCLKCTL) Field Description 105
Table 3-40: PWM Clock Control Register (PWMCLKCTL) Layout 105
Table 3-41: PWM Clock Control Register (PWMCLKCTL) Field Description 105
Table 3-42: ECAP Clock Control Register (ECAPCLKCTL) Layout 106
Table 3-43: ECAP Clock Control Register (ECAPCLKCTL) Field Description 106
Table 3-44: Timer 0 Clock Control Register (TMR0CLKCTL) Layout 106
Table 3-45: Timer 0 Clock Control Register (TMR0CLKCTL) Field Description 106
Table 3-46: Timer 1 Clock Control Register (TMR1CLKCTL) Layout 107
Table 3-47: Timer 1 Clock Control Register (TMR1CLKCTL) Field Description 107
Table 3-48: Timer 2 Clock Control Register (TMR2CLKCTL) Layout 107
Table 3-49: Timer 2 Clock Control Register (TMR2CLKCTL) Field Description 107
Table 3-50: SIO Clock Control Register (SIOCLKCTL) Layout 108
Table 3-51: SIO Clock Control Register (SIOCLKCTL) Field Description 108
Table 3-52: SYSCLK1 Control Register (SYSCLK1CTL) Layout 108
Table 3-53: SYSCLK1 Control Register (SYSCLK1CTL) Field Description 108
Table 3-54: PCLK Control Register (PCLKCTL) Layout 109
Table 3-55: PCLK Control Register (PCLKCTL) Field Description 109
Table 3-56: Deglitch Clock Control Register (DGCLKCTL) Layout 109
Table 3-57: Deglitch Clock Control Register (DGCLKCTL) Field Description 109
Table 3-58: UART Clock Control Register (UARTCLKCTL) Layout 110
Table 3-59: UART Clock Control Register (UARTCLKCTL) Field Description 110
Table 3-60: SSP Clock Control Register (SSPCLKCTL) Layout 110
Table 3-61: SSP Clock Control Register (SSPCLKCTL) Field Description 110
Table 3-62: I2C Clock Control Register (I2CCLKCTL) Layout 111
Table 3-63: I2C Clock Control Register (I2CCLKCTL) Field Description 111
Table 3-64: WDT0 Clock Control Register (WDT0CLKCTL) Layout 112
Table 3-65: WDT0 Clock Control Register (WDT0CLKCTL) Field Description 112

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Table 3-66: WDT1 Clock Control Register (WDT1CLKCTL) Layout 113
Table 3-67: WDT1 Clock Control Register (WDT1CLKCTL) Field Description 113
Table 3-68: Clock Register Write-Allow Key Register (CLKREGKEY) Layout 113
Table 3-69: Clock Register Write-Allow Key Register (CLKREGKEY) Field Description 113
Table 4-1: I/O function channel definition 117
Table 4-2: PINMUX Module Base Address 122
Table 4-3: PINMUX Register Map 122
Table 4-4: GPIO# Pin Control Register (GPIO#) Layout (# = 0 ~61) 124
Table 4-5: GPIO# Pin Control Register (GPIO#) Field Description (# = 0 ~61) 124
Table 4-6: PINMUX Register Write-Allow Key Register (PINMUXREGKEY) Layout 125
Table 4-7: PINMUX Register Write-Allow Key Register (PINMUXREGKEY) Field Description 125
Table 4-8: GPIO Module Base Address 126
Table 4-9: GPIO Register Map 126
Table 4-10: GPIO Pin Level Register 0 (GPLR0) Layout 128
Table 4-11: GPIO Pin Level Register 0 (GPLR0) Field Description 128
Table 4-12: GPIO Pin Level Register 1 (GPLR1) Layout 128
Table 4-13: GPIO Pin Level Register 1 (GPLR1) Field Description 128
Table 4-14: GPIO Pin Direction Register 0 (GPDR0) Layout 129
Table 4-15: GPIO Pin Direction Register 0 (GPDR0) Field Description 129
Table 4-16: GPIO Pin Direction Register 1 (GPDR1) Layout 129
Table 4-17: GPIO Pin Direction Register 1 (GPDR1) Field Description 129
Table 4-18: GPIO Pin Output Set Register 0 (GSLR0) Layout 130
Table 4-19: GPIO Pin Output Set Register 0 (GSLR0) Field Description 130
Table 4-20: GPIO Pin Output Set Register 1 (GSLR1) Layout 130
Table 4-21: GPIO Pin Output Set Register 1 (GSLR1) Field Description 130
Table 4-22: GPIO Pin Output Clear Register 0 (GCLR0) Layout 131
Table 4-23: GPIO Pin Output Clear Register 0 (GCLR0) Field Description 131
Table 4-24: GPIO Pin Output Clear Register 1 (GCLR1) Layout 131
Table 4-25: GPIO Pin Output Clear Register 1 (GCLR1) Field Description 131
Table 4-26: GPIO Rising Edge Detect Enable Register 0 (GRER0) Layout 132
Table 4-27: GPIO Rising Edge Detect Enable Register 0 (GRER0) Field Description 132
Table 4-28: GPIO Rising Edge Detect Enable Register 1 (GRER1) Layout 132
Table 4-29: GPIO Rising Edge Detect Enable Register 1 (GRER1) Field Description 132
Table 4-30: GPIO Falling Edge Detect Enable Register 0 (GFER0) Layout 133
Table 4-31: GPIO Falling Edge Detect Enable Register 0 (GFER0) Field Description 133
Table 4-32: GPIO Falling Edge Detect Enable Register 1 (GFER1) Layout 133
Table 4-33: GPIO Falling Edge Detect Enable Register 1 (GFER1) Field Description 133
Table 4-34: GPIO Edge Detect Status Register 0 (GEDR0) Layout 134
Table 4-35: GPIO Edge Detect Status Register 0 (GEDR0) Field Description 134
Table 4-36: GPIO Edge Detect Status Register 1 (GEDR1) Layout 134
Table 4-37: GPIO Edge Detect Status Register 1 (GEDR1) Field Description 134
Table 4-38: GPIO Pin Bitwise Set Direction Register 0 (GSDR0) Layout 135
Table 4-39: GPIO Pin Bitwise Set Direction Register 0 (GSDR0) Field Description 135
Table 4-40: GPIO Pin Bitwise Set Direction Register 1 (GSDR1) Layout 135
Table 4-41: GPIO Pin Bitwise Set Direction Register 1 (GSDR1) Field Description 135
Table 4-42: GPIO Pin Bitwise Clear Direction Register 0 (GCDR0) Layout 136
Table 4-43: GPIO Pin Bitwise Clear Direction Register 0 (GCDR0) Field Description 136

SPINTROL

Table 4-44: GPIO Pin Bitwise Clear Direction Register 1 (GCDR1) Layout 136
Table 4-45: GPIO Pin Bitwise Clear Direction Register 1 (GCDR1) Field Description 136
Table 4-46: GPIO Bitwise Set Rising Edge Detect Enable Register 0 (GSRER0) Layout 137
Table 4-47: GPIO Bitwise Set Rising Edge Detect Enable Register 0 (GSRER0) Field Description 137
Table 4-48: GPIO Bitwise Set Rising Edge Detect Enable Register 1 (GSRER1) Layout 137
Table 4-49: GPIO Bitwise Set Rising Edge Detect Enable Register 1 (GSRER1) Field Description 137
Table 4-50: GPIO Bitwise Clear Rising Edge Detect Enable Register 0 (GCRER0) Layout 138
Table 4-51: GPIO Bitwise Clear Rising Edge Detect Enable Register 0 (GCRER0) Field Description 138
Table 4-52: GPIO Bitwise Clear Rising Edge Detect Enable Register 1 (GCRER1) Layout 138
Table 4-53: GPIO Bitwise Clear Rising Edge Detect Enable Register 1 (GCRER1) Field Description 138
Table 4-54: GPIO Bitwise Set Falling Edge Detect Enable Register 0 (GSFER0) Layout 139
Table 4-55: GPIO Bitwise Set Falling Edge Detect Enable Register 0 (GSFER0) Field Description 139
Table 4-56: GPIO Bitwise Set Falling Edge Detect Enable Register 1 (GSFER1) Layout 139
Table 4-57: GPIO Bitwise Set Falling Edge Detect Enable Register 1 (GSFER1) Field Description 139
Table 4-58: GPIO Bitwise Clear Falling Edge Detect Enable Register 0 (GCFER0) Layout 140
Table 4-59: GPIO Bitwise Clear Falling Edge Detect Enable Register 0 (GCFER0) Field Description 140
Table 4-60: GPIO Bitwise Clear Falling Edge Detect Enable Register 1 (GCFER1) Layout 140
Table 4-61: GPIO Bitwise Clear Falling Edge Detect Enable Register 1 (GCFER1) Field Description 140
Table 4-62: GPIO Edge-Triggered Interrupt Enable Register 0 (GEIE0) Layout 141
Table 4-63: GPIO Edge-Triggered Interrupt Enable Register 0 (GEIE0) Field Description 141
Table 4-64: GPIO Edge-Triggered Interrupt Enable Register 1 (GEIE1) Layout 141
Table 4-65: GPIO Edge-Triggered Interrupt Enable Register 1 (GEIE1) Field Description 141
Table 4-66: GPIO Level-Triggered Interrupt Flag Register 0 (GLIF0) Layout 142
Table 4-67: GPIO Level-Triggered Interrupt Flag Register 0 (GLIF0) Field Description 142
Table 4-68: GPIO Level-Triggered Interrupt Flag Register 1 (GLIF1) Layout 142
Table 4-69: GPIO Level-Triggered Interrupt Flag Register 1 (GLIF1) Field Description 142
Table 4-70: GPIO Level-Triggered Interrupt Enable Register 0 (GLIE0) Layout 143
Table 4-71: GPIO Level-Triggered Interrupt Enable Register 0 (GLIE0) Field Description 143
Table 4-72: GPIO Level-Triggered Interrupt Enable Register 1 (GLIE1) Layout 143
Table 4-73: GPIO Level-Triggered Interrupt Enable Register 1 (GLIE1) Field Description 143
Table 4-74: GPIO Level-Triggered Interrupt Clear Register 0 (GLIC0) Layout 144
Table 4-75: GPIO Level-Triggered Interrupt Clear Register 0 (GLIC0) Field Description 144
Table 4-76: GPIO Level-Triggered Interrupt Clear Register 1 (GLIC1) Layout 144
Table 4-77: GPIO Level-Triggered Interrupt Clear Register 1 (GLIC1) Field Description 144
Table 4-78: GPIO Level-Triggered Interrupt Force Register 0 (GLIFRC0) Layout 145
Table 4-79: GPIO Level-Triggered Interrupt Force Register 0 (GLIFRC0) Field Description 145
Table 4-80: GPIO Level-Triggered Interrupt Force Register 1 (GLIFRC1) Layout 145
Table 4-81: GPIO Level-Triggered Interrupt Force Register 1 (GLIFRC1) Field Description 145
Table 4-82: GPIO Level-Triggered Interrupt Polarity Register 0 (GLIPOL0) Layout 146
Table 4-83: GPIO Level-Triggered Interrupt Polarity Register 0 (GLIPOL0) Field Description 146
Table 4-84: GPIO Level-Triggered Interrupt Polarity Register 1 (GLIPOL1) Layout 146
Table 4-85: GPIO Level-Triggered Interrupt Polarity Register 1 (GLIPOL1) Field Description 146
Table 4-86: GPIO Interrupt Flag Register (GIF) Layout 147
Table 4-87: GPIO Interrupt Flag Register (GIF) Field Description 147
Table 4-88: GPIO Interrupt Flag Clear Register (GIC) Layout 148
Table 4-89: GPIO Interrupt Flag Clear Register (GIC) Field Description 148
Table 4-90: GPIO Register Write-Allow Key Register (GPIOREGKEY) Layout 148

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Table 4-91: GPIO Register Write-Allow Key Register (GPIOREGKEY) Field Description 148
Table 5-1: Vector table for SPC2168 149
Table 6-1: Padding scheme 156
Table 6-2: Error code for different AES block cipher modes 156
Table 6-3: AES output vector 157
Table 6-4: AES Module Base Address 158
Table 6-5: AES Register Map 158
Table 6-6: AES Control Register 0 (AESCTL0) Layout 159
Table 6-7: AES Control Register 0 (AESCTL0) Field Description 159
Table 6-8: AES Status Register (AESSTS) Layout 161
Table 6-9: AES Status Register (AESSTS) Field Description 161
Table 6-10: AES Associate String Length Register (AESASTRLEN) Layout 162
Table 6-11: AES Associate String Length Register (AESASTRLEN) Field Description 162
Table 6-12: AES Message String Length Register (AESMSTRLEN) Layout 162
Table 6-13: AES Message String Length Register (AESMSTRLEN) Field Description 162
Table 6-14: AES Input Message Word Register (AESSTRIN) Layout 163
Table 6-15: AES Input Message Word Register (AESSTRIN) Field Description 163
Table 6-16: AES Initial Vector Register 0 (AESIV0) Layout 163
Table 6-17: AES Initial Vector Register 0 (AESIV0) Field Description 163
Table 6-18: AES Initial Vector Register 1 (AESIV1) Layout 164
Table 6-19: AES Initial Vector Register 1 (AESIV1) Field Description 164
Table 6-20: AES Initial Vector Register 2 (AESIV2) Layout 164
Table 6-21: AES Initial Vector Register 2 (AESIV2) Field Description 164
Table 6-22: AES Initial Vector Register 3 (AESIV3) Layout 165
Table 6-23: AES Initial Vector Register 3 (AESIV3) Field Description 165
Table 6-24: AES Key Register 0 (AESKEY0) Layout 165
Table 6-25: AES Key Register 0 (AESKEY0) Field Description 165
Table 6-26: AES Key Register 1 (AESKEY1) Layout 166
Table 6-27: AES Key Register 1 (AESKEY1) Field Description 166
Table 6-28: AES Key Register 2 (AESKEY2) Layout 166
Table 6-29: AES Key Register 2 (AESKEY2) Field Description 166
Table 6-30: AES Key Register 3 (AESKEY3) Layout 167
Table 6-31: AES Key Register 3 (AESKEY3) Field Description 167
Table 6-32: AES Key Register 4 (AESKEY4) Layout 167
Table 6-33: AES Key Register 4 (AESKEY4) Field Description 167
Table 6-34: AES Key Register 5 (AESKEY5) Layout 168
Table 6-35: AES Key Register 5 (AESKEY5) Field Description 168
Table 6-36: AES Key Register 6 (AESKEY6) Layout 168
Table 6-37: AES Key Register 6 (AESKEY6) Field Description 168
Table 6-38: AES Key Register 7 (AESKEY7) Layout 169
Table 6-39: AES Key Register 7 (AESKEY7) Field Description 169
Table 6-40: AES Output Message Word Register (AESSTROUT) Layout 169
Table 6-41: AES Output Message Word Register (AESSTROUT) Field Description 169
Table 6-42: AES Output Vector Register 0 (AESOV0) Layout 170
Table 6-43: AES Output Vector Register 0 (AESOV0) Field Description 170
Table 6-44: AES Output Vector Register 1 (AESOV1) Layout 170
Table 6-45: AES Output Vector Register 1 (AESOV1) Field Description 170

SPINTROL

Table 6-46: AES Output Vector Register 2 (AESOV2) Layout 171
Table 6-47: AES Output Vector Register 2 (AESOV2) Field Description 171
Table 6-48: AES Output Vector Register 3 (AESOV3) Layout 171
Table 6-49: AES Output Vector Register 3 (AESOV3) Field Description 171
Table 6-50: AES Interrupt Status Register (AESIF) Layout 172
Table 6-51: AES Interrupt Status Register (AESIF) Field Description 172
Table 6-52: AES Interrupt Enable Register (AESIE) Layout 173
Table 6-53: AES Interrupt Enable Register (AESIE) Field Description 173
Table 6-54: AES Interrupt Raw Status Register (AESRAWIF) Layout 174
Table 6-55: AES Interrupt Raw Status Register (AESRAWIF) Field Description 174
Table 6-56: AES Interrupt Clear Register (AESIC) Layout 175
Table 6-57: AES Interrupt Clear Register (AESIC) Field Description 175
Table 7-1: CRC Module Base Address 178
Table 7-2: CRC Register Map 178
Table 7-3: CRC Interrupt Flag Register (CRCIF) Layout 179
Table 7-4: CRC Interrupt Flag Register (CRCIF) Field Description 179
Table 7-5: CRC Raw Interrupt Flag Register (CRCRAWIF) Layout 179
Table 7-6: CRC RAW Interrupt Flag Register (CRCRAWIF) Field Description 179
Table 7-7: CRC Interrupt Clear Register (CRCIC) Layout 180
Table 7-8: CRC Interrupt Clear Register (CRCIC) Field Description 180
Table 7-9: CRC Interrupt Enable Register (CRCIE) Layout 180
Table 7-10: CRC Interrupt Enable Register (CRCIE) Field Description 180
Table 7-11: CRC Control Register (CRCCTL) Layout 181
Table 7-12: CRC Control Register (CRCCRL) Field Description 181
Table 7-13: CRC Stream Length Register (CRCSTRLEN) Layout 182
Table 7-14: CRC Stream Length Register (CRCSTRLEN) Field Description 182
Table 7-15: CRC Stream Input Register (CRCSTRIN) Layout 182
Table 7-16: CRC Stream Input Register (CRCSTRIN) Field Description 182
Table 7-17: CRC Result Register (CRCRESULT) Layout 183
Table 7-18: CRC Result Register (CRCRESULT) Field Description 183
Table 8-1: Timer Module Base Address 186
Table 8-2: Timer Register Map 186
Table 8-3: Timer Control Register (TMRCTL) Layout 187
Table 8-4: Timer Control Register (TMRCTL) Field Description 187
Table 8-5: Timer Counter Value Register (TMRCNT) Layout 188
Table 8-6: Timer Counter Value Register (TMRCNT) Field Description 188
Table 8-7: Timer Reload Value Register (TMRRELOAD) Layout 188
Table 8-8: Timer Reload Value Register (TMRRELOAD) Field Description 188
Table 8-9: Timer Interrupt Flag Register (TMRIF) Layout 189
Table 8-10: Timer Interrupt Flag Register (TMRIF) Field Description 189
Table 8-11: Timer Raw Interrupt Flag Register (TMRRAWIF) Layout 189
Table 8-12: Timer Raw Interrupt Flag Register (TMRRAWIF) Field Description 189
Table 8-13: Timer Interrupt Enable Register (TMRIE) Layout 190
Table 8-14: Timer Interrupt Enable Register (TMRIE) Field Description 190
Table 8-15: Timer Interrupt Force Register (TMRIFRC) Layout 190
Table 8-16: Timer Interrupt Force Register (TMRIFRC) Field Description 190
Table 8-17: Timer Interrupt Clear Register (TMRIC) Layout 191

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Table 8-18: Timer Interrupt Clear Register (TMRIC) Field Description 191
Table 9-1: WDT Module Base Address 194
Table 9-2: WDT Register Map 194
Table 9-3: Watchdog Timer Load Register (WDTLOAD) Layout 195
Table 9-4: Watchdog Timer Load Register (WDTLOAD) Field Description 195
Table 9-5: Watchdog Timer Current Value Register (WDTCNT) Layout 195
Table 9-6: Watchdog Timer Current Value Register (WDTCNT) Field Description 195
Table 9-7: Watchdog Timer Control Register (WDTCTL) Layout 196
Table 9-8: Watchdog Timer Control Register (WDTCTL) Field Description 196
Table 9-9: Watchdog Timer Clear Interrupt Register (WDTIC) Layout 197
Table 9-10: Watchdog Timer Clear Interrupt Register (WDTIC) Field Description 197
Table 9-11: Watchdog Timer Raw Interrupt Status Register (WDTRAWIF) Layout 197
Table 9-12: Watchdog Timer Raw Interrupt Status Register (WDTRAWIF) Field Description 197
Table 9-13: Watchdog Timer Interrupt Status Register (WDTIF) Layout 198
Table 9-14: Watchdog Timer Interrupt Status Register (WDTIF) Field Description 198
Table 9-15: Watchdog Timer Lock Register (WDTREGKEY) Layout 199
Table 9-16: Watchdog Timer Lock Register (WDTREGKEY) Field Description 199
Table 10-1: Action-Qualifier event priority for Up-Count mode 209
Table 10-2: Action-Qualifier Event Priority for Down-Count Mode 209
Table 10-3: Action-Qualifier Event Priority for Up-Down-Count Mode 209
Table 10-4: Typical Dead-Band operating modes 212
Table 10-5: Priority of events that effect the final PWM outputs 216
Table 10-6: PWM Module Base Address 222
Table 10-7: PWM Register Map 222
Table 10-8: Shadow Status Register (SHADOWSTS) Layout 224
Table 10-9: Shadow Status Register (SHADOWSTS) Field Description 224
Table 10-10: Global Shadow to Active Load Control Register 0 (GLDCTL0) Layout 226
Table 10-11: Global Shadow to Active Load Control Register 0 (GLDCTL0) Field Description 226
Table 10-12: Global Shadow to Active Load Control Register 1 (GLDCTL1) Layout 227
Table 10-13: Global Shadow to Active Load Control Register 1 (GLDCTL1) Field Description 227
Table 10-14: Global Shadow to Active Load Select Register (GLDSEL) Layout 228
Table 10-15: Global Shadow to Active Load Select Register (GLDSEL) Field Description 228
Table 10-16: PWM Link Control Register (PWMLINK) Layout 230
Table 10-17: PWM Link Control Register (PWMLINK) Field Description 230
Table 10-18: Time-Base Control Register (TBCTL) Layout 233
Table 10-19: Time-Base Control Register (TBCTL) Field Description 233
Table 10-20: Time-Base Period Register (TBPRD) Layout 235
Table 10-21: Time-Base Period Register (TBPRD) Field Description 235
Table 10-22: Time-Base Period Active Register (TBPRDA) Layout 236
Table 10-23: Time-Base Period Active Register (TBPRDA) Field Description 236
Table 10-24: Time-Base Phase Register (TBPHS) Layout 237
Table 10-25: Time-Base Phase Register (TBPHS) Field Description 237
Table 10-26: Time-Base Counter Register (TBCNT) Layout 237
Table 10-27: Time-Base Counter Register (TBCNT) Field Description 237
Table 10-28: Time-Base Status Register (TBSTS) Layout 238
Table 10-29: Time-Base Status Register (TBSTS) Field Description 238
Table 10-30: Time-Base Status Clear Register (TBSTSCLR) Layout 239

SPINTROL

Table 10-31: Time-Base Status Clear Register (TBSTSCLR) Field Description 239
Table 10-32: Counter-Compare Control Register (CMPCTL) Layout 241
Table 10-33: Counter-Compare Control Register (CMPCTL) Field Description 241
Table 10-34: Counter-Compare A Threshold Register (CMPA) Layout 243
Table 10-35: Counter-Compare A Threshold Register (CMPA) Field Description 243
Table 10-36: Counter-Compare A Threshold Active Register (CMPAA) Layout 244
Table 10-37: Counter-Compare A Threshold Active Register (CMPAA) Field Description 244
Table 10-38: Counter-Compare B Threshold Register (CMPB) Layout 244
Table 10-39: Counter-Compare B Threshold Register (CMPB) Field Description 244
Table 10-40: Counter-Compare B Threshold Active Register (CMPBA) Layout 245
Table 10-41: Counter-Compare B Threshold Active Register (CMPBA) Field Description 245
Table 10-42: Counter-Compare C Threshold Register (CMPC) Layout 245
Table 10-43: Counter-Compare C Threshold Register (CMPC) Field Description 245
Table 10-44: Counter-Compare C Threshold Active Register (CMPCA) Layout 246
Table 10-45: Counter-Compare C Threshold Active Register (CMPCA) Field Description 246
Table 10-46: Counter-Compare D Threshold Register (CMPD) Layout 246
Table 10-47: Counter-Compare D Threshold Register (CMPD) Field Description 246
Table 10-48: Counter-Compare D Threshold Active Register (CMPDA) Layout 247
Table 10-49: Counter-Compare D Threshold Active Register (CMPDA) Field Description 247
Table 10-50: Action-Qualifier Control Register (AQCTL) Layout 248
Table 10-51: Action-Qualifier Control Register (AQCTL) Field Description 248
Table 10-52: Action-Qualifier Output A Control Register (AQCTLA) Layout 250
Table 10-53: Action-Qualifier Output A Control Register (AQCTLA) Field Description 250
Table 10-54: Action-Qualifier Output A Control Active Register (AQCTLAA) Layout 252
Table 10-55: Action-Qualifier Output A Control Active Register (AQCTLAA) Field Description 252
Table 10-56: Action-Qualifier Output B Control Register (AQCTLB) Layout 254
Table 10-57: Action-Qualifier Output B Control Register (AQCTLB) Field Description 254
Table 10-58: Action-Qualifier Output B Control Active Register (AQCTLBA) Layout 256
Table 10-59: Action-Qualifier Output B Control Active Register (AQCTLBA) Field Description 256
Table 10-60: Action-Qualifier Software Force Register (AQSFRC) Layout 258
Table 10-61: Action-Qualifier Software Force Register (AQSFRC) Field Description 258
Table 10-62: Action-Qualifier Continuous Software Force Register (AQCSFRC) Layout 259
Table 10-63: Action-Qualifier Continuous Software Force Register (AQCSFRC) Field Description 259
Table 10-64: Action-Qualifier Continuous Software Force Active Register (AQCSFRCA) Layout 260
Table 10-65: Action-Qualifier Continuous Software Force Active Register (AQCSFRCA) Field Description 260
Table 10-66: Dead-Band Generator Control Register (DBCTL) Layout 261
Table 10-67: Dead-Band Generator Control Register (DBCTL) Field Description 261
Table 10-68: Dead-Band Generator Control Active Register (DBCTLA) Layout 264
Table 10-69: Dead-Band Generator Control Active Register (DBCTLA) Field Description 264
Table 10-70: Dead-Band Generator Rising Edge Delay Register (DBRED) Layout 265
Table 10-71: Dead-Band Generator Rising Edge Delay Register (DBRED) Field Description 265
Table 10-72: Dead-Band Generator Rising Edge Delay Active Register (DBREDA) Layout 266
Table 10-73: Dead-Band Generator Rising Edge Delay Active Register (DBREDA) Field Description 266
Table 10-74: Dead-Band Generator Falling Edge Delay Register (DBFED) Layout 266
Table 10-75: Dead-Band Generator Falling Edge Delay Register (DBFED) Field Description 266
Table 10-76: Dead-Band Generator Falling Edge Delay Active Register (DBFEDA) Layout 267

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Table 10-77: Dead-Band Generator Falling Edge Delay Active Register (DBFEDA) Field Description 267
Table 10-78: Trip-Zone Event Select Register (TZSEL) Layout 268
Table 10-79: Trip-Zone Event Select Register (TZSEL) Field Description 268
Table 10-80: Trip-Zone Status Register (TZSTS) Layout 270
Table 10-81: Trip-Zone Status Register (TZSTS) Field Description 270
Table 10-82: Trip-Zone Status Clear Register (TZSTSCLR) Layout 272
Table 10-83: Trip-Zone Status Clear Register (TZSTSCLR) Field Description 272
Table 10-84: Trip-Zone Digital Compare Event Select Register (TZDCSEL) Layout 275
Table 10-85: Trip-Zone Digital Compare Event Select Register (TZDCSEL) Field Description 275
Table 10-86: Trip-Zone Output A Control Register (TZACTL) Layout 277
Table 10-87: Trip-Zone Output A Control Register (TZACTL) Field Description 277
Table 10-88: Trip-Zone Output B Control Register (TZBCTL) Layout 279
Table 10-89: Trip-Zone Output B Control Register (TZBCTL) Field Description 279
Table 10-90: Trip-Zone Flag Register (TZIF) Layout 281
Table 10-91: Trip-Zone Flag Register (TZIF) Field Description 281
Table 10-92: Trip-Zone Clear Register (TZIC) Layout 282
Table 10-93: Trip-Zone Clear Register (TZIC) Field Description 282
Table 10-94: Trip-Zone Interrupt Enable Register (TZIE) Layout 284
Table 10-95: Trip-Zone Interrupt Enable Register (TZIE) Field Description 284
Table 10-96: Trip-Zone Force Register (TZFRC) Layout 285
Table 10-97: Trip-Zone Force Register (TZFRC) Field Description 285
Table 10-98: Digital Compare AL Trip Select Register (DCALTRIPSEL) Layout 286
Table 10-99: Digital Compare AL Trip Select Register (DCALTRIPSEL) Field Description 286
Table 10-100: Digital Compare AH Trip Select Register (DCAHTRIPSEL) Layout 289
Table 10-101: Digital Compare AH Trip Select Register (DCAHTRIPSEL) Field Description 289
Table 10-102: Digital Compare BL Trip Select Register (DCBLTRIPSEL) Layout 292
Table 10-103: Digital Compare BL Trip Select Register (DCBLTRIPSEL) Field Description 292
Table 10-104: Digital Compare BH Trip Select Register (DCBHTRIPSEL) Layout 295
Table 10-105: Digital Compare BH Trip Select Register (DCBHTRIPSEL) Field Description 295
Table 10-106: Digital Compare A Control Register (DCACTL) Layout 298
Table 10-107: Digital Compare A Control Register (DCACTL) Field Description 298
Table 10-108: Digital Compare B Control Register (DCBCTL) Layout 299
Table 10-109: Digital Compare B Control Register (DCBCTL) Field Description 299
Table 10-110: Digital Compare Filter Register (DCFCTL) Layout 300
Table 10-111: Digital Compare Filter Register (DCFCTL) Field Description 300
Table 10-112: Digital Compare Filter Offset Register (DCFOFFSET) Layout 301
Table 10-113: Digital Compare Filter Offset Register (DCFOFFSET) Field Description 301
Table 10-114: Digital Compare Filter Offset Counter Register (DCFOFFSETCNT) Layout 302
Table 10-115: Digital Compare Filter Offset Counter Register (DCFOFFSETCNT) Field Description 302
Table 10-116: Digital Compare Filter Window Register (DCFWINDOW) Layout 303
Table 10-117: Digital Compare Filter Window Register (DCFWINDOW) Field Description 303
Table 10-118: Digital Compare Filter Window Counter Register (DCFWINDOWCNT) Layout 304
Table 10-119: Digital Compare Filter Window Counter Register (DCFWINDOWCNT) Field Description 304
Table 10-120: Digital Compare Capture Control Register (DCCAPCTL) Layout 305
Table 10-121: Digital Compare Capture Control Register (DCCAPCTL) Field Description 305
Table 10-122: Digital Compare Counter Capture Register (DCCAP) Layout 306
Table 10-123: Digital Compare Counter Capture Register (DCCAP) Field Description 306

SPINTROL

Table 10-124: Event-Trigger Control Register (ETCTL) Layout 307
Table 10-125: Event-Trigger Control Register (ETCTL) Field Description 307
Table 10-126: Event-Trigger Prescale Register (ETPS) Layout 310
Table 10-127: Event-Trigger Prescale Register (ETPS) Field Description 310
Table 10-128: Event-Trigger Flag Register (ETFLG) Layout 312
Table 10-129: Event-Trigger Flag Register (ETFLG) Field Description 312
Table 10-130: Event-Trigger Clear Register (ETCLR) Layout 313
Table 10-131: Event-Trigger Clear Register (ETCLR) Field Description 313
Table 10-132: Event-Trigger Force Register (ETFRC) Layout 314
Table 10-133: Event-Trigger Force Register (ETFRC) Field Description 314
Table 10-134: PWM Register Write-Allow Key Register (PWMREGKEY) Layout 315
Table 10-135: PWM Register Write-Allow Key Register (PWMREGKEY) Field Description 315
Table 10-136: PWMCFG Module Base Address 316
Table 10-137: PWMCFG Register Map 316
Table 10-138: TZ0 Source Control Register (TZ0SRCCTL) Layout 317
Table 10-139: TZ0 Source Control Register (TZ0SRCCTL) Field Description 317
Table 10-140: TZ1 Source Control Register (TZ1SRCCTL) Layout 317
Table 10-141: TZ1 Source Control Register (TZ1SRCCTL) Field Description 317
Table 10-142: TZ2 Source Control Register (TZ2SRCCTL) Layout 318
Table 10-143: TZ2 Source Control Register (TZ2SRCCTL) Field Description 318
Table 10-144: TZ3 Source Control Register (TZ3SRCCTL) Layout 318
Table 10-145: TZ3 Source Control Register (TZ3SRCCTL) Field Description 318
Table 10-146: TZ4 Source Control Register (TZ4SRCCTL) Layout 319
Table 10-147: TZ4 Source Control Register (TZ4SRCCTL) Field Description 319
Table 10-148: Global PWM Force Synchronization Register (FRCSYNC) Layout 320
Table 10-149: Global PWM Force Synchronization Register (FRCSYNC) Field Description 320
Table 10-150: GPIO PWMSYNCI Control Register (GPIOSYNCCTL) Layout 321
Table 10-151: GPIO PWMSYNCI Control Register (GPIOSYNCCTL) Field Description 321
Table 10-152: GPIO Force PWMSYNCI Enable Register (GPIOSYNCEN) Layout 322
Table 10-153: GPIO Force PWMSYNCI Enable Register (GPIOSYNCEN) Field Description 322
Table 10-154: Timer 0 Force PWMSYNCI Enable Register (TMR0SYNCEN) Layout 323
Table 10-155: Timer 0 Force PWMSYNCI Enable Register (TMR0SYNCEN) Field Description 323
Table 10-156: Timer 1 Force PWMSYNCI Enable Register (TMR1SYNCEN) Layout 324
Table 10-157: Timer 1 Force PWMSYNCI Enable Register (TMR1SYNCEN) Field Description 324
Table 10-158: Timer 2 Force PWMSYNCI Enable Register (TMR2SYNCEN) Layout 325
Table 10-159: Timer 2 Force PWMSYNCI Enable Register (TMR2SYNCEN) Field Description 325
Table 10-160: PWMSYNCO Control Register (SYNCOCTL) Layout 326
Table 10-161: PWMSYNCO Control Register (SYNCOCTL) Field Description 326
Table 10-162: PWMSOCA Output Control Register (SOCAOCTL) Layout 327
Table 10-163: PWMSOCA Output Control Register (SOCAOCTL) Field Description 327
Table 10-164: PWMSOCB Output Control Register (SOCBOCTL) Layout 329
Table 10-165: PWMSOCB Output Control Register (SOCBOCTL) Field Description 329
Table 10-166: PWMSOCC Output Control Register (SOCCOCTL) Layout 331
Table 10-167: PWMSOCC Output Control Register (SOCCOCTL) Field Description 331
Table 10-168: PWMCFG Register Write-Allow Key Register (PWMCFGKEY) Layout 332
Table 10-169: PWMCFG Register Write-Allow Key Register (PWMCFGKEY) Field Description 332
Table 11-1: ECAP Module Base Address 352

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Table 11-2: ECAP Register Map 352
Table 11-3: Capture Source Input Control Register (CAPSRCCTL) Layout 353
Table 11-4: Capture Source Input Control Register (CAPSRCCTL) Field Description 353
Table 11-5: Capture Synchronization Source Input Control Register (CAPSYNCICTL) Layout 353
Table 11-6: Capture Synchronization Source Input Control Register (CAPSYNCICTL) Field Description 353
Table 11-7: Time-Stamp Counter Register (CAPTSCNT) Layout 354
Table 11-8: Time-Stamp Counter Register (CAPTSCNT) Field Description 354
Table 11-9: Counter Phase Offset Value Register (CAPCNTPHS) Layout 354
Table 11-10: Counter Phase Offset Value Register (CAPCNTPHS) Field Description 354
Table 11-11: Capture Register 0 (CAP0) Layout 355
Table 11-12: Capture Register 0 (CAP0) Field Description 355
Table 11-13: Capture Register 1 (CAP1) Layout 356
Table 11-14: Capture Register 1 (CAP1) Field Description 356
Table 11-15: Capture Register 2 (CAP2) Layout 357
Table 11-16: Capture Register 2 (CAP2) Field Description 357
Table 11-17: Capture Register 3 (CAP3) Layout 357
Table 11-18: Capture Register 3 (CAP3) Field Description 357
Table 11-19: Capture Control Register (CAPCTL) Layout 358
Table 11-20: Capture Control Register (CAPCTL) Field Description 358
Table 11-21: Capture Interrupt Flag Register (CAPIF) Layout 362
Table 11-22: Capture Interrupt Flag Register (CAPIF) Field Description 362
Table 11-23: Capture Interrupt Enable Register (CAPIE) Layout 364
Table 11-24: Capture Interrupt Enable Register (CAPIE) Field Description 364
Table 11-25: Capture Interrupt Clear Register (CAPIC) Layout 365
Table 11-26: Capture Interrupt Clear Register (CAPIC) Field Description 365
Table 11-27: Capture Interrupt Force Register (CAPIFRC) Layout 366
Table 11-28: Capture Interrupt Force Register (CAPIFRC) Field Description 366
Table 11-29: Capture Register Write-Allow Key Register (CAPREGKEY) Layout 367
Table 11-30: Capture Register Write-Allow Key Register (CAPREGKEY) Filed Description 367
Table 12-1: Trigger source selection 374
Table 12-2: Sample mode description 375
Table 12-3: ADCSOCCTL[x] channel selection for sequential sampler sampling 375
Table 12-4: ADC channel selection 376
Table 12-5: Use SOC0/SOC1/SOC2 for 3 sampler simultaneous sampling 376
Table 12-6: Use SOC4/SOC5 for 2 sampler simultaneous sampling 376
Table 12-7: Averaging time selection 379
Table 12-8: Sampling time with different SAMPCNT and CONVCNT (Example) 379
Table 12-9: Simultaneous sampling mode control 384
Table 12-10: ADC Module Base Address 398
Table 12-11: ADC Register Map 398
Table 12-12: ADC Interrupt Flag Register (ADCIF) Layout 403
Table 12-13: ADC Interrupt Flag Register (ADCIF) Field Description 403
Table 12-14: ADC Interrupt Flag Clear Register (ADCIC) Layout 405
Table 12-15: ADC Interrupt Flag Clear Register (ADCIC) Field Description 405
Table 12-16: ADC Interrupt Overflow Flag Register (ADCIOVF) Layout 407
Table 12-17: ADC Interrupt Overflow Flag Register (ADCIOVF) Field Description 407
Table 12-18: ADC Interrupt Overflow Flag Clear Register (ADCIOVFC) Layout 409

SPINTROL

Table 12-19: ADC Interrupt Overflow Flag Clear Register (ADCIOVFC) Field Description 409
Table 12-20: ADC Interrupt Enable Register (ADCIE) Layout 411
Table 12-21: ADC Interrupt Enable Register (ADCIE) Field Description 411
Table 12-22: ADC Start of Conversion Priority Control Register (ADCSOCPRICTL) Layout 413
Table 12-23: ADC Start of Conversion Priority Control Register (ADCSOCPRICTL) Field Description 413
Table 12-24: ADC SOC Flag Register (ADCSOCFLG) Layout 415
Table 12-25: ADC SOC Flag Register (ADCSOCFLG) Field Description 415
Table 12-26: ADC SOC Force Register (ADCSOCFRC) Layout 417
Table 12-27: ADC SOC Force Register (ADCSOCFRC) Field Description 417
Table 12-28: ADC SOC Overflow Register (ADCSOCOVF) Layout 419
Table 12-29: ADC SOC Overflow Register (ADCSOCOVF) Field Description 419
Table 12-30: ADC SOC Overflow Clear Register (ADCSOCOVFC) Layout 421
Table 12-31: ADC SOC Overflow Clear Register (ADCSOCOVFC) Field Description 421
Table 12-32: ADC Interrupt Trigger SOC Enable Register (ADCINTSOCEN) Layout 423
Table 12-33: ADC Interrupt Trigger SOC Enable Register (ADCINTSOCEN) Field Description 423
Table 12-34: ADC Interrupt Trigger SOC Select Register 0 (ADCINTSOCSEL0) Layout 425
Table 12-35: ADC Interrupt Trigger SOC Select Register 0 (ADCINTSOCSEL0) Field Description 425
Table 12-36: ADC Interrupt Trigger SOC Select Register 1 (ADCINTSOCSEL1) Layout 426
Table 12-37: ADC Interrupt Trigger SOC Select Register 1 (ADCINTSOCSEL1) Field Description 426
Table 12-38: ADC External SOC Input Control Register (ADCEXTSOCCTL) Layout 427
Table 12-39: ADC External SOC Input Control Register (ADCEXTSOCCTL) Field Description 427
Table 12-40: ADC SOC0 Control Register (ADCSOCCTL0) Layout 428
Table 12-41: ADC SOC0 Control Register (ADCSOCCTL0) Field Description 428
Table 12-42: ADC SOC1 Control Register (ADCSOCCTL1) Layout 430
Table 12-43: ADC SOC1 Control Register (ADCSOCCTL1) Field Description 430
Table 12-44: ADC SOC2 Control Register (ADCSOCCTL2) Layout 432
Table 12-45: ADC SOC2 Control Register (ADCSOCCTL2) Field Description 432
Table 12-46: ADC SOC3 Control Register (ADCSOCCTL3) Layout 434
Table 12-47: ADC SOC3 Control Register (ADCSOCCTL3) Field Description 434
Table 12-48: ADC SOC4 Control Register (ADCSOCCTL4) Layout 436
Table 12-49: ADC SOC4 Control Register (ADCSOCCTL4) Field Description 436
Table 12-50: ADC SOC5 Control Register (ADCSOCCTL5) Layout 438
Table 12-51: ADC SOC5 Control Register (ADCSOCCTL5) Field Description 438
Table 12-52: ADC SOC6 Control Register (ADCSOCCTL6) Layout 440
Table 12-53: ADC SOC6 Control Register (ADCSOCCTL6) Field Description 440
Table 12-54: ADC SOC7 Control Register (ADCSOCCTL7) Layout 442
Table 12-55: ADC SOC7 Control Register (ADCSOCCTL7) Field Description 442
Table 12-56: ADC SOC8 Control Register (ADCSOCCTL8) Layout 444
Table 12-57: ADC SOC8 Control Register (ADCSOCCTL8) Field Description 444
Table 12-58: ADC SOC9 Control Register (ADCSOCCTL9) Layout 446
Table 12-59: ADC SOC9 Control Register (ADCSOCCTL9) Field Description 446
Table 12-60: ADC SOC10 Control Register (ADCSOCCTL10) Layout 448
Table 12-61: ADC SOC10 Control Register (ADCSOCCTL10) Field Description 448
Table 12-62: ADC SOC11 Control Register (ADCSOCCTL11) Layout 450
Table 12-63: ADC SOC11 Control Register (ADCSOCCTL11) Field Description 450
Table 12-64: ADC SOC12 Control Register (ADCSOCCTL12) Layout 452
Table 12-65: ADC SOC12 Control Register (ADCSOCCTL12) Field Description 452

SPINTROL

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Table 12-66: ADC SOC13 Control Register (ADCSOCCTL13) Layout 454
Table 12-67: ADC SOC13 Control Register (ADCSOCCTL13) Field Description 454
Table 12-68: ADC SOC14 Control Register (ADCSOCCTL14) Layout 456
Table 12-69: ADC SOC14 Control Register (ADCSOCCTL14) Field Description 456
Table 12-70: ADC SOC15 Control Register (ADCSOCCTL15) Layout 458
Table 12-71: ADC SOC15 Control Register (ADCSOCCTL15) Field Description 458
Table 12-72: ADC Offset Trim Register 0 (ADCOFFSET0) Layout 460
Table 12-73: ADC Offset Trim Register 0 (ADCOFFSET0) Field Description 460
Table 12-74: ADC Offset Trim Register 1 (ADCOFFSET1) Layout 460
Table 12-75: ADC Offset Trim Register 1 (ADCOFFSET1) Field Description 460
Table 12-76: ADC Offset Trim Register 2 (ADCOFFSET2) Layout 461
Table 12-77: ADC Offset Trim Register 2 (ADCOFFSET2) Field Description 461
Table 12-78: ADC Offset Trim Register 3 (ADCOFFSET3) Layout 461
Table 12-79: ADC Offset Trim Register 3 (ADCOFFSET3) Field Description 461
Table 12-80: ADC Offset Trim Register 4 (ADCOFFSET4) Layout 462
Table 12-81: ADC Offset Trim Register 4 (ADCOFFSET4) Field Description 462
Table 12-82: ADC Offset Trim Register 5 (ADCOFFSET5) Layout 462
Table 12-83: ADC Offset Trim Register 5 (ADCOFFSET5) Field Description 462
Table 12-84: ADC Offset Trim Register 6 (ADCOFFSET6) Layout 463
Table 12-85: ADC Offset Trim Register 6 (ADCOFFSET6) Field Description 463
Table 12-86: ADC Offset Trim Register 7 (ADCOFFSET7) Layout 463
Table 12-87: ADC Offset Trim Register 7 (ADCOFFSET7) Field Description 463
Table 12-88: ADC Offset Trim Register 8 (ADCOFFSET8) Layout 464
Table 12-89: ADC Offset Trim Register 8 (ADCOFFSET8) Field Description 464
Table 12-90: ADC Offset Trim Register 9 (ADCOFFSET9) Layout 464
Table 12-91: ADC Offset Trim Register 9 (ADCOFFSET9) Field Description 464
Table 12-92: ADC Offset Trim Register 10 (ADCOFFSET10) Layout 465
Table 12-93: ADC Offset Trim Register 10 (ADCOFFSET10) Field Description 465
Table 12-94: ADC Offset Trim Register 11 (ADCOFFSET11) Layout 465
Table 12-95: ADC Offset Trim Register 11 (ADCOFFSET11) Field Description 465
Table 12-96: ADC Offset Trim Register 12 (ADCOFFSET12) Layout 466
Table 12-97: ADC Offset Trim Register 12 (ADCOFFSET12) Field Description 466
Table 12-98: ADC Offset Trim Register 13 (ADCOFFSET13) Layout 466
Table 12-99: ADC Offset Trim Register 13 (ADCOFFSET13) Field Description 466
Table 12-100: ADC Offset Trim Register 14 (ADCOFFSET14) Layout 467
Table 12-101: ADC Offset Trim Register 14 (ADCOFFSET14) Field Description 467
Table 12-102: ADC Offset Trim Register 15 (ADCOFFSET15) Layout 467
Table 12-103: ADC Offset Trim Register 15 (ADCOFFSET15) Field Description 467
Table 12-104: ADC Gain Trim Register 0 (ADCGAIN0) Layout 468
Table 12-105: ADC Gain Trim Register 0 (ADCGAIN0) Field Description 468
Table 12-106: ADC Gain Trim Register 1 (ADCGAIN1) Layout 468
Table 12-107: ADC Gain Trim Register 1 (ADCGAIN1) Field Description 468
Table 12-108: ADC Gain Trim Register 2 (ADCGAIN2) Layout 469
Table 12-109: ADC Gain Trim Register 2 (ADCGAIN2) Field Description 469
Table 12-110: ADC Gain Trim Register 3 (ADCGAIN3) Layout 469
Table 12-111: ADC Gain Trim Register 3 (ADCGAIN3) Field Description 469
Table 12-112: ADC Gain Trim Register 4 (ADCGAIN4) Layout 470

SPINTROL

Table 12-113: ADC Gain Trim Register 4 (ADCGAIN4) Field Description 470
Table 12-114: ADC Gain Trim Register 5 (ADCGAIN5) Layout 470
Table 12-115: ADC Gain Trim Register 5 (ADCGAIN5) Field Description 470
Table 12-116: ADC Gain Trim Register 6 (ADCGAIN6) Layout 471
Table 12-117: ADC Gain Trim Register 6 (ADCGAIN6) Field Description 471
Table 12-118: ADC Gain Trim Register 7 (ADCGAIN7) Layout 471
Table 12-119: ADC Gain Trim Register 7 (ADCGAIN7) Field Description 471
Table 12-120: ADC Gain Trim Register 8 (ADCGAIN8) Layout 472
Table 12-121: ADC Gain Trim Register 8 (ADCGAIN8) Field Description 472
Table 12-122: ADC Gain Trim Register 9 (ADCGAIN9) Layout 472
Table 12-123: ADC Gain Trim Register 9 (ADCGAIN9) Field Description 472
Table 12-124: ADC Gain Trim Register 10 (ADCGAIN10) Layout 473
Table 12-125: ADC Gain Trim Register 10 (ADCGAIN10) Field Description 473
Table 12-126: ADC Gain Trim Register 11 (ADCGAIN11) Layout 473
Table 12-127: ADC Gain Trim Register 11 (ADCGAIN11) Field Description 473
Table 12-128: ADC Gain Trim Register 12 (ADCGAIN12) Layout 474
Table 12-129: ADC Gain Trim Register 12 (ADCGAIN12) Field Description 474
Table 12-130: ADC Gain Trim Register 13 (ADCGAIN13) Layout 474
Table 12-131: ADC Gain Trim Register 13 (ADCGAIN13) Field Description 474
Table 12-132: ADC Gain Trim Register 14 (ADCGAIN14) Layout 475
Table 12-133: ADC Gain Trim Register 14 (ADCGAIN14) Field Description 475
Table 12-134: ADC Gain Trim Register 15 (ADCGAIN15) Layout 475
Table 12-135: ADC Gain Trim Register 15 (ADCGAIN15) Field Description 475
Table 12-136: ADC SHA Offset Trim Register (ADCOFFSETA) Layout 476
Table 12-137: ADC SHA Offset Trim Register (ADCOFFSETA) Field Description 476
Table 12-138: ADC SHB Offset Trim Register (ADCOFFSETB) Layout 476
Table 12-139: ADC SHB Offset Trim Register (ADCOFFSETB) Field Description 476
Table 12-140: ADC SHC Offset Trim Register (ADCOFFSETC) Layout 477
Table 12-141: ADC SHC Offset Trim Register (ADCOFFSETC) Field Description 477
Table 12-142: ADC SHA Gain Trim Register (ADCGAINA) Layout 477
Table 12-143: ADC SHA Gain Trim Register (ADCGAINA) Field Description 477
Table 12-144: ADC SHB Gain Trim Register (ADCGAINB) Layout 478
Table 12-145: ADC SHB Gain Trim Register (ADCGAINB) Field Description 478
Table 12-146: ADC SHC Gain Trim Register (ADCGAINC) Layout 478
Table 12-147: ADC SHC Gain Trim Register (ADCGAINC) Field Description 478
Table 12-148: ADC Status Register (ADCSTS) Layout 479
Table 12-149: ADC Status Register (ADCSTS) Field Description 479
Table 12-150: ADC Status Clear Register (ADCSTSCLR) Layout 480
Table 12-151: ADC Status Clear Register (ADCSTSCLR) Field Description 480
Table 12-152: ADC Control Register (ADCCTL) Layout 481
Table 12-153: ADC Control Register (ADCCTL) Field Description 481
Table 12-154: ADC Bandgap Control Register (ADCBGCTL) Layout 482
Table 12-155: ADC Bandgap Control Register (ADCBGCTL) Field Description 482
Table 12-156: ADC Reference Control Register (ADCREFCTL) Layout 483
Table 12-157: ADC Reference Control Register (ADCREFCTL) Field Description 483
Table 12-158: ADC SHA Raw Code Register (ADCRAWCODEA) Layout 484
Table 12-159: ADC SHA Raw Code Register (ADCRAWCODEA) Field Description 484

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Table 12-160: ADC SHB Raw Code Register (ADCRAWCODEB) Layout 484
Table 12-161: ADC SHB Raw Code Register (ADCRAWCODEB) Field Description 484
Table 12-162: ADC SHC Raw Code Register (ADCRAWCODEC) Layout 485
Table 12-163: ADC SHC Raw Code Register (ADCRAWCODEC) Field Description 485
Table 12-164: ADC Result Register 0 (ADCRESULT0) Layout 485
Table 12-165: ADC Result Register 0 (ADCRESULT0) Field Description 485
Table 12-166: ADC Result Register 1 (ADCRESULT1) Layout 486
Table 12-167: ADC Result Register 1 (ADCRESULT1) Field Description 486
Table 12-168: ADC Result Register 2 (ADCRESULT2) Layout 486
Table 12-169: ADC Result Register 2 (ADCRESULT2) Field Description 486
Table 12-170: ADC Result Register 3 (ADCRESULT3) Layout 487
Table 12-171: ADC Result Register 3 (ADCRESULT3) Field Description 487
Table 12-172: ADC Result Register 4 (ADCRESULT4) Layout 487
Table 12-173: ADC Result Register 4 (ADCRESULT4) Field Description 487
Table 12-174: ADC Result Register 5 (ADCRESULT5) Layout 488
Table 12-175: ADC Result Register 5 (ADCRESULT5) Field Description 488
Table 12-176: ADC Result Register 6 (ADCRESULT6) Layout 488
Table 12-177: ADC Result Register 6 (ADCRESULT6) Field Description 488
Table 12-178: ADC Result Register 7 (ADCRESULT7) Layout 489
Table 12-179: ADC Result Register 7 (ADCRESULT7) Field Description 489
Table 12-180: ADC Result Register 8 (ADCRESULT8) Layout 489
Table 12-181: ADC Result Register 8 (ADCRESULT8) Field Description 489
Table 12-182: ADC Result Register 9 (ADCRESULT9) Layout 490
Table 12-183: ADC Result Register 9 (ADCRESULT9) Field Description 490
Table 12-184: ADC Result Register 10 (ADCRESULT10) Layout 490
Table 12-185: ADC Result Register 10 (ADCRESULT10) Field Description 490
Table 12-186: ADC Result Register 11 (ADCRESULT11) Layout 491
Table 12-187: ADC Result Register 11 (ADCRESULT11) Field Description 491
Table 12-188: ADC Result Register 12 (ADCRESULT12) Layout 491
Table 12-189: ADC Result Register 12 (ADCRESULT12) Field Description 491
Table 12-190: ADC Result Register 13 (ADCRESULT13) Layout 492
Table 12-191: ADC Result Register 13 (ADCRESULT13) Field Description 492
Table 12-192: ADC Result Register 14 (ADCRESULT14) Layout 492
Table 12-193: ADC Result Register 14 (ADCRESULT14) Field Description 492
Table 12-194: ADC Result Register 15 (ADCRESULT15) Layout 493
Table 12-195: ADC Result Register 15 (ADCRESULT15) Field Description 493
Table 12-196: ADCPPU0 Comparison Result Register (ADCPPURESULT0) Layout 493
Table 12-197: ADCPPU0 Comparison Result Register (ADCPPURESULT0) Field Description 493
Table 12-198: ADCPPU1 Comparison Result Register (ADCPPURESULT1) Layout 494
Table 12-199: ADCPPU1 Comparison Result Register (ADCPPURESULT1) Field Description 494
Table 12-200: ADCPPU2 Comparison Result Register (ADCPPURESULT2) Layout 494
Table 12-201: ADCPPU2 Comparison Result Register (ADCPPURESULT2) Field Description 494
Table 12-202: ADCPPU3 Comparison Result Register (ADCPPURESULT3) Layout 495
Table 12-203: ADCPPU3 Comparison Result Register (ADCPPURESULT3) Field Description 495
Table 12-204: ADCPPU4 Comparison Result Register (ADCPPURESULT4) Layout 495
Table 12-205: ADCPPU4 Comparison Result Register (ADCPPURESULT4) Field Description 495
Table 12-206: ADCPPU5 Comparison Result Register (ADCPPURESULT5) Layout 496

SPINTROL

Table 12-207: ADCPPU5 Comparison Result Register (ADCPPURESULT5) Field Description 496
Table 12-208: ADCPPU6 Comparison Result Register (ADCPPURESULT6) Layout 496
Table 12-209: ADCPPU6 Comparison Result Register (ADCPPURESULT6) Field Description 496
Table 12-210: ADCPPU7 Comparison Result Register (ADCPPURESULT7) Layout 497
Table 12-211: ADCPPU7 Comparison Result Register (ADCPPURESULT7) Field Description 497
Table 12-212: ADCPPU0 SOC Delay Register (ADCPPUSOCDLY0) Layout..... 497
Table 12-213: ADCPPU0 SOC Delay Register (ADCPPUSOCDLY0) Field Description 497
Table 12-214: ADCPPU1 SOC Delay Register (ADCPPUSOCDLY1) Layout..... 498
Table 12-215: ADCPPU1 SOC Delay Register (ADCPPUSOCDLY1) Field Description 498
Table 12-216: ADCPPU2 SOC Delay Register (ADCPPUSOCDLY2) Layout..... 498
Table 12-217: ADCPPU2 SOC Delay Register (ADCPPUSOCDLY2) Field Description 498
Table 12-218: ADCPPU3 SOC Delay Register (ADCPPUSOCDLY3) Layout..... 499
Table 12-219: ADCPPU3 SOC Delay Register (ADCPPUSOCDLY3) Field Description 499
Table 12-220: ADCPPU4 SOC Delay Register (ADCPPUSOCDLY4) Layout..... 499
Table 12-221: ADCPPU4 SOC Delay Register (ADCPPUSOCDLY4) Field Description 499
Table 12-222: ADCPPU5 SOC Delay Register (ADCPPUSOCDLY5) Layout..... 500
Table 12-223: ADCPPU5 SOC Delay Register (ADCPPUSOCDLY5) Field Description 500
Table 12-224: ADCPPU6 SOC Delay Register (ADCPPUSOCDLY6) Layout..... 500
Table 12-225: ADCPPU6 SOC Delay Register (ADCPPUSOCDLY6) Field Description 500
Table 12-226: ADCPPU7 SOC Delay Register (ADCPPUSOCDLY7) Layout..... 501
Table 12-227: ADCPPU7 SOC Delay Register (ADCPPUSOCDLY7) Field Description 501
Table 12-228: ADCPPU0 Interrupt Flag Register (ADCPPUIF0) Layout..... 502
Table 12-229: ADCPPU0 Interrupt Flag Register (ADCPPUIF0) Field Description..... 502
Table 12-230: ADCPPU1 Interrupt Flag Register (ADCPPUIF1) Layout..... 503
Table 12-231: ADCPPU1 Interrupt Flag Register (ADCPPUIF1) Field Description..... 503
Table 12-232: ADCPPU2 Interrupt Flag Register (ADCPPUIF2) Layout..... 504
Table 12-233: ADCPPU2 Interrupt Flag Register (ADCPPUIF2) Field Description..... 504
Table 12-234: ADCPPU3 Interrupt Flag Register (ADCPPUIF3) Layout..... 505
Table 12-235: ADCPPU3 Interrupt Flag Register (ADCPPUIF3) Field Description..... 505
Table 12-236: ADCPPU4 Interrupt Flag Register (ADCPPUIF4) Layout..... 506
Table 12-237: ADCPPU4 Interrupt Flag Register (ADCPPUIF4) Field Description..... 506
Table 12-238: ADCPPU5 Interrupt Flag Register (ADCPPUIF5) Layout..... 507
Table 12-239: ADCPPU5 Interrupt Flag Register (ADCPPUIF5) Field Description..... 507
Table 12-240: ADCPPU6 Interrupt Flag Register (ADCPPUIF6) Layout..... 508
Table 12-241: ADCPPU6 Interrupt Flag Register (ADCPPUIF6) Field Description..... 508
Table 12-242: ADCPPU7 Interrupt Flag Register (ADCPPUIF7) Layout..... 509
Table 12-243: ADCPPU7 Interrupt Flag Register (ADCPPUIF7) Field Description..... 509
Table 12-244: ADCPPU0 Interrupt Clear Register (ADCPPUIC0) Layout..... 510
Table 12-245: ADCPPU0 Interrupt Clear Register (ADCPPUIC0) Field Description 510
Table 12-246: ADCPPU1 Interrupt Clear Register (ADCPPUIC1) Layout..... 511
Table 12-247: ADCPPU1 Interrupt Clear Register (ADCPPUIC1) Field Description 511
Table 12-248: ADCPPU2 Interrupt Clear Register (ADCPPUIC2) Layout..... 512
Table 12-249: ADCPPU2 Interrupt Clear Register (ADCPPUIC2) Field Description 512
Table 12-250: ADCPPU3 Interrupt Clear Register (ADCPPUIC3) Layout..... 513
Table 12-251: ADCPPU3 Interrupt Clear Register (ADCPPUIC3) Field Description 513
Table 12-252: ADCPPU4 Interrupt Clear Register (ADCPPUIC4) Layout..... 514
Table 12-253: ADCPPU4 Interrupt Clear Register (ADCPPUIC4) Field Description 514

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Table 12-254: ADCPPU5 Interrupt Clear Register (ADCPPUIC5) Layout 515
Table 12-255: ADCPPU5 Interrupt Clear Register (ADCPPUIC5) Field Description 515
Table 12-256: ADCPPU6 Interrupt Clear Register (ADCPPUIC6) Layout 516
Table 12-257: ADCPPU6 Interrupt Clear Register (ADCPPUIC6) Field Description 516
Table 12-258: ADCPPU7 Interrupt Clear Register (ADCPPUIC7) Layout 517
Table 12-259: ADCPPU7 Interrupt Clear Register (ADCPPUIC7) Field Description 517
Table 12-260: ADCPPU0 Interrupt Enable Register (ADCPPUIE0) Layout 518
Table 12-261: ADCPPU0 Interrupt Enable Register (ADCPPUIE0) Field Description 518
Table 12-262: ADCPPU1 Interrupt Enable Register (ADCPPUIE1) Layout 519
Table 12-263: ADCPPU1 Interrupt Enable Register (ADCPPUIE1) Field Description 519
Table 12-264: ADCPPU2 Interrupt Enable Register (ADCPPUIE2) Layout 520
Table 12-265: ADCPPU2 Interrupt Enable Register (ADCPPUIE2) Field Description 520
Table 12-266: ADCPPU3 Interrupt Enable Register (ADCPPUIE3) Layout 521
Table 12-267: ADCPPU3 Interrupt Enable Register (ADCPPUIE3) Field Description 521
Table 12-268: ADCPPU4 Interrupt Enable Register (ADCPPUIE4) Layout 522
Table 12-269: ADCPPU4 Interrupt Enable Register (ADCPPUIE4) Field Description 522
Table 12-270: ADCPPU5 Interrupt Enable Register (ADCPPUIE5) Layout 523
Table 12-271: ADCPPU5 Interrupt Enable Register (ADCPPUIE5) Field Description 523
Table 12-272: ADCPPU6 Interrupt Enable Register (ADCPPUIE6) Layout 524
Table 12-273: ADCPPU6 Interrupt Enable Register (ADCPPUIE6) Field Description 524
Table 12-274: ADCPPU7 Interrupt Enable Register (ADCPPUIE7) Layout 525
Table 12-275: ADCPPU7 Interrupt Enable Register (ADCPPUIE7) Field Description 525
Table 12-276: ADCPPU0 Trip-Zone Event Enable Register (ADCPPUTZE0) Layout 526
Table 12-277: ADCPPU0 Trip-Zone Event Enable Register (ADCPPUTZE0) Field Description 526
Table 12-278: ADCPPU1 Trip-Zone Event Enable Register (ADCPPUTZE1) Layout 527
Table 12-279: ADCPPU1 Trip-Zone Event Enable Register (ADCPPUTZE1) Field Description 527
Table 12-280: ADCPPU2 Trip-Zone Event Enable Register (ADCPPUTZE2) Layout 528
Table 12-281: ADCPPU2 Trip-Zone Event Enable Register (ADCPPUTZE2) Field Description 528
Table 12-282: ADCPPU3 Trip-Zone Event Enable Register (ADCPPUTZE3) Layout 529
Table 12-283: ADCPPU3 Trip-Zone Event Enable Register (ADCPPUTZE3) Field Description 529
Table 12-284: ADCPPU4 Trip-Zone Event Enable Register (ADCPPUTZE4) Layout 530
Table 12-285: ADCPPU4 Trip-Zone Event Enable Register (ADCPPUTZE4) Field Description 530
Table 12-286: ADCPPU5 Trip-Zone Event Enable Register (ADCPPUTZE5) Layout 531
Table 12-287: ADCPPU5 Trip-Zone Event Enable Register (ADCPPUTZE5) Field Description 531
Table 12-288: ADCPPU6 Trip-Zone Event Enable Register (ADCPPUTZE6) Layout 532
Table 12-289: ADCPPU6 Trip-Zone Event Enable Register (ADCPPUTZE6) Field Description 532
Table 12-290: ADCPPU7 Trip-Zone Event Enable Register (ADCPPUTZE7) Layout 533
Table 12-291: ADCPPU7 Trip-Zone Event Enable Register (ADCPPUTZE7) Field Description 533
Table 12-292: ADCPPU0 Control Register (ADCPPUCTL0) Layout 534
Table 12-293: ADCPPU0 Control Register (ADCPPUCTL0) Field Description 534
Table 12-294: ADCPPU1 Control Register (ADCPPUCTL1) Layout 535
Table 12-295: ADCPPU1 Control Register (ADCPPUCTL1) Field Description 535
Table 12-296: ADCPPU2 Control Register (ADCPPUCTL2) Layout 536
Table 12-297: ADCPPU2 Control Register (ADCPPUCTL2) Field Description 536
Table 12-298: ADCPPU3 Control Register (ADCPPUCTL3) Layout 537
Table 12-299: ADCPPU3 Control Register (ADCPPUCTL3) Field Description 537
Table 12-300: ADCPPU4 Control Register (ADCPPUCTL4) Layout 538

SPINTROL

Table 12-301: ADCPPU4 Control Register (ADCPPUCTL4) Field Description 538
Table 12-302: ADCPPU5 Control Register (ADCPPUCTL5) Layout 539
Table 12-303: ADCPPU5 Control Register (ADCPPUCTL5) Field Description 539
Table 12-304: ADCPPU6 Control Register (ADCPPUCTL6) Layout 540
Table 12-305: ADCPPU6 Control Register (ADCPPUCTL6) Field Description 540
Table 12-306: ADCPPU7 Control Register (ADCPPUCTL7) Layout 541
Table 12-307: ADCPPU7 Control Register (ADCPPUCTL7) Field Description 541
Table 12-308: ADCPPU0 Reference Register (ADCPPUREF0) Layout 542
Table 12-309: ADCPPU0 Reference Register (ADCPPUREF0) Field Description 542
Table 12-310: ADCPPU1 Reference Register (ADCPPUREF1) Layout 542
Table 12-311: ADCPPU1 Reference Register (ADCPPUREF1) Field Description 542
Table 12-312: ADCPPU2 Reference Register (ADCPPUREF2) Layout 543
Table 12-313: ADCPPU2 Reference Register (ADCPPUREF2) Field Description 543
Table 12-314: ADCPPU3 Reference Register (ADCPPUREF3) Layout 543
Table 12-315: ADCPPU3 Reference Register (ADCPPUREF3) Field Description 543
Table 12-316: ADCPPU4 Reference Register (ADCPPUREF4) Layout 544
Table 12-317: ADCPPU4 Reference Register (ADCPPUREF4) Field Description 544
Table 12-318: ADCPPU5 Reference Register (ADCPPUREF5) Layout 544
Table 12-319: ADCPPU5 Reference Register (ADCPPUREF5) Field Description 544
Table 12-320: ADCPPU6 Reference Register (ADCPPUREF6) Layout 545
Table 12-321: ADCPPU6 Reference Register (ADCPPUREF6) Field Description 545
Table 12-322: ADCPPU7 Reference Register (ADCPPUREF7) Layout 545
Table 12-323: ADCPPU7 Reference Register (ADCPPUREF7) Field Description 545
Table 12-324: ADCPPU0 Trip-Zone High-Side Threshold Register (ADCPPUTHH0) Layout 546
Table 12-325: ADCPPU0 Trip-Zone High-Side Threshold Register (ADCPPUTHH0) Field Description 546
Table 12-326: ADCPPU1 Trip-Zone High-Side Threshold Register (ADCPPUTHH1) Layout 546
Table 12-327: ADCPPU1 Trip-Zone High-Side Threshold Register (ADCPPUTHH1) Field Description 546
Table 12-328: ADCPPU2 Trip-Zone High-Side Threshold Register (ADCPPUTHH2) Layout 547
Table 12-329: ADCPPU2 Trip-Zone High-Side Threshold Register (ADCPPUTHH2) Field Description 547
Table 12-330: ADCPPU3 Trip-Zone High-Side Threshold Register (ADCPPUTHH3) Layout 547
Table 12-331: ADCPPU3 Trip-Zone High-Side Threshold Register (ADCPPUTHH3) Field Description 547
Table 12-332: ADCPPU4 Trip-Zone High-Side Threshold Register (ADCPPUTHH4) Layout 548
Table 12-333: ADCPPU4 Trip-Zone High-Side Threshold Register (ADCPPUTHH4) Field Description 548
Table 12-334: ADCPPU5 Trip-Zone High-Side Threshold Register (ADCPPUTHH5) Layout 548
Table 12-335: ADCPPU5 Trip-Zone High-Side Threshold Register (ADCPPUTHH5) Field Description 548
Table 12-336: ADCPPU6 Trip-Zone High-Side Threshold Register (ADCPPUTHH6) Layout 549
Table 12-337: ADCPPU6 Trip-Zone High-Side Threshold Register (ADCPPUTHH6) Field Description 549
Table 12-338: ADCPPU7 Trip-Zone High-Side Threshold Register (ADCPPUTHH7) Layout 549
Table 12-339: ADCPPU7 Trip-Zone High-Side Threshold Register (ADCPPUTHH7) Field Description 549
Table 12-340: ADCPPU0 Trip-Zone Low-Side Threshold Register (ADCPPUTHL0) Layout 550
Table 12-341: ADCPPU0 Trip-Zone Low-Side Threshold Register (ADCPPUTHL0) Field Description 550
Table 12-342: ADCPPU1 Trip-Zone Low-Side Threshold Register (ADCPPUTHL1) Layout 550
Table 12-343: ADCPPU1 Trip-Zone Low-Side Threshold Register (ADCPPUTHL1) Field Description 550
Table 12-344: ADCPPU2 Trip-Zone Low-Side Threshold Register (ADCPPUTHL2) Layout 551
Table 12-345: ADCPPU2 Trip-Zone Low-Side Threshold Register (ADCPPUTHL2) Field Description 551
Table 12-346: ADCPPU3 Trip-Zone Low-Side Threshold Register (ADCPPUTHL3) Layout 551
Table 12-347: ADCPPU3 Trip-Zone Low-Side Threshold Register (ADCPPUTHL3) Field Description 551

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Table 12-348: ADCPPU4 Trip-Zone Low-Side Threshold Register (ADCPPUTHL4) Layout 552
Table 12-349: ADCPPU4 Trip-Zone Low-Side Threshold Register (ADCPPUTHL4) Field Description 552
Table 12-350: ADCPPU5 Trip-Zone Low-Side Threshold Register (ADCPPUTHL5) Layout 552
Table 12-351: ADCPPU5 Trip-Zone Low-Side Threshold Register (ADCPPUTHL5) Field Description 552
Table 12-352: ADCPPU6 Trip-Zone Low-Side Threshold Register (ADCPPUTHL6) Layout 553
Table 12-353: ADCPPU6 Trip-Zone Low-Side Threshold Register (ADCPPUTHL6) Field Description 553
Table 12-354: ADCPPU7 Trip-Zone Low-Side Threshold Register (ADCPPUTHL7) Layout 553
Table 12-355: ADCPPU7 Trip-Zone Low-Side Threshold Register (ADCPPUTHL7) Field Description 553
Table 12-356: Temperature Sensor Control Register (TSENSCTL) Layout 554
Table 12-357: Temperature Sensor Control Register (TSENSCTL) Field Description 554
Table 12-358: ADC Register Write-Allow Key Register (ADCREGKEY) Layout 554
Table 12-359: ADC Register Write-Allow Key Register (ADCREGKEY) Field Description 554
Table 13-1: MUX selection for PGA0/1/2 557
Table 13-2: MUX selection for PGA3/4/5 557
Table 13-3: PGA mode selection 558
Table 13-4: PGA gain selection 558
Table 13-5: PGA input range in different gain for single-ended mode 559
Table 13-6: PGA Module Base Address 567
Table 13-7: PGA Register Map 567
Table 13-8: PGA0 Control Register (PGA0CTL) Layout 568
Table 13-9: PGA0 Control Register (PGA0CTL) Field Description 568
Table 13-10: PGA1 Control Register (PGA1CTL) Layout 570
Table 13-11: PGA1 Control Register (PGA1CTL) Field Description 570
Table 13-12: PGA2 Control Register (PGA2CTL) Layout 572
Table 13-13: PGA2 Control Register (PGA2CTL) Field Description 572
Table 13-14: PGA3 Control Register (PGA3CTL) Layout 574
Table 13-15: PGA3 Control Register (PGA3CTL) Field Description 574
Table 13-16: PGA4 Control Register (PGA4CTL) Layout 576
Table 13-17: PGA4 Control Register (PGA4CTL) Field Description 576
Table 13-18: PGA5 Control Register (PGA5CTL) Layout 578
Table 13-19: PGA5 Control Register (PGA5CTL) Field Description 578
Table 13-20: PGA Register Write-Allow Key Register (PGAREGKEY) Layout 580
Table 13-21: PGA Register Write-Allow Key Register (PGAREGKEY) Field Description 580
Table 14-1: Comparator MUX selection 582
Table 14-2: Comparator Module Base Address 585
Table 14-3: Comparator Register Map 585
Table 14-4: Comparator Filter Output Register (COMPFLTOUT) Layout 587
Table 14-5: Comparator Filter Output Register (COMPFLTOUT) Field Description 587
Table 14-6: Comparator Status Register (COMPSTS) Layout 589
Table 14-7: Comparator Status Register (COMPSTS) Field Description 589
Table 14-8: Comparator Status Clear Register (COMPSTSCLR) Layout 591
Table 14-9: Comparator Status Clear Register (COMPSTSCLR) Field Description 591
Table 14-10: Comparator 0 Control Register (COMP0CTL) Layout 593
Table 14-11: Comparator 0 Control Register (COMP0CTL) Field Description 593
Table 14-12: COMP0L Control Register (COMP0LCTL) Layout 595
Table 14-13: COMP0L Control Register (COMP0LCTL) Field Description 595
Table 14-14: COMP0H Control Register (COMP0HCTL) Layout 597

SPINTROL

Table 14-15: COMP0H Control Register (COMP0HCTL) Field Description 597
Table 14-16: Comparator 1 Control Register (COMP1CTL) Layout..... 599
Table 14-17: Comparator 1 Control Register (COMP1CTL) Field Description 599
Table 14-18: COMP1L Control Register (COMP1LCTL) Layout 601
Table 14-19: COMP1L Control Register (COMP1LCTL) Field Description 601
Table 14-20: COMP1H Control Register (COMP1HCTL) Layout..... 603
Table 14-21: COMP1H Control Register (COMP1HCTL) Field Description 603
Table 14-22: Comparator 2 Control Register (COMP2CTL) Layout..... 605
Table 14-23: Comparator 2 Control Register (COMP2CTL) Field Description 605
Table 14-24: COMP2L Control Register (COMP2LCTL) Layout 607
Table 14-25: COMP2L Control Register (COMP2LCTL) Field Description 607
Table 14-26: COMP2H Control Register (COMP2HCTL) Layout..... 609
Table 14-27: COMP2H Control Register (COMP2HCTL) Field Description 609
Table 14-28: Comparator 3 Control Register (COMP3CTL) Layout..... 611
Table 14-29: Comparator 3 Control Register (COMP3CTL) Field Description 611
Table 14-30: COMP3L Control Register (COMP3LCTL) Layout 613
Table 14-31: COMP3L Control Register (COMP3LCTL) Field Description 613
Table 14-32: COMP3H Control Register (COMP3HCTL) Layout..... 615
Table 14-33: COMP3H Control Register (COMP3HCTL) Field Description 615
Table 14-34: Comparator 4 Control Register (COMP4CTL) Layout..... 617
Table 14-35: Comparator 4 Control Register (COMP4CTL) Field Description 617
Table 14-36: COMP4L Control Register (COMP4LCTL) Layout 619
Table 14-37: COMP4L Control Register (COMP4LCTL) Field Description 619
Table 14-38: COMP4H Control Register (COMP4HCTL) Layout..... 621
Table 14-39: COMP4H Control Register (COMP4HCTL) Field Description 621
Table 14-40: Comparator 5 Control Register (COMP5CTL) Layout..... 623
Table 14-41: Comparator 5 Control Register (COMP5CTL) Field Description 623
Table 14-42: COMP5L Control Register (COMP5LCTL) Layout 625
Table 14-43: COMP5L Control Register (COMP5LCTL) Field Description 625
Table 14-44: COMP5H Control Register (COMP5HCTL) Layout..... 627
Table 14-45: COMP5H Control Register (COMP5HCTL) Field Description 627
Table 14-46: Comparator 6 Control Register (COMP6CTL) Layout..... 629
Table 14-47: Comparator 6 Control Register (COMP6CTL) Field Description 629
Table 14-48: COMP6L Control Register (COMP6LCTL) Layout 631
Table 14-49: COMP6L Control Register (COMP6LCTL) Field Description 631
Table 14-50: COMP6H Control Register (COMP6HCTL) Layout..... 633
Table 14-51: COMP6H Control Register (COMP6HCTL) Field Description 633
Table 14-52: Comparator 7 Control Register (COMP7CTL) Layout..... 635
Table 14-53: Comparator 7 Control Register (COMP7CTL) Field Description 635
Table 14-54: COMP7L Control Register (COMP7LCTL) Layout 637
Table 14-55: COMP7L Control Register (COMP7LCTL) Field Description 637
Table 14-56: COMP7H Control Register (COMP7HCTL) Layout..... 639
Table 14-57: COMP7H Control Register (COMP7HCTL) Field Description 639
Table 14-58: DAC0 Control Register (DAC0CTL) Layout 641
Table 14-59: DAC0 Control Register (DAC0CTL) Field Description 641
Table 14-60: DAC0 Code Register (DAC0CODE) Layout..... 642
Table 14-61: DAC0 Code Register (DAC0CODE) Field Description..... 642

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Table 14-62: DAC0 Active Code Register (DAC0CODEA) Layout 643
Table 14-63: DAC0 Active Code Register (DAC0CODEA) Field Description 643
Table 14-64: RAMP0 Delay Shadow Register (RAMP0DLY) Layout 643
Table 14-65: RAMP0 Delay Shadow Register (RAMP0DLY) Field Description 643
Table 14-66: RAMP0 Delay Active Register (RAMP0DLYA) Layout 644
Table 14-67: RAMP0 Delay Active Register (RAMP0DLYA) Field Description 644
Table 14-68: RAMP0 Decrement Shadow Register (RAMP0DEC) Layout 644
Table 14-69: RAMP0 Decrement Shadow Register (RAMP0DEC) Field Description 644
Table 14-70: RAMP0 Decrement Active Register (RAMP0DECA) Layout 645
Table 14-71: RAMP0 Decrement Active Register (RAMP0DECA) Field Description 645
Table 14-72: RAMP0 Maximum Value Shadow Register (RAMP0MAX) Layout 645
Table 14-73: RAMP0 Maximum Value Shadow Register (RAMP0MAX) Field Description 645
Table 14-74: RAMP0 Maximum Value Active Register (RAMP0MAXA) Layout 646
Table 14-75: RAMP0 Maximum Value Active Register (RAMP0MAXA) Field Description 646
Table 14-76: RAMP0 Count Register (RAMP0CNT) Layout 646
Table 14-77: RAMP0 Count Register (RAMP0CNT) Field Description 646
Table 14-78: DAC1 Control Register (DAC1CTL) Layout 647
Table 14-79: DAC1 Control Register (DAC1CTL) Field Description 647
Table 14-80: DAC1 Code Register (DAC1CODE) Layout 648
Table 14-81: DAC1 Code Register (DAC1CODE) Field Description 648
Table 14-82: DAC1 Active Code Register (DAC1CODEA) Layout 649
Table 14-83: DAC1 Active Code Register (DAC1CODEA) Field Description 649
Table 14-84: RAMP1 Delay Shadow Register (RAMP1DLY) Layout 649
Table 14-85: RAMP1 Delay Shadow Register (RAMP1DLY) Field Description 649
Table 14-86: RAMP1 Delay Active Register (RAMP1DLYA) Layout 650
Table 14-87: RAMP1 Delay Active Register (RAMP1DLYA) Field Description 650
Table 14-88: RAMP1 Decrement Shadow Register (RAMP1DEC) Layout 650
Table 14-89: RAMP1 Decrement Shadow Register (RAMP1DEC) Field Description 650
Table 14-90: RAMP1 Decrement Active Register (RAMP1DECA) Layout 651
Table 14-91: RAMP1 Decrement Active Register (RAMP1DECA) Field Description 651
Table 14-92: RAMP1 Maximum Value Shadow Register (RAMP1MAX) Layout 651
Table 14-93: RAMP1 Maximum Value Shadow Register (RAMP1MAX) Field Description 651
Table 14-94: RAMP1 Maximum Value Active Register (RAMP1MAXA) Layout 652
Table 14-95: RAMP1 Maximum Value Active Register (RAMP1MAXA) Field Description 652
Table 14-96: RAMP1 Count Register (RAMP1CNT) Layout 652
Table 14-97: RAMP1 Count Register (RAMP1CNT) Field Description 652
Table 14-98: DAC2 Control Register (DAC2CTL) Layout 653
Table 14-99: DAC2 Control Register (DAC2CTL) Field Description 653
Table 14-100: DAC2 Code Register (DAC2CODE) Layout 654
Table 14-101: DAC2 Code Register (DAC2CODE) Field Description 654
Table 14-102: DAC2 Active Code Register (DAC2CODEA) Layout 654
Table 14-103: DAC2 Active Code Register (DAC2CODEA) Field Description 654
Table 14-104: DAC3 Control Register (DAC3CTL) Layout 655
Table 14-105: DAC3 Control Register (DAC3CTL) Field Description 655
Table 14-106: DAC3 Code Register (DAC3CODE) Layout 656
Table 14-107: DAC3 Code Register (DAC3CODE) Field Description 656
Table 14-108: DAC3 Active Code Register (DAC3CODEA) Layout 656

SPINTROL

Table 14-109: DAC3 Active Code Register (DAC3CODEA) Field Description 656
Table 14-110: DAC4 Control Register (DAC4CTL) Layout 657
Table 14-111: DAC4 Control Register (DAC4CTL) Field Description 657
Table 14-112: DAC4 Code Register (DAC4CODE) Layout 658
Table 14-113: DAC4 Code Register (DAC4CODE) Field Description 658
Table 14-114: DAC4 Active Code Register (DAC4CODEA) Layout 658
Table 14-115: DAC4 Active Code Register (DAC4CODEA) Field Description 658
Table 14-116: DAC5 Control Register (DAC5CTL) Layout 659
Table 14-117: DAC5 Control Register (DAC5CTL) Field Description 659
Table 14-118: DAC5 Code Register (DAC5CODE) Layout 660
Table 14-119: DAC5 Code Register (DAC5CODE) Field Description 660
Table 14-120: DAC5 Active Code Register (DAC5CODEA) Layout 660
Table 14-121: DAC5 Active Code Register (DAC5CODEA) Field Description 660
Table 14-122: DAC Buffer 0 Control Register (DACBUF0CTL) Layout 661
Table 14-123: DAC Buffer 0 Control Register (DACBUF0CTL) Field Description 661
Table 14-124: DAC Buffer 1 Control Register (DACBUF1CTL) Layout 662
Table 14-125: DAC Buffer 1 Control Register (DACBUF1CTL) Field Description 662
Table 14-126: COMP Register Write-Allow Key Register (COMPREGKEY) Layout 663
Table 14-127: COMP Register Write-Allow Key Register (COMPREGKEY) Field Description 663
Table 15-1: DAC buffer MUX 664
Table 17-1: UART signal descriptions 672
Table 17-2: Recommended baud rates 677
Table 17-3: UART Module Base Address 679
Table 17-4: UART Register Map 679
Table 17-5: UART Receive Buffer Register (UARTRBR) Layout 680
Table 17-6: UART Receive Buffer Register (UARTRBR) Field Description 680
Table 17-7: UART Transmit Holding Register (UARTTHR) Layout 681
Table 17-8: UART Transmit Holding Register (UARTTHR) Field Description 681
Table 17-9: UART Divisor Latch Low Byte Register (UARTDLL) Layout 681
Table 17-10: UART Divisor Latch Low Byte Register (UARTDLL) Field Description 681
Table 17-11: UART Divisor Latch High Byte Register (UARTDLH) Layout 682
Table 17-12: UART Divisor Latch High Byte Register (UARTDLH) Field Description 682
Table 17-13: UART Interrupt Enable Register (UARTIER) Layout 683
Table 17-14: UART Interrupt Enable Register (UARTIER) Field Description 683
Table 17-15: UART Interrupt Identification Register (UARTIIR) Layout 685
Table 17-16: UART Interrupt Identification Register (UARTIIR) Field Description 685
Table 17-17: UART FIFO Control Register (UARTFCR) Layout 686
Table 17-18: UART FIFO Control Register (UARTFCR) Field Description 686
Table 17-19: UART Line Control Register (UARTLCR) Layout 688
Table 17-20: UART Line Control Register (UARTLCR) Field Description 688
Table 17-21: UART Modem Control Register (UARTMCR) Layout 689
Table 17-22: UART Modem Control Register (UARTMCR) Field Description 689
Table 17-23: UART Line Status Register (UARTLSR) Layout 690
Table 17-24: UART Line Status Register (UARTLSR) Field Description 690
Table 17-25: UART Infrared Selection Register (UARTISR) Layout 693
Table 17-26: UART Infrared Selection Register (UARTISR) Field Description 693
Table 17-27: UART Receive FIFO Occupancy Register (UARTFOR) Layout 694

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Table 17-28: UART Receive FIFO Occupancy Register (UARTFOR) Field Description 694
Table 17-29: UART Auto-Baud Control Register (UARTABR) Layout 694
Table 17-30: UART Auto-Baud Control Register (UARTABR) Field Description 694
Table 17-31: UART Auto-Baud Count Register (UARTACR) Layout 695
Table 17-32: UART Auto-Baud Count Register (UARTACR) Field Description 695
Table 18-1: I2C signal description 696
Table 18-2: I2C Module Base Address 701
Table 18-3: I2C Register Map 701
Table 18-4: I2C Control Register (I2CCTL) Layout 703
Table 18-5: I2C Control Register (I2CCTL) Field Description 703
Table 18-6: I2C Master Address Register (I2CMASTERADDR) Layout 705
Table 18-7: I2C Master Address Register (I2CMASTERADDR) Field Description 705
Table 18-8: I2C Slave Address Register (I2CSLVADDR) Layout 706
Table 18-9: I2C Slave Address Register (I2CSLVADDR) Field Description 706
Table 18-10: I2C High Speed Master Mode Code Register (I2CHSMADDR) Layout 707
Table 18-11: I2C High Speed Master Mode Code Register (I2CHSMADDR) Field Description 707
Table 18-12: I2C Data Buffer and Command Register (I2CDATACMD) Layout 708
Table 18-13: I2C Data Buffer and Command Register (I2CDATACMD) Field Description 708
Table 18-14: Standard Speed I2C Clock SCL High Count Register (I2CSSHCNT) Layout 709
Table 18-15: Standard Speed I2C Clock SCL High Count Register (I2CSSHCNT) Field Description 709
Table 18-16: Standard Speed I2C Clock SCL Low Count Register (I2CSSLCNT) Layout 710
Table 18-17: Standard Speed I2C Clock SCL Low Count Register (I2CSSLCNT) Field Description 710
Table 18-18: Fast Speed I2C Clock SCL High Count Register (I2CFSHCNT) Layout 711
Table 18-19: Fast Speed I2C Clock SCL High Count Register (I2CFSHCNT) Field Description 711
Table 18-20: Fast Speed I2C Clock SCL Low Count Register (I2CFSLCNT) Layout 711
Table 18-21: Fast Speed I2C Clock SCL Low Count Register (I2CFSLCNT) Field Description 711
Table 18-22: High Speed I2C Clock SCL High Count Register (I2CHSHCNT) Layout 712
Table 18-23: High Speed I2C Clock SCL High Count Register (I2CHSHCNT) Field Description 712
Table 18-24: High Speed I2C Clock SCL Low Count Register (I2CHSLCNT) Layout 712
Table 18-25: High Speed I2C Clock SCL Low Count Register (I2CHSLCNT) Field Description 712
Table 18-26: I2C Interrupt Flag Register (I2CIF) Layout 713
Table 18-27: I2C Interrupt Flag Register (I2CIF) Field Description 713
Table 18-28: I2C Interrupt Enable Register (I2CIE) Layout 715
Table 18-29: I2C Interrupt Enable Register (I2CIE) Field Description 715
Table 18-30: I2C Raw Interrupt Flag Register (I2CRAWIF) Layout 717
Table 18-31: I2C Raw Interrupt Flag Register (I2CRAWIF) Field Description 717
Table 18-32: I2C Receive FIFO Threshold Register (I2CRXTH) Layout 719
Table 18-33: I2C Receive FIFO Threshold Register (I2CRXTH) Field Description 719
Table 18-34: I2Ctransmit FIFO Threshold Register (I2CTXTH) Layout 720
Table 18-35: I2Ctransmit FIFO Threshold Register (I2CTXTH) Field Description 720
Table 18-36: Clear Combined and Individual Interrupt Register (I2CINTCLR) Layout 721
Table 18-37: Clear Combined and Individual Interrupt Register (I2CINTCLR) Field Description 721
Table 18-38: Clear RXUDF Interrupt Register (I2CRXUDFCLR) Layout 721
Table 18-39: Clear RXUDF Interrupt Register (I2CRXUDFCLR) Field Description 721
Table 18-40: Clear RXOVF Interrupt Register (I2CRXOVFCLR) Layout 722
Table 18-41: Clear RXOVF Interrupt Register (I2CRXOVFCLR) Field Description 722
Table 18-42: Clear TXOVF Interrupt Register (I2CTXOVFCLR) Layout 722

SPINTROL

Table 18-43: Clear TXOVF Interrupt Register (I2CTXOVFCLR) Field Description 722
Table 18-44: Clear RDREQ Interrupt Register (I2CRDREQCLR) Layout 723
Table 18-45: Clear RDREQ Interrupt Register (I2CRDREQCLR) Field Description 723
Table 18-46: Clear TXABRT Interrupt Register (I2CTXABRTCLR) Layout 723
Table 18-47: Clear TXABRT Interrupt Register (I2CTXABRTCLR) Field Description 723
Table 18-48: Clear RXDONE Interrupt Register (I2CRXDONECLR) Layout 724
Table 18-49: Clear RXDONE Interrupt Register (I2CRXDONECLR) Field Description 724
Table 18-50: Clear ACT Interrupt Register (I2CACTCLR) Layout 724
Table 18-51: Clear ACT Interrupt Register (I2CACTCLR) Field Description 724
Table 18-52: Clear STOPDET Interrupt Register (I2CSTOPDETCLR) Layout 725
Table 18-53: Clear STOPDET Interrupt Register (I2CSTOPDETCLR) Field Description 725
Table 18-54: Clear STARTDET Interrupt Register (I2CSTARTDETCLR) Layout 725
Table 18-55: Clear STARTDET Interrupt Register (I2CSTARTDETCLR) Field Description 725
Table 18-56: Clear GENCALL Interrupt Register (I2CGENCALLCLR) Layout 726
Table 18-57: Clear GENCALL Interrupt Register (I2CGENCALLCLR) Field Description 726
Table 18-58: I2C Enable Register (I2CENABLE) Layout 727
Table 18-59: I2C Enable Register (I2CENABLE) Field Description 727
Table 18-60: I2C Status Register (I2CSTS) Layout 728
Table 18-61: I2C Status Register (I2CSTS) Field Description 728
Table 18-62: I2C Transmit FIFO Level Register (I2CTFLVL) Layout 729
Table 18-63: I2C Transmit FIFO Level Register (I2CTFLVL) Field Description 729
Table 18-64: I2C Receive FIFO Level Register (I2CRFLVL) Layout 729
Table 18-65: I2C Receive FIFO Level Register (I2CRFLVL) Field Description 729
Table 18-66: I2C SDA Hold-Time Register (I2CSDAHOLD) Layout 730
Table 18-67: I2C SDA Hold-Time Register (I2CSDAHOLD) Field Description 730
Table 18-68: I2C Transmit Abort Source Register (I2CTXABRTSRC) Layout 731
Table 18-69: I2C Transmit Abort Source Register (I2CTXABRTSRC) Field Description 731
Table 18-70: I2C SDA Setup Register (I2CSDASETUP) Layout 733
Table 18-71: I2C SDA Setup Register (I2CSDASETUP) Field Description 733
Table 18-72: I2C ACK General Call Register (I2CACKGC) Layout 734
Table 18-73: I2C ACK General Call Register (I2CACKGC) Field Description 734
Table 18-74: I2C Enable Status Register (I2CENSTS) Layout 735
Table 18-75: I2C Enable Status Register (I2CENSTS) Field Description 735
Table 18-76: I2C Fast Speed Spike Suppresion Limit Register (I2CFSSPKLEN) Layout 736
Table 18-77: I2C Fast Speed Spike Suppresion Limit Register (I2CFSSPKLEN) Field Description 736
Table 18-78: I2C High Speed Spike Suppresion Limit Register (I2CHSSPKLEN) Layout 737
Table 18-79: I2C High Speed Spike Suppresion Limit Register (I2CHSSPKLEN) Field Description 737
Table 19-1: SSP signal description 739
Table 19-2: SSP Module Base Address 746
Table 19-3: SSP Register Map 746
Table 19-4: SSP Control Register 0 (SSPCTL0) Layout 747
Table 19-5: SSP Control Register 0 (SSPCTL0) Field Description 747
Table 19-6: SSP Control Register 1 (SSPCTL1) Layout 749
Table 19-7: SSP Control Register 1 (SSPCTL1) Field Description 749
Table 19-8: SSP Status Register (SSPSTS) Layout 752
Table 19-9: SSP Status Register (SSPSTS) Field Description 752
Table 19-10: SSP Interrupt Force Register (SSPFRC) Layout 754

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Table 19-11: SSP Interrupt Force Register (SSPFRC) Field Description 754
Table 19-12: SSP Data Register (SSPDATA) Layout 755
Table 19-13: SSP Data Register (SSPDATA) Field Description 755
Table 19-14: SSP Time Out Register (SSPTO) Layout 755
Table 19-15: SSP Time Out Register (SSPTO) Field Description 755
Table 20-1: Flash module organization 759
Table 20-2: Flash memory read access latency 759
Table 20-3: Organization and description of the Configuration Words 766
Table 20-4: Flash Module Base Address 769
Table 20-5: Flash Register Map 769
Table 20-6: Flash Control Register (FLASHCTL) Layout 770
Table 20-7: Flash Control Register (FLASHCTL) Field Description 770
Table 20-8: Flash Address Register (FLASHADDR) Layout 771
Table 20-9: Flash Address Register (FLASHADDR) Field Description 771
Table 20-10: Flash Data Input Register (FLASHDIN) Layout 771
Table 20-11: Flash Data Input Register (FLASHDIN) Field Description 771
Table 20-12: Flash Data Output Register (FLASHDOUT) Layout 772
Table 20-13: Flash Data Output Register (FLASHDOUT) Field Description 772
Table 20-14: Flash Write Protect Register 0 (FLASHWP0) Layout 773
Table 20-15: Flash Write Protect Register 0 (FLASHWP0) Field Description 773
Table 20-16: Flash Write Protect Register 1 (FLASHWP1) Layout 777
Table 20-17: Flash Write Protect Register 1 (FLASHWP1) Field Description 777
Table 20-18: Flash Write Protect Register 2 (FLASHWP2) Layout 781
Table 20-19: Flash Write Protect Register 2 (FLASHWP2) Field Description 781
Table 20-20: Flash Write Protect Register 3 (FLASHWP3) Layout 785
Table 20-21: Flash Write Protect Register 3 (FLASHWP3) Field Description 785
Table 20-22: Flash Register Write-Allow Key Register (FLASHREGKEY) Layout 789
Table 20-23: Flash Register Write-Allow Key Register (FLASHREGKEY) Field Description 789
Table 22-1: SYSTEM Module Base Address 794
Table 22-2: SYSTEM Register Map 794
Table 22-3: Chip ID Register 0 (CID0) Layout 795
Table 22-4: Chip ID Register 0 (CID0) Field Description 795
Table 22-5: Chip ID Register 1 (CID1) Layout 795
Table 22-6: Chip ID Register 1 (CID1) Field Description 795
Table 22-7: Unique ID Register 0 (UID0) Layout 796
Table 22-8: Unique ID Register 0 (UID0) Field Description 796
Table 22-9: Unique ID Register 1 (UID1) Layout 796
Table 22-10: Unique ID Register 1 (UID1) Field Description 796
Table 22-11: Random Number Register 0 (RND0) Layout 797
Table 22-12: Random Number Register 0 (RND0) Field Description 797
Table 22-13: Random Number Register 1 (RND1) Layout 797
Table 22-14: Random Number Register 1 (RND1) Field Description 797
Table 22-15: Revision Information Register 0 (REV0) Layout 798
Table 22-16: Revision Information Register 0 (REV0) Field Description 798
Table 22-17: Revision Information Register 1 (REV1) Layout 798
Table 22-18: Revision Information Register 1 (REV1) Field Description 798
Table 22-19: Memory Error Interrupt Flag Register (MEMIF) Layout 799

SPINTROL

Table 22-20: Memory Error Interrupt Flag Register (MEMIF) Field Description 799
Table 22-21: Memory Error Interrupt Clear Register (MEMIC) Layout 801
Table 22-22: Memory Error Interrupt Clear Register (MEMIC) Field Description 801
Table 22-23: Memory Error Interrupt Enable Register (MEMIE) Layout 803
Table 22-24: Memory Error Interrupt Enable Register (MEMIE) Field Description 803
Table 22-25: Memory ECC Enable Register (MEMECCEN) Layout 805
Table 22-26: Memory ECC Enable Register (MEMECCEN) Field Description 805
Table 22-27: Memory Lock Status Register (MEMLOCKSTS) Layout 806
Table 22-28: Memory Lock Status Register (MEMLOCKSTS) Field Description 806
Table 22-29: Reset Event Status Register (RSTEVTSTS) Layout 808
Table 22-30: Reset Event Status Register (RSTEVTSTS) Field Description 808
Table 22-31: Reset Event Status Clear Register (RSTEVTCLR) Layout 810
Table 22-32: Reset Event Status Clear Register (RSTEVTCLR) Field Description 810
Table 22-33: Reset Event Enable Register (RSTEVTEN) Layout 813
Table 22-34: Reset Event Enable Register (RSTEVTEN) Field Description 813
Table 22-35: System Information Register (SYSINFO) Layout 815
Table 22-36: System Information Register (SYSINFO) Field Description 815
Table 22-37: CAU Control Register (CAUCTL) Layout 816
Table 22-38: CAU Control Register (CAUCTL) Field Description 816
Table 22-39: System Register Write-Allow Key Register (SYSREGKEY) Layout 817
Table 22-40: System Register Write-Allow Key Register (SYSREGKEY) Field Description 817
Table 23-1: DMA hardware handshaking interface for UART and SSP 820
Table 23-2: DMACH Module Base Address 830
Table 23-3: DMACH Register Map 830
Table 23-4: DMA Channel Source Address Register (DMACHSA) Layout 831
Table 23-5: DMA Channel Source Address Register (DMACHSA) Field Description 831
Table 23-6: DMA Channel Destination Address Register (DMACHDA) Layout 831
Table 23-7: DMA Channel Destination Address Register (DMACHDA) Field Description 831
Table 23-8: DMA Channel Control Register 0 (DMACHCTL0) Layout 832
Table 23-9: DMA Channel 0 Control Register 0 (DMACH0CTL0) Field Description 832
Table 23-10: DMA Channel Control Register 1 (DMACHCTL1) Layout 834
Table 23-11: DMA Channel Control Register 1 (DMACHCTL1) Field Description 834
Table 23-12: DMA Channel Control Register 2 (DMACHCTL2) Layout 835
Table 23-13: DMA Channel Control Register 2 (DMACHCTL2) Field Description 835
Table 23-14: DMA Channel Control Register 3 (DMACHCTL3) Layout 837
Table 23-15: DMA Channel Control Register 3 (DMACHCTL3) Field Description 837
Table 23-16: DMAC Module Base Address 838
Table 23-17: DMAC Register Map 838
Table 23-18: DMA Transfer Complete Raw Interrupt Flag Register (DMATCRAWIF) Layout 839
Table 23-19: DMA Transfer Complete Raw Interrupt Flag Register (DMATCRAWIF) Field Description 839
Table 23-20: DMA Error Raw Interrupt Flag Register (DMAERRRAWIF) Layout 840
Table 23-21: DMA Error Raw Interrupt Flag Register (DMAERRRAWIF) Field Description 840
Table 23-22: DMA Transfer Complete Interrupt Flag Register (DMATCIF) Layout 841
Table 23-23: DMA Transfer Complete Interrupt Flag Register (DMATCIF) Field Description 841
Table 23-24: DMA Error Interrupt Flag Register (DMAERRIF) Layout 842
Table 23-25: DMA Error Interrupt Flag Register (DMAERRIF) Field Description 842
Table 23-26: DMA Transfer Complete Interrupt Enable Register (DMATCIE) Layout 843

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Table 23-27: DMA Transfer Complete Interrupt Enable Register (DMATCIE) Field Description 843
Table 23-28: DMA Error Interrupt Enable Register (DMAERRIE) Layout 845
Table 23-29: DMA Error Interrupt Enable Register (DMAERRIE) Field Description 845
Table 23-30: DMA Transfer Complete Interrupt Clear Register (DMATCIC) Layout 847
Table 23-31: DMA Transfer Complete Interrupt Clear Register (DMATCIC) Field Description 847
Table 23-32: DMA Error Interrupt Clear Register (DMAERRIC) Layout 848
Table 23-33: DMA Error Interrupt Clear Register (DMAERRIC) Field Description 848
Table 23-34: DMA Combined Interrupt Flag Register (DMAIF) Layout 849
Table 23-35: DMA Combined Interrupt Flag Register (DMAIF) Field Description 849
Table 23-36: DMA Enable Register (DMAEN) Layout 850
Table 23-37: DMA Enable Register (DMAEN) Field Description 850
Table 23-38: DMA Channel Enable Register (DMACHEN) Layout 851
Table 23-39: DMA Channel Enable Register (DMACHEN) Field Description 851
Table 24-1: Mailbox organization 854
Table 24-2: Mailbox Module Base Address 856
Table 24-3: Mailbox Register Map 856
Table 24-4: Main CPU Trigger CAU Interrupt Control Register (M2CINTCTL) Layout 857
Table 24-5: Main CPU Trigger CAU Interrupt Control Register (M2CINTCTL) Field Description 857
Table 24-6: CAU Trigger Main CPU Interruprt Control Register (C2MINTCTL) Layout 858
Table 24-7: CAU Trigger Main CPU Interruprt Control Register (C2MINTCTL) Field Description 858
Table 25-1: WDT debug behavior 859
Table 25-2: PWM debug behavior 859
Table 25-3: ECAP debug behavior 859
Table 25-4: UART debug behavior 860
Table 25-5: SSP debug behavior 860
Table 25-6: I2C debug behavior 860

SPINTROL

Revision History

Version	Date	Author	Status	Changes
1	2019-07-09	–	Outdated	1. Initial release.
2	2019-08-01	–	Outdated	1. Add design defect note for ECAP module in section 0.
3	2019-08-15	–	Outdated	1. Update Figure 23-1 and Figure 23-5.
4	2019-09-13	–	Outdated	1. Update description and the figure for SRAM allocation in Section 1.4.2. 2. Update the note in Section 3.4 that clock can be observed at GPIO11. 3. Remove the incorrect statement on TBSTS.CNTDIR in Section 10.2. 4. Update the TZ0~TZ4 signal description in Section 10.6. 5. Fix the format issue in Section 10.7. 6. Fix the error in description for option '011' & '100' in Table 10-85.
5	2019-10-10	–	Outdated	1. Update Table 4-3, rename PINMUXKEY to PINMUXREGKEY. 2. Update Table 4-5, modify description of SMT bitfield. 3. Add Table 4-6 and Table 4-7. 4. Remove AESCTL1.RST in Section 6.2.4. 5. Update Timer features in Section 8.1. 6. Update WDT features in Section 9.1. 7. Update titles of Table 9-15 and Table 9-16, rename WDTLOCK to WDTREGKEY. 8. Update Table 10-19, modify description of DBGRUN bitfield. 9. Update Table 10-133, modify description of SOCA bitfield. 10. Update Note in Section 0. 11. Update Table 11-20, modify description of DBGRUN bitfield. 12. Update power-up timing requirements in Section 12.9. 13. Update Table 12-33, modify bitfield description. 14. Update Table 12-55, modify description of SHEN bitfield. 15. Update Table 12-153, modify bitfield description. 16. Change DVDD to AVDD in Chapter 13.

SPINTROL

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Version	Date	Author	Status	Changes
				17. Change PGAxCTL.INPOL to PGAxCTL.CMSEL in Section 13.4. 18. Remove the content contains PGAxCTL.IBOOST in Section 13.7. 19. Update Table 13-8 to Table 13-19. 20. Change UARTIER.NRZE to UARTIER.NRZME in Section 17.4. 21. Change UARTLSR.TXEMPTY to UARTLSR.TXDONE in Section 17.4.2. 22. Remove Table Method statement in Section 17.4.3. 23. Update Table 17-26, modify description of XMITIR bitfield. 24. Update Table 18-67, Table 18-77 and Table 18-79, change I2CCTL_EN to I2CENABLE. 25. Update Table 19-1, change SFM to SFRM. 26. Change SSPCTL1.RXTOIE to SSPSTS.RXTOINT in Section 19.4.3.2. 27. Update Note in Section 19.4.4.5, change SS to SFRM. 28. Modify content in Section 19.4.5. 29. Update Table 19-7, change SSP_CLK/SSP_FRM to SSP_SCLK/SSP_SFRM. 30. Modify content in Section 20.3.1. 31. Update Table 22-28, modify bitfield description.
6	2019-11-28	–	Outdated	1. Update Table 23-12 and Table 23-13, rename FIFODAV to FIFOEMPTY.
7	2020-11-21	–	Outdated	1. Add Table 1-2. 2. Modify content in Section 1.5. 3. Modify content in Section 4.3. 4. Update Table 10-89. 5. Update Figure 12-2. 6. Modify content in Section 12.7. 7. Modify content in Section 12.10.2. 8. Update Section 12.12. 9. Update Section 17.2 for UART features. 10. Add Table 20-2. 11. Update Table 10-11, modify description of GLDPRD bitfield. 12. Update Table 23-12.
8	2021-05-29	–	Outdated	1. Update Figure 10-11. 2. Update Section 23.1 and Figure 23-1. 3. Update Table 23-3.

SPINTROL

Version	Date	Author	Status	Changes
				4. Update Section3.9.11, modified maximum frequency of SIO. 5. Add Table 10-5. 6. Update Figure 10-17 and Figure 10-19. 7. Update Section 1.4.2 for SRAM ECC feature. 8. Update Table 10-19 . 9. Add Section 3.9.1. 10. Update Section 3.9.2 and Section 3.9.4. 11. Update Section 3.10. 12. Update Section 19.4.3, add Note for SSP RXONLY mode.
9	2021-12-24	–	Outdated	1. Update Figure 4-2. 2. Add Figure 4-5. 3. Update Table 4-3 and Table 4-5. 4. Update Table 12-33 and Table 12-153. 5. Update Section 17.4.2.2, add Note for receive interrupt. 6. Update Section 15.2. 7. Update Figure 3-4 and Figure 3-5. 8. Update Section 3.6. 9. Update Table 3-14 and Table 3-15. 10. Update Table 17-27 and Table 17-28, modify the UARTFOR.BYTECNT bit-field width. 11. Update Table 14-1. 12. Update Figure 10-4 13. Update Section 10.6 14. Update Section 15.2 15. Update Section 17.4.5, delete the information of XMODE 16. Update Section 16 17. Update Figure 4-6 and Figure 4-7 18. Update Table 8-3 and Table 8-4 19. Update Section 7.2 20. Add Chapter 25 21. Update Section 1.1
10	2022-07-05	–	Outdated	1. Add Figure 4-1, Figure 4-3 and Figure 4-4. 2. Update Figure 1-2. 3. Add Section 13.9. 4. Add Section 14.5 and Section 15.4. 5. Add Section 16.3. 6. Update Section 12.11. 7. Update Trip-Zone sub-module logic in Section 10.6. 8. Update Example description in Section 15.2.

SPINTROL

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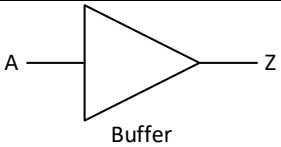
Version	Date	Author	Status	Changes
11	2023-08-28	–	Outdated	1. Update Section 17.5.3, added instructions for configuring automatic baud rate
C/0	2024-09-11	J. Zhou	Outdated	1. Modify number of DAC and buffer in Section 15.1 2. Update Figure 1-4, Figure 1-5. 3. Modify Table 19-15 4. Modify Figure 10-2, Figure 10-3. 5. Modify Figure 15-2. 6. Modify Figure 13-4, Figure 13-5. 7. Modify the wrong bit of TZSEL in Figure 10-14. 8. Modify Figure 4-1. 9. Modify the description of the logic that generates the UART TX interrupt 10. Modify Table 19-7 and Sction 19.4.3.2. 11. Modify Figure 15-2. 12. Modify PWMCLK in Figure 14-1 to ADCCLK, and modify related descriptions synchronously. 13. Note that the multi-zone protection feature doesn't include DRAM in Section 20.5.1.
C/1	2025-10-22	J. Zhou	Released	1. Add description of DMA interrupt. 2. Modify Figure 10-2 and Figure 10-8. 3. Add logic symbols. 4. Added Section 1.2 to describe the resources accessible to both cores, and modified Section 1.4.2.

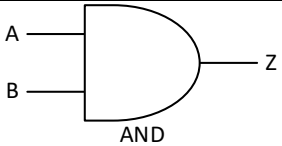
SPINTROL

Logic Symbols



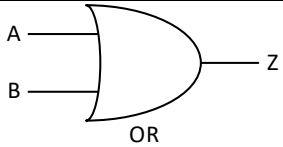
Buffer

A	Z = A
0	0
1	1



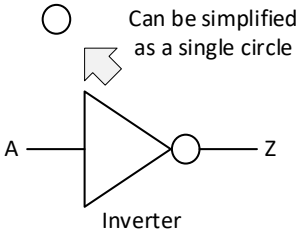
AND

A	B	Z = A and B
0	0	0
0	1	0
1	0	0
1	1	1



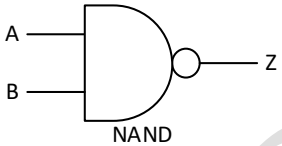
OR

A	B	Z = A or B
0	0	0
0	1	1
1	0	1
1	1	1



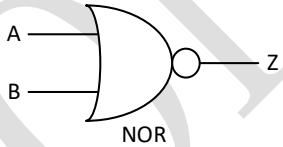
Inverter

A	Z = not A
0	1
1	0



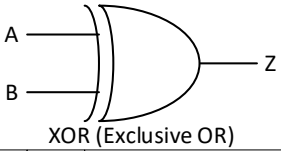
NAND

A	B	Z = not (A and B)
0	0	1
0	1	1
1	0	1
1	1	0



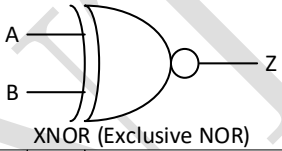
NOR

A	B	Z = not (A or B)
0	0	1
0	1	0
1	0	0
1	1	0



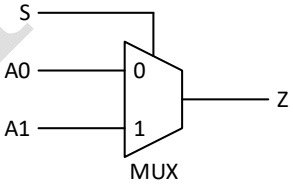
XOR (Exclusive OR)

A	B	Z = (A and not B) or (B and not A)
0	0	0
0	1	1
1	0	1
1	1	0



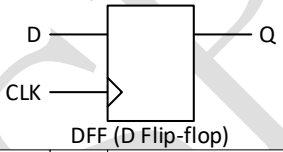
XNOR (Exclusive NOR)

A	B	Z = (A and B) or (not A and not B)
0	0	1
0	1	0
1	0	0
1	1	1



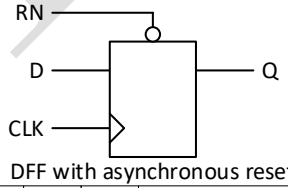
MUX

A0	A1	S	Z = A0 if S = 0 A1 if S = 1
0	any	0	0
1	any	0	1
any	0	1	0
any	1	1	1



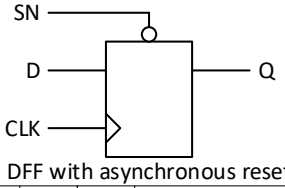
DFF (D Flip-flop)

D	CLK	Q
any	0	keep it's old value
any	1	keep it's old value
any	↓	keep it's old value
0	↑	0
1	↑	1



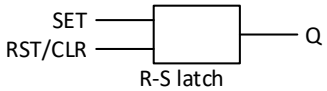
DFF with asynchronous reset

D	RN	CLK	Q
any	0	any	0
any	1	0	keep it's old value
any	1	1	keep it's old value
any	1	↓	keep it's old value
0	1	↑	0
1	1	↑	1



DFF with asynchronous reset

D	SN	CLK	Q
any	0	any	1
any	1	0	keep it's old value
any	1	1	keep it's old value
any	1	↓	keep it's old value
0	1	↑	0
1	1	↑	1



R-S latch

SET	RST	Q
1	0	1
0	1	0
0	0	keep it's old value
1	1	Invalid input

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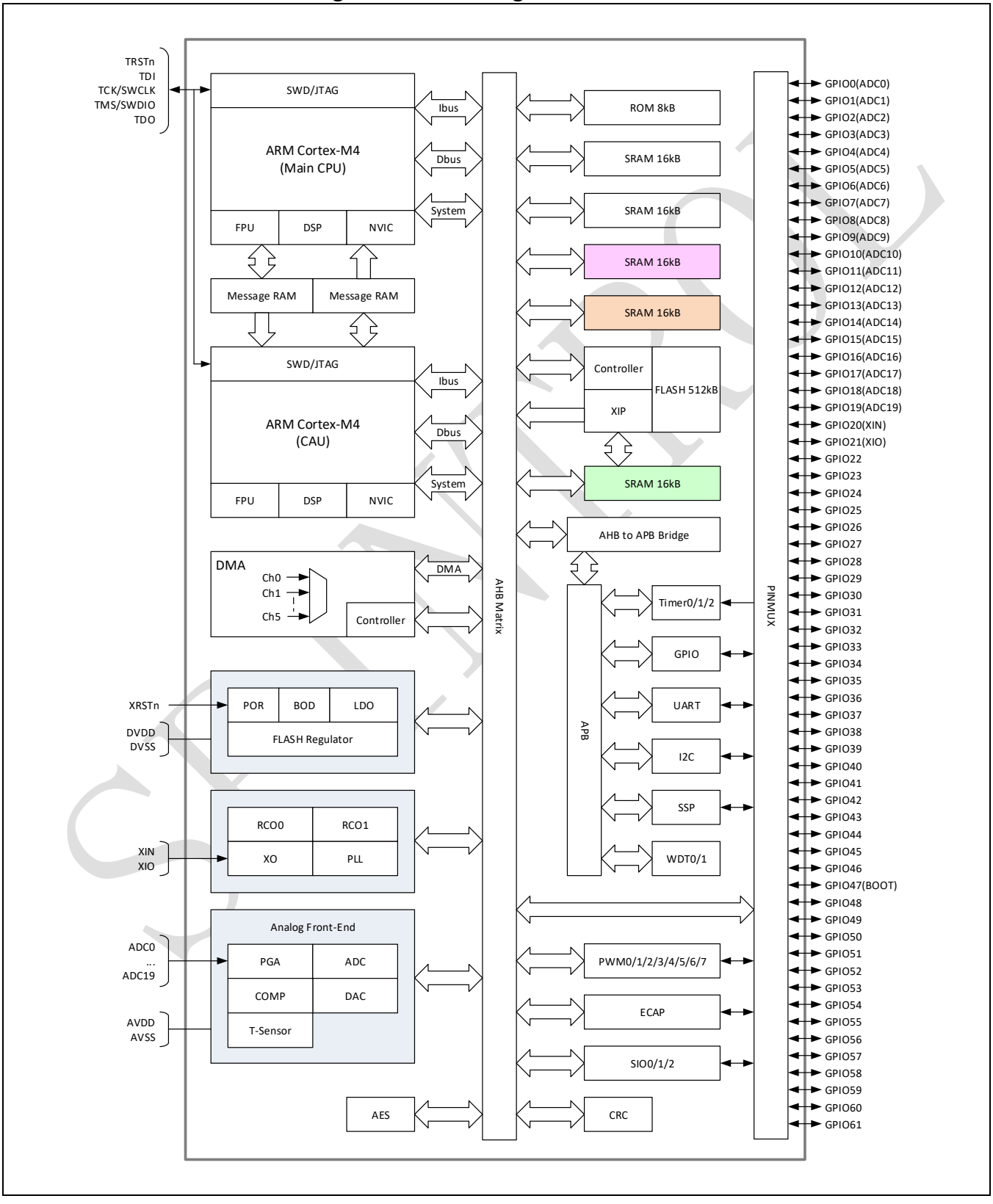
1 Memory and bus architecture

1.1 System architecture

Figure 1-1: Block diagram of SPC2168



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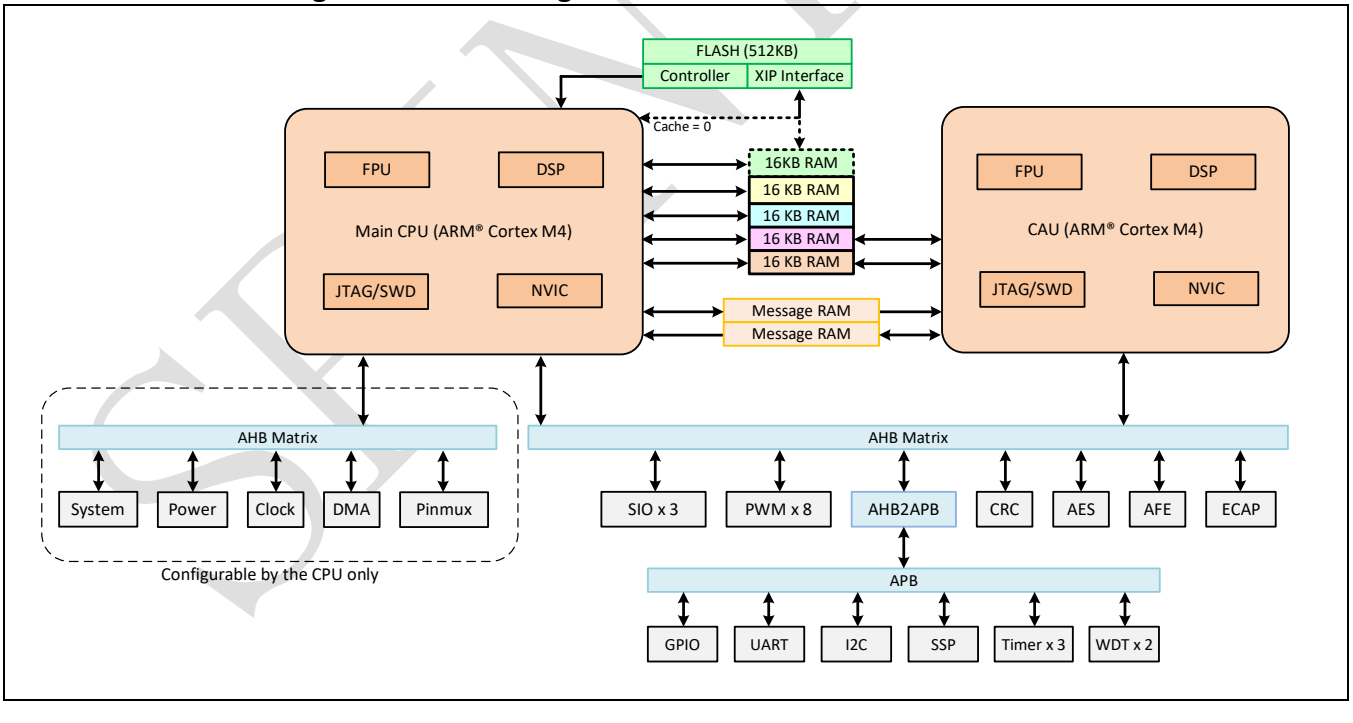
In SPC2168, the main system consists of:

- 7 masters:
  - Main Cortex-M4 I-bus, D-bus and system bus
  - CAU(Control Accelerator Unit) Cortex-M4 I-bus, D-bus and system bus
  - DMA
- 21 slaves:
  - ROM
  - Five 16KB SRAMs: one of them can be used as XIP cache and another two of them can be assigned to main CPU or CAU
  - Flash controller and XIP interface, which is connected to the main CPU only
  - Two MessageBox
  - Power and Clock registers
  - DMA controller registers
  - AHB peripherals: AES, CRC, AFE, PWM, ECAP and SIO0/1/2
  - AHB to APB bridge, which connect all APB peripherals

As shown in Figure 1-1, they are interconnected through a low-latency AHB bus architecture. The AHB-to-APB bridge connects all APB peripherals and synchronizes signals from AHB to APB. The maximum speed of the APB bus is limited to 50 MHz.

1.2 Dual-core resource access

Figure 1-2: Block diagram between the Main CPU and CAU



As shown in Figure 1-2, there are certain areas that can only be accessed by the Main CPU and are inaccessible to the CAU. These include the Flash, portions of the RAM, as well as write operations to the System, Power, Clock, DMA, and Pinmux registers. For details on dual-core access to the RAM, refer to Section 1.4.2.

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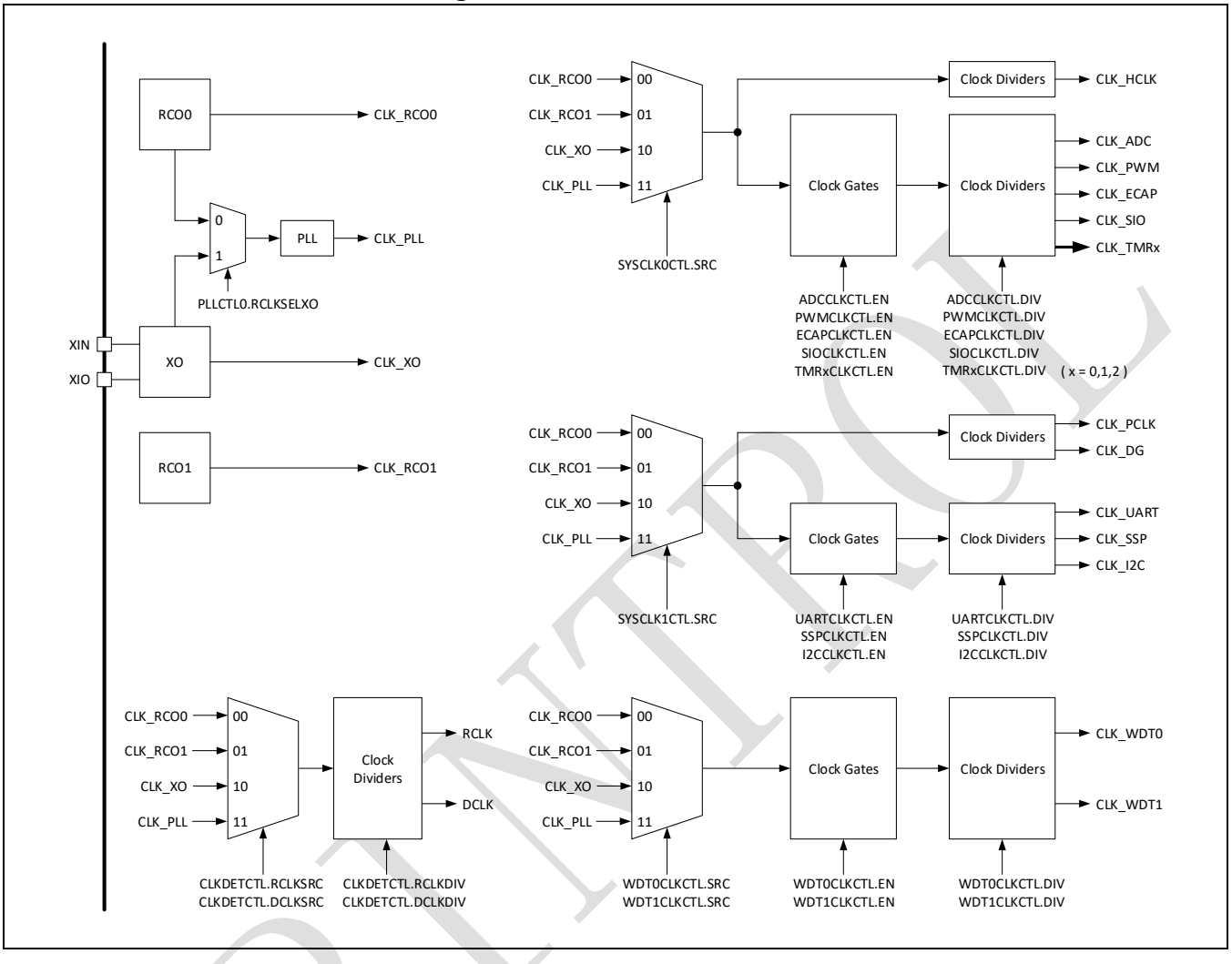
1.3 Clock tree

Figure 1-3: SPC2168 clock tree



As shown in Figure 1-3, there are four root clocks in SPC2168:

- RCO0: Trimmed at 32MHz
- RCO1: Trimmed at 32MHz
- XO: External crystal with on-chip active resonator (2-pin configuration) or external clock input (1-pin configuration via XIN or XIO)
- PLL: Provide flexible on-chip clock up to 200MHz. The reference clock can be selected as RCO0 or XO clock

The succeeding smooth MUX provides glitch-free switching. Dedicated clocks are generated for each function building block with independent clock gate and divider.

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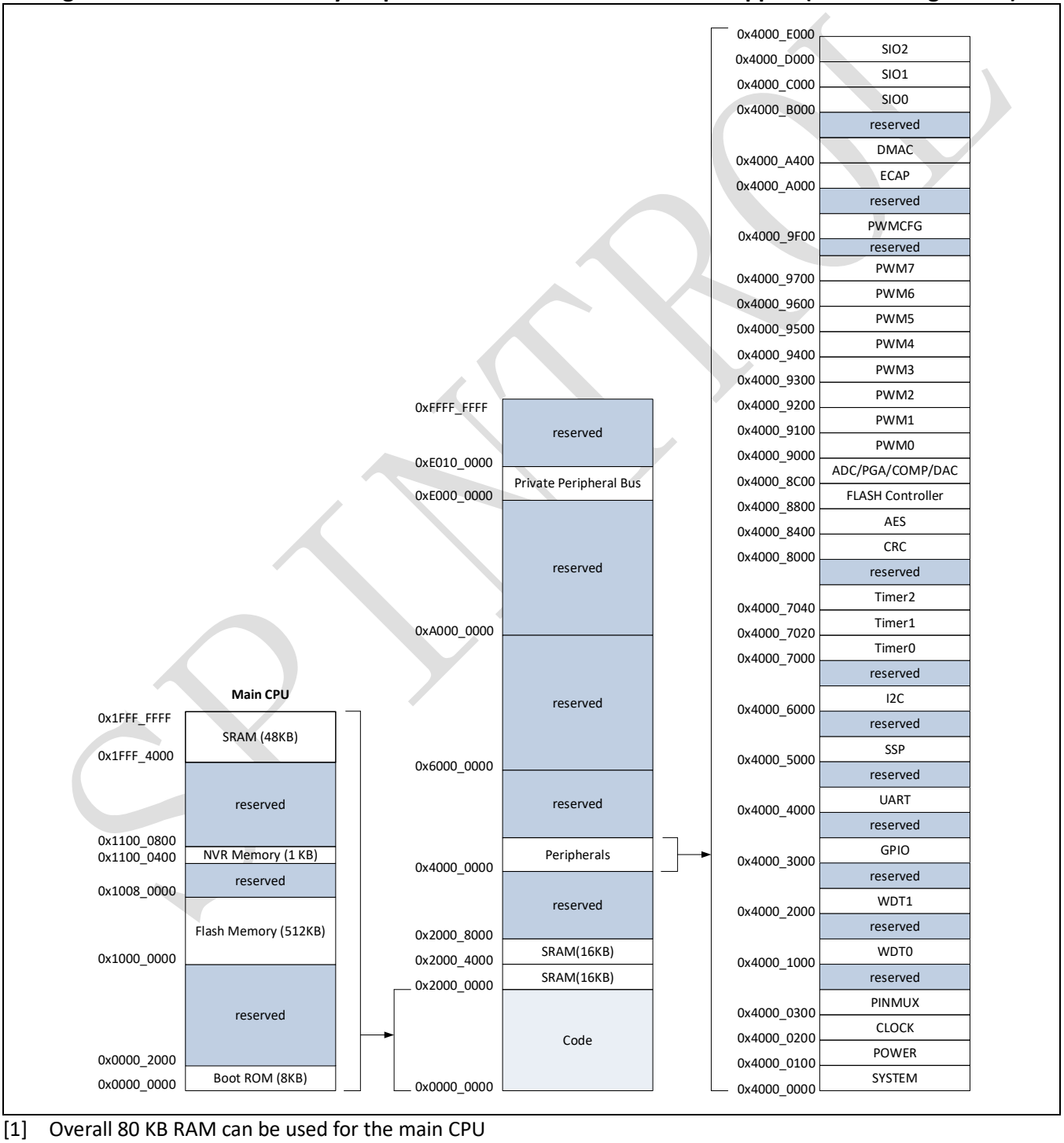
1.4 Memory map

In SPC2168 device, ROM, SRAMs, registers and I/O ports are organized within the same linear 4GB address space. The bytes are coded in memory in Little Endian format.

All the memory areas that are not allocated to on-chip memories and peripherals are considered “Not Used”. Access to these address results in bus fault.The memory map of SPC2168 is shown in Figure 1-4 ~ Figure 1-7.

Figure 1-4: SPC2168 memory map with Cache disabled and CAU stopped (Used as single core)



[1] Overall 80 KB RAM can be used for the main CPU

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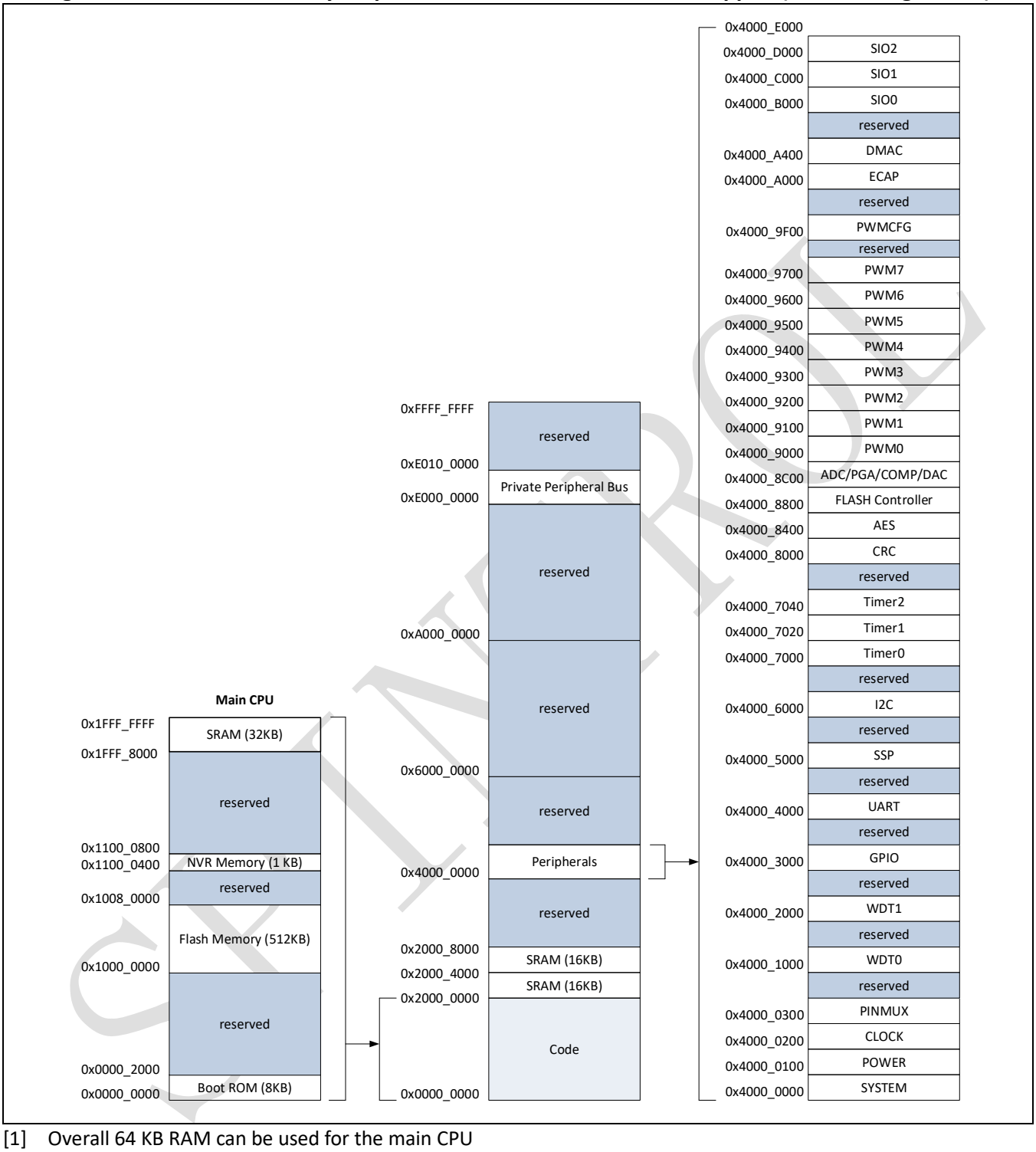
Figure 1-5: SPC2168 memory map with Cache enabled and CAU stopped (Used as single-core)



[1] Overall 64 KB RAM can be used for the main CPU

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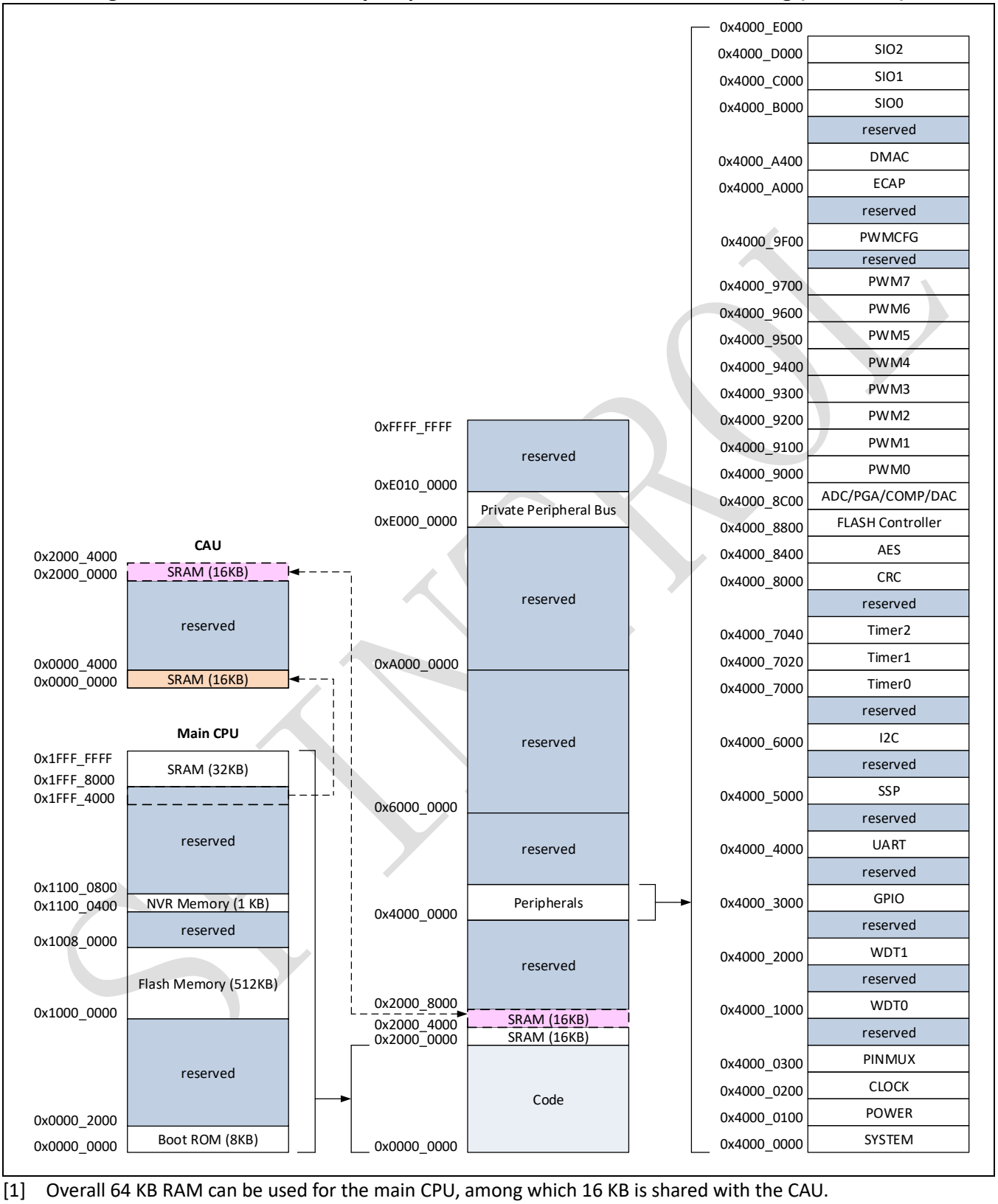
Figure 1-6: SPC2168 memory map with Cache disabled and CAU running (Dual core)



[1] Overall 64 KB RAM can be used for the main CPU, among which 16 KB is shared with the CAU.

[2] Overall 32 KB RAM can be used for the CAU, among which 16 KB is shared with the main CPU.

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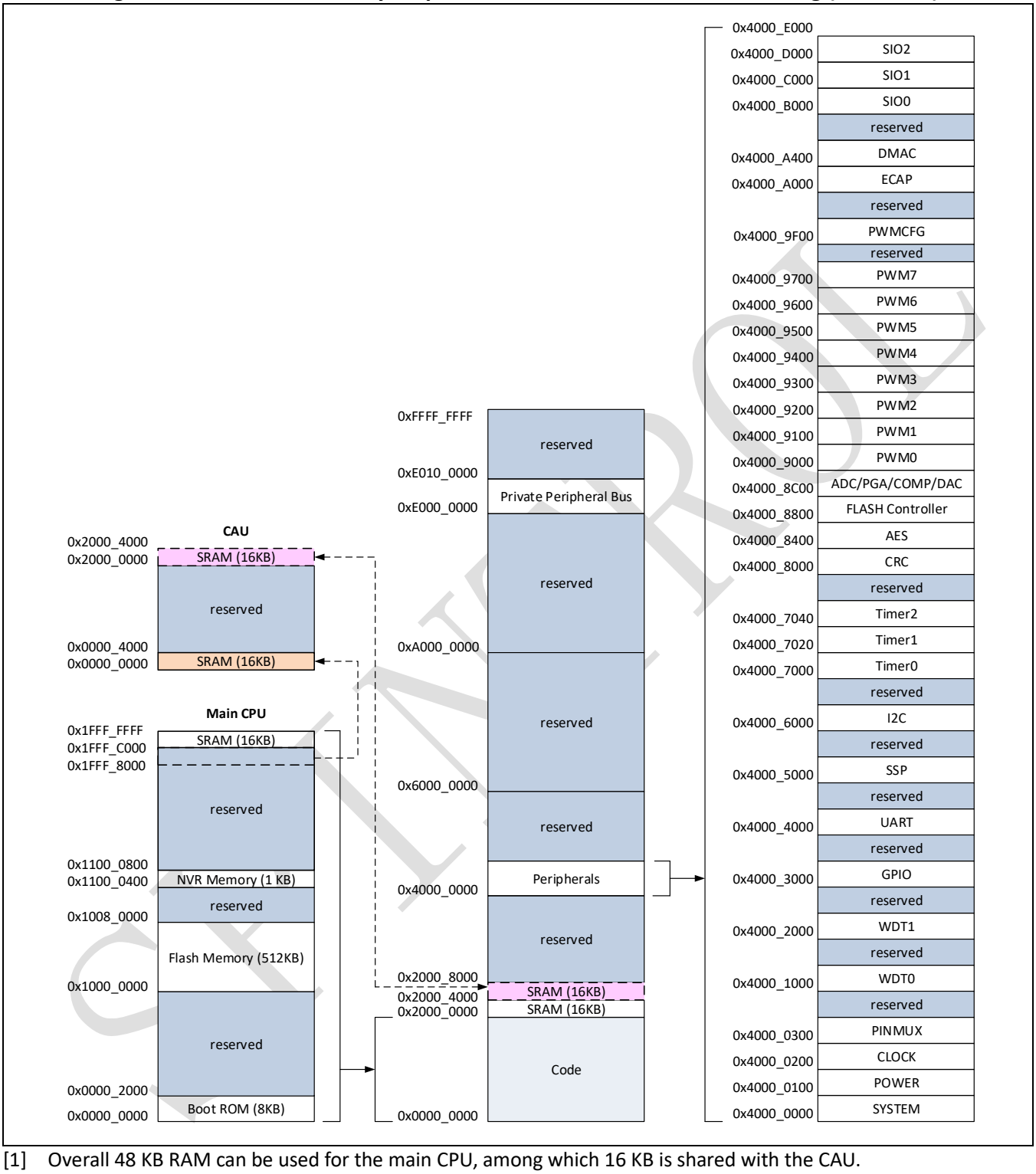
Figure 1-7: SPC2168 memory map with Cache enabled and CAU running (Dual core)



[1] Overall 48 KB RAM can be used for the main CPU, among which 16 KB is shared with the CAU.

[2] Overall 32 KB RAM can be used for the CAU, among which 16 KB is shared with the main CPU.

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Table 1-1 gives the base address of the peripherals available in SPC2168 device.

Table 1-1: Peripheral Module Base Address

Peripheral Module	Base Address	Register Map
SYSTEM	0x4000 0000	Section 22.9.1
POWER	0x4000 0100	Section 2.5.1
CLOCK	0x4000 0200	Section 3.11.1
GPIO	0x4000 3000	Section 4.4.1
PINMUX	0x4100 0300	Section 4.4.3
AES	0x4000 8400	Section 6.3.1
CRC	0x4000 8000	Section 7.4.1
TIMER0	0x4000 7000	Section 8.4.1
TIMER1	0x4000 7020	Section 8.4.1
TIMER2	0x4000 7040	Section 8.4.1
WDT0	0x4000 1000	Section 9.4.1
WDT1	0x4000 2000	Section 9.4.1
PWM0	0x4000 9000	Section 10.11.1
PWM1	0x4000 9100	Section 10.11.1
PWM2	0x4000 9200	Section 10.11.1
PWM3	0x4000 9300	Section 10.11.1
PWM4	0x4000 9400	Section 10.11.1
PWM5	0x4000 9500	Section 10.11.1
PWM6	0x4000 9600	Section 10.11.1
PWM7	0x4000 9700	Section 10.11.1
PWMCFG	0x4000 9F00	Section 10.11.1
ECAP	0x4000 A000	Section 11.7.1
ADC	0x4000 8C00	Section 12.13.1
PGA	0x4000 8C00	Section 13.10.1
COMP	0x4000 8C00	Section 14.6.1
UART	0x4000 4000	Section 17.5.1
I2C	0x4000 6000	Section 18.6.1
SSP	0x4000 5000	Section 19.5.1
FLASH	0x4000 8800	Section 20.8.1
DMAC	0x4000 A400	Section 23.6.1
MAILBOX	0x2000 8200	Section 24.4.1

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1.4.1 Embedded Flash Memory

The SPC2168 is integrated with an embedded flash memory up to 512KB for storing program code and data. An XIP (Execution-in-Place) controller is dedicated to reading of flash memory as shown in Figure 1-1, while another AHB controller interface is used to erase and program the Flash memory. When the SPC2168 starts up, any code in the Flash memory can be directly executed, or loaded into SRAM memory before running from the SRAM. Optional 16KB cache can be enabled to speed up the execution for XIP mode.

For the data safety concern, optional ECC feature is design for both the embedded Flash and the ROM, which is capable to correct 1-bit error and detect 2-bit errors. The error bit correction feature can be enabled or disabled via MEMECCEN register as shown in Table 22-25 and Table 22-26.

The Flash memory is organized into 1024 programmable sectors of 512 words each. The Flash memory can be programmed 32 bits (word) at a time. Data can be erased via 512-byte sector erase, 4KB block erase or entire chip erase.

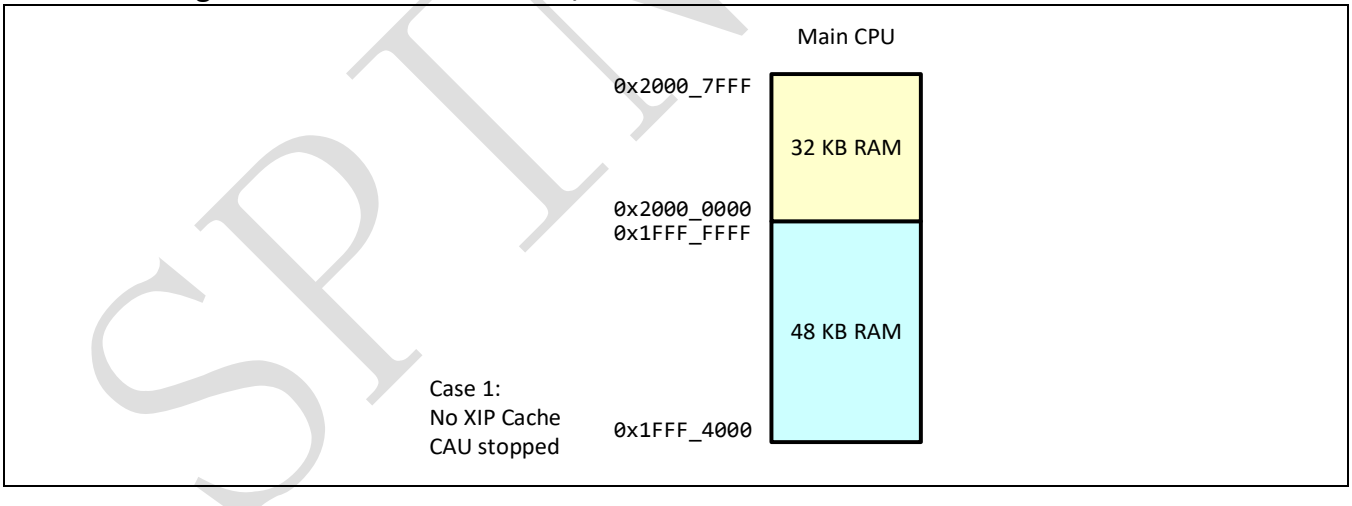
1.4.2 Embedded SRAM

The SPC2168 has implemented multiple SRAM memories for running code and data. The SRAMs can be accessed as bytes, half-words (16 bits) or full words (32 bits) with 0 wait states. Depending on whether Control Accelerator Unit (CAU) and cache for XIP are available, the address of overall 80KB SRAM is re-arranged as shown in Figure 1-8~Figure 1-11.

- XIP cache is unavailable, CAU is stopped (CAUCTL.RUN=0)

  In this case, all 80KB can be accessed by the main CPU from 0x1FFF4000 to 0x20007FFF.

Figure 1-8: XIP Cache Disabled, SRAM Address Allocation with CAU Disabled



- XIP cache is unavailable, CAU is running (CAUCTL.RUN=1)

  In this case, 48KB SRAM is allocated for main CPU from 0x1FFF8000 to 0x20003FFF. Another 16KB SRAM can be accessed by main CPU from 0x20004000 to 0x20007FFF, and by CAU from 0x20000000 to 0x20003FFF. The left 16KB SRAM, which originally can be accessed by main CPU from 0x1FFF4000 to 0x1FFF7FFF for initializing the CAU code, is now allocated as code RAM for the CAU and can be accessed only by the CAU with address from 0x0000 to 0x3FFF.

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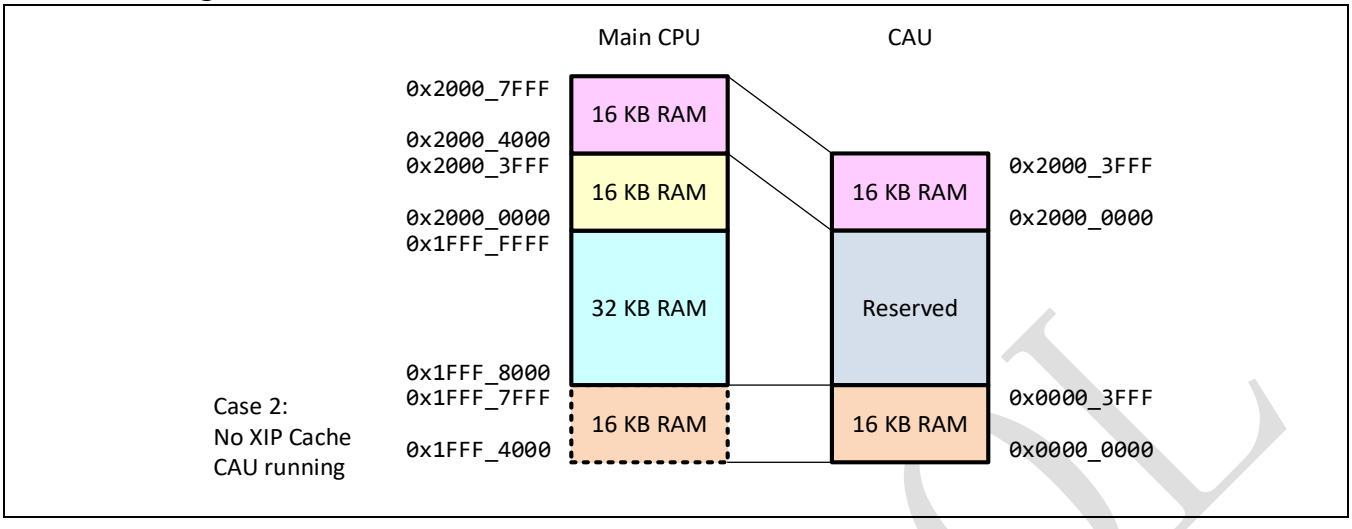
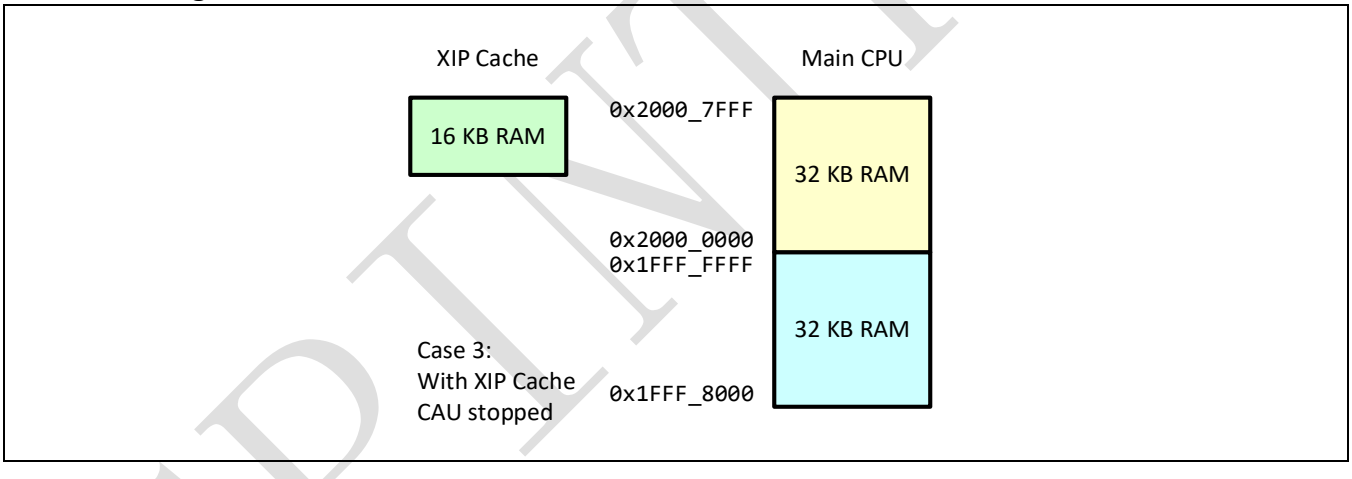
Figure 1-9: XIP Cache Disabled, SRAM Address Allocation with CAU Enabled



- XIP cache is available, CAU is stopped (CAUCTL.RUN=0)

  In this case, 16KB SRAM is used as XIP cache, while the other 64KB is allocated to Main CPU, with user-accessible addresses ranging from 0x1FFF8000 to 0x20007FFF.

Figure 1-10: XIP Cache Enabled, SRAM Address Allocation with CAU Disabled



- XIP cache is available, CAU is running (CAUCTL.RUN=1)

  In this case, 16KB SRAM is used as XIP cahe. 32KB SRAM is allocated for main CPU from 0x1FFFC000 to 0x20003FFF. Another 16KB can be accessed by main CPU from 0x20004000 to 0x20007FFF, and by CAU from 0x20000000 to 0x20003FFF. The left 16KB SRAM, which originally can be accessed by main CPU from 0x1FFF8000 to 0x1FFFBFFF for initializing the CAU code, is now allocated as code RAM for the CAU and can be accessed only by the CAU with address from 0x0000 to 0x3FFF.

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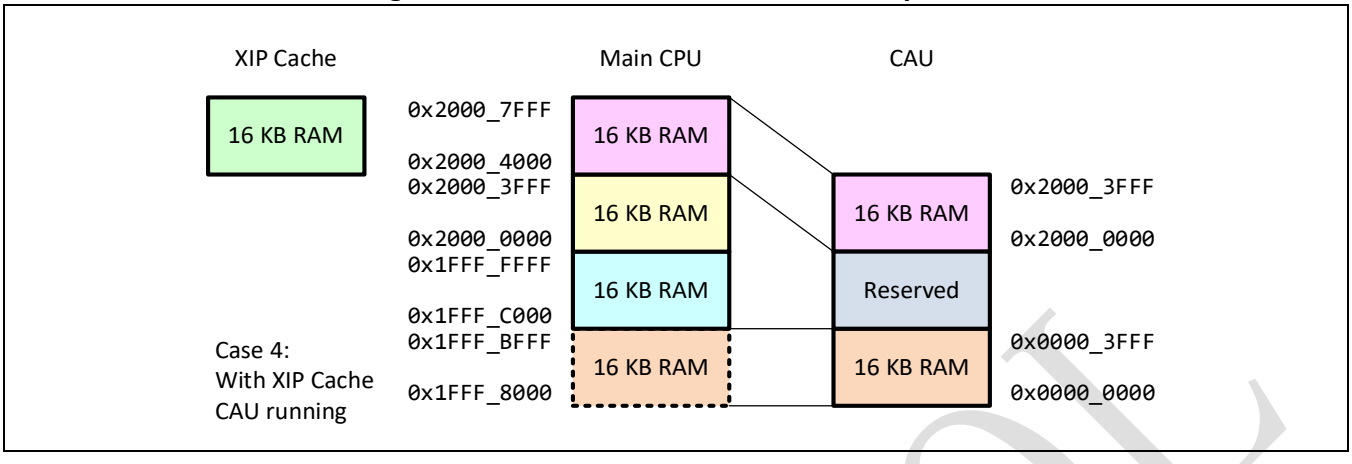
Figure 1-11: SPC2168 SRAM Allocation Options



Additionally, the SPC2168 also implements a ECC check feature for SRAMs to increase the data safety. The ECC feature is capable to correct 1-bit error and detect 2-bit errors. When enabled, an interrupt would be generated upon the 1-bit error correction or 2-bit error detection to notify the Cortex-M4 processor. The feature is controlled by MEMIF, MEMIC and MEMIE register in SYSTEM module. Please see Table 22-19 to Table 22-24 for register details.

SPINTROL

1.5 Boot configuration

In SPC2168, two different boot modes can be selected through BOOT pin:

- Boot from the Flash memory (BOOT pin = High): after a reset, the boot loader jumps to the Flash memory and runs from the address 0x1000 0000
- ISP mode (BOOT pin = Low): the boot loader reprograms the Flash memory by using UART. During the process, for chip with QFN52L package, the GPIO38 is configured as UART_TXD and the GPIO39 is configured as UART_RXD; for chip with other packages, the GPIO44 is configured as UART_TXD and the GPIO45 is configured as UART_RXD.

Note: When BOOT pin is Low, the TRSTn pin must keep Low, or the chip will enter engineering TEST mode.

Table 1-2: Boot modes

Boot mode select pins		Boot Mode
BOOT	TRSTn	
0	0	ISP mode (For chip with QFN52L package, the GPIO38 is configured as UART_TXD and the GPIO39 is configured as UART_RXD; for chip with other packages, the GPIO44 is configured as UART_TXD and the GPIO45 is configured as UART_RXD)
0	1	Engineering TEST mode. In this mode, the chip would not work normal, so **do not select this mode whenever chip was powered**.
1	x	Normal start mode, boot from Flash memory **Note that when TRSTn is high, the debug interface is in active**.

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2 Power

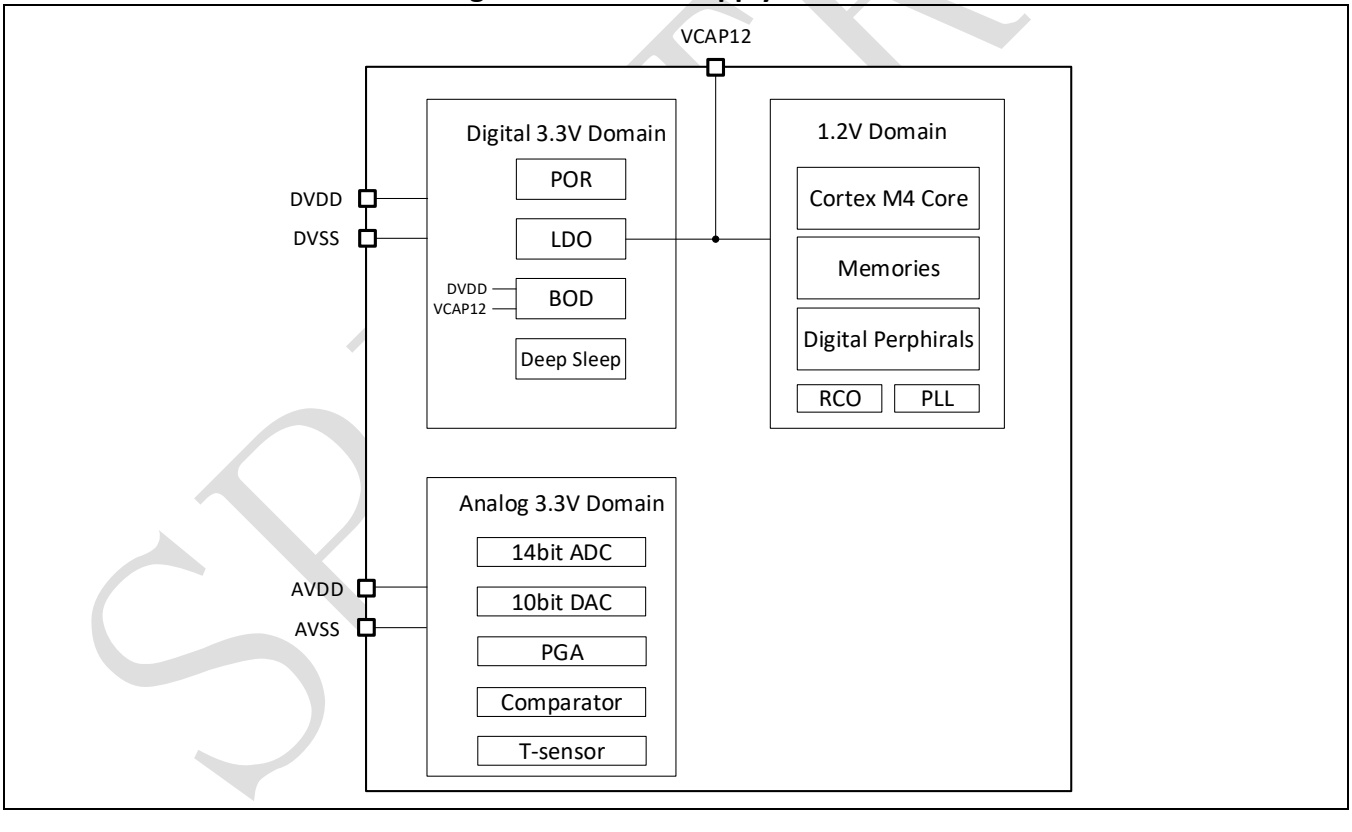
2.1 Single power domain

The SPC2168 implementation requires a single nominal 3.3V power supply DVDD. The nominal 1.2V digital power is obtained via on-chip regulator fed by DVDD and output to the pin VCAP12. There are no special power-sequencing steps required.

During power-up transient, the on-chip regulator guarantees that the current to VCAP12 is below about 30mA. If VCAP12 current exceeds this number (due to on-board parasitic short, for example) during power-up, VCAP12 will not come out and the chip will not power up. This safety feature protects the chip during power-up in case of power pin connection problems.

After VCAP12 is charged up the chip exits reset condition, and the on-chip regulator limits the maximum current delivered to VCAP12 between 500mA and 1A. If the current from VCAP12 exceeds this limit value due to some catastrophic event, the current limit will reset back to about 30mA level and VCAP12 voltage will collapse. This safety feature prevents burn-out of the chip.

Figure 2-1: Power supply overview



2.2 Analog power

The SPC2168 analog power AVDD is at the same level as the main power DVDD described in Section 2.1. Local bypass capacitors between analog power AVDD and analog ground pins AVSS should be placed on board as close to those pins as possible.

SPINTROL

2.3 Brown-out detectors

The Brown-out detectors (BOD) can be used to monitor the 3.3V/1.2V domain power supply by comparing them to the pre-set thresholds. The TOO_HIGH and TOO_LOW flags are available in the BODIF register, to indicate if the 3.3V/1.2V domain is higher or lower than the pre-set thresholds. The TOO_HIGH and TOO_LOW events can generate an interrupt if enabled.

The BOD33CTL and BOD12CTL registers determine how to enable 3.3V/1.2V domain brown-out detector and set the too-high and too-low thresholds. The BODIE register enables the 3.3V/1.2V domain too-high and too-low interrupts.

There are two 1.2V domain monitors. This allows additional level of flexibility. For example, the higher-set level can be set to provide a system alert while a lower-set level can be set to initiate a backup subroutine or reset.

Figure 2-2 and Figure 2-3 shows the 3.3V and 1.2V domain brown-out detector structure.

Figure 2-2: 3.3V domain brown-out detector diagram

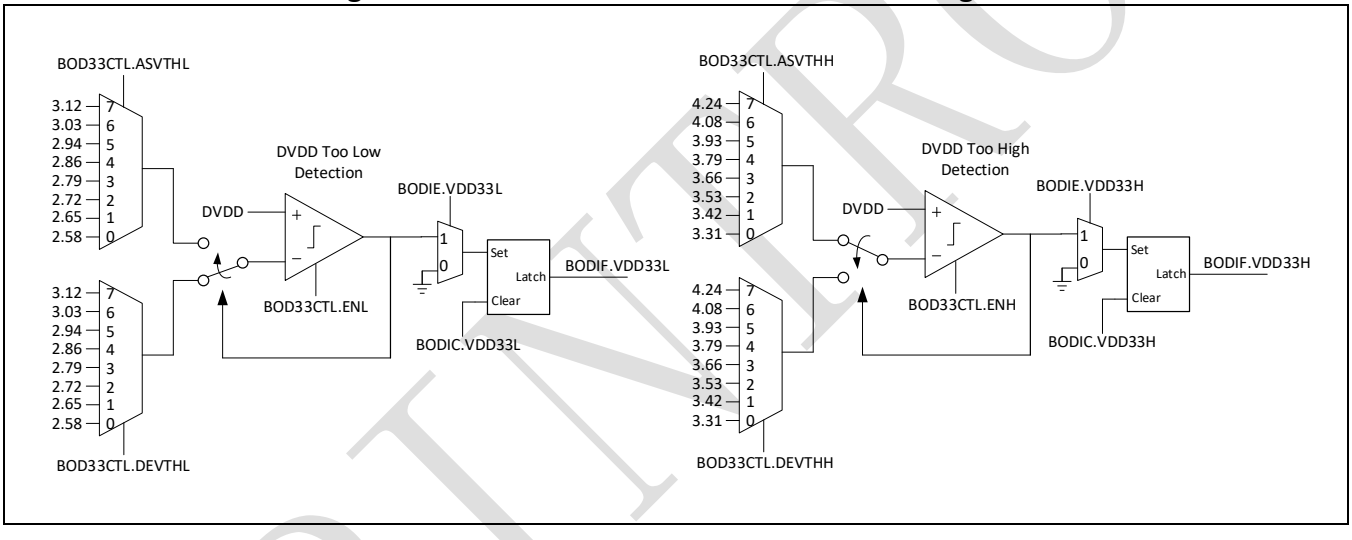
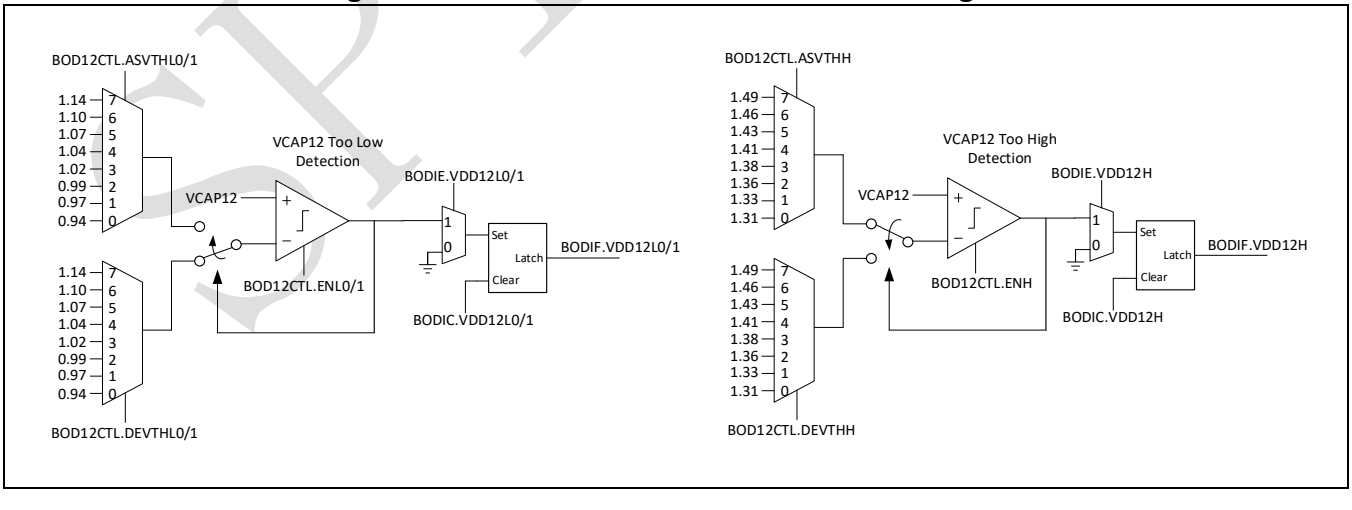


Figure 2-3: 1.2V domain brown-out detector diagram



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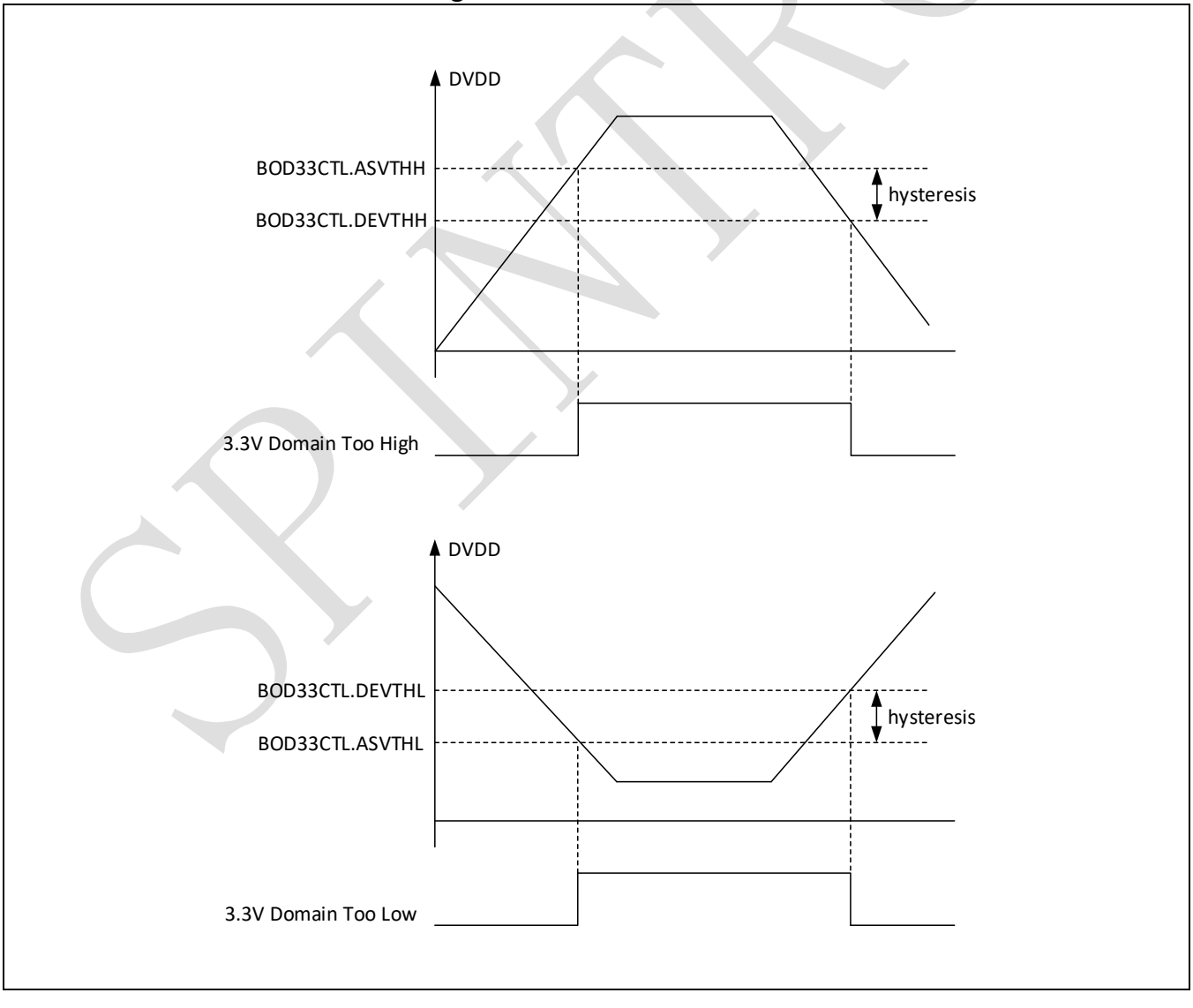
Note: For proper operation of each BOD:

- In Too High Detection, the 0→1 transition code BOD33CTL.ASVTHH/ BOD12CTL.ASVTHH must be larger or equal to 1→0 transition code BOD33CTL.DEVTHH/ BOD12CTL.DEVTHH.
- In Too Low Detection, the 0→1 transition code BOD33CTL.ASVTHL/BOD12CTL.ASVTHL0/ BOD12CTL.ASVTHL1 must be smaller or equal to 1→0 transition code BOD33CTL.DEVTHL/BOD12CTL.DEVTHL0/BOD12CTL.DEVTHL1.

After a reset is triggered, the registers BOD33CTL and BOD12CTL will be reset to their default values. The event thresholds configured by the user before the reset will revert to the default levels. For specific information, please refer to the register list.

The 3.3V domain too-high or too-low interrupt can be generated when DVDD rises above the TOO_HIGH threshold or when DVDD drops below the TOO_LOW threshold.

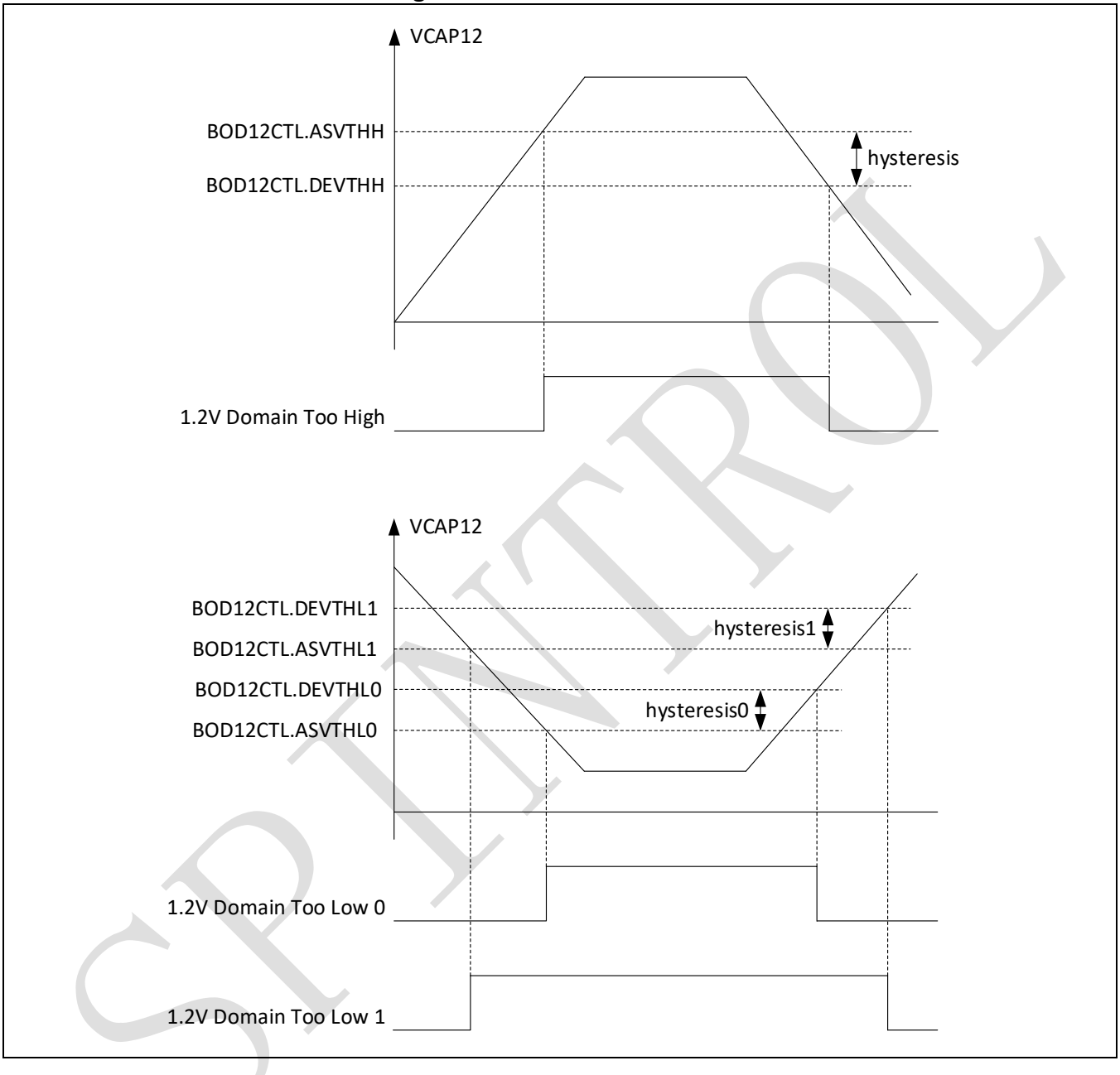
Figure 2-4: DVDD thresholds



SPINTROL

The 1.2V too-high or too-low interrupt can be generated when VCAP12 rises above the TOO_HIGH threshold or when VCAP12 drops below the TOO_LOW threshold.

Figure 2-5: VCAP12 thresholds



2.4 Deep-sleep mode

A deep-sleep mode is implemented for the internal 1.2V LDO in SPC2168. By writing 0x51ee9 to DPSLPKEY register, the 1.2V LDO can be disabled and the system enters into deep-sleep mode for power saving. The whole system can be waken up by pull down XRSTn pin.

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2.5 Registers

2.5.1 Power register map

Table 2-1: POWER Module Base Address

Peripheral Module	Base Address
POWER	0x4000 0100

Table 2-2: POWER Register Map

Register	Offset	Description	Reset Value
PWRSTS	0x00	Power Status Register	0x00000001
LDOCTL*	0x04	LDO Control Register	0x00000007
PORCTL*	0x0C	Low Power POR Control Register	0x00000000
BODIF	0x10	BOD Interrupt Flag Register	0x00000000
BODIC	0x14	BOD Interrupt Clear Register	0x00000000
BODIE*	0x18	BOD Interrupt Enable Register	0x00000000
BODCTL*	0x1C	BOD Control Register	0x00000007
BOD33CTL*	0x20	3.3V BOD Control Register	0x00006E10
BOD12CTL*	0x24	1.2V BOD Control Register	0x006E1010
DPSLPKEY*	0x28	Deep Sleep Enable Key Register	0x00000000
PWRREGKEY	0x2C	Power Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the PWRREGKEY=0x1ACCE551.

SPINTROL

2.5.2 Power registers

2.5.2.1 Power Status Register (PWRSTS)

Table 2-3: Power Status Register (PWRSTS) Layout

PWRSTS (Power Status Register) Offset: 0x0 Default: 0x00000001 Access: POWER -> PWRSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FLASHREGRDY

Table 2-4: Power Status Register (PWRSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	RESERVED_5	RO	0x0	Reserved
4	RESERVED_4	RO	0x0	Reserved
3	RESERVED_3	RO	0x0	Reserved
2	RESERVED_2	RO	0x0	Reserved
1	RESERVED_1	RO	0x0	Reserved
0	FLASHREGRDY	RO	0x1	Flash regulator ready indicator 0: Not ready 1: Ready

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2.5.2.2 LDO Control Register (LDOCTL)

Table 2-5: LDO Control Register (LDOCTL) Layout

LDOCTL (LDO Control Register) Offset: 0x4 Default: 0x00000007 Access: POWER -> LDOCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				VREFTRIM			

Table 2-6: LDO Control Register (LDOCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3:0	VREFTRIM	RW	0x7	Reference voltage trim for LDO 0000: 1.06V 0001: 1.08V 0010: 1.10V 0011: 1.12V 0100: 1.14V 0101: 1.16V 0110: 1.18V 0111: 1.20V 1000: 1.22V 1001: 1.24V 1010: 1.26V 1011: 1.28V 1100: 1.30V 1101: 1.32V 1110: 1.34V 1111: 1.36V

SPINTROL

2.5.2.3 Low Power POR Control Register (PORCTL)

Table 2-7: Low Power POR Control Register (PORCTL) Layout

PORCTL (Low Power POR Control Register) Offset: 0xC Default: 0x00000000 Access: POWER -> PORCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					RESERVED	XRSTFILT	

Table 2-8: Low Power POR Control Register (PORCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	RESERVED_2	W1C	0x0	Reserved
1:0	XRSTFILT	RW	0x0	External reset input deglitch filtering window 00: 500us 01: 1ms 10: 2ms 11: 4ms

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2.5.2.4 BOD Interrupt Flag Register (BODIF)

Table 2-9: BOD Interrupt Flag Register (BODIF) Layout

BODIF (BOD Interrupt Flag Register) Offset: 0x10 Default: 0x00000000 Access: POWER -> BODIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		BODINT	VDD33H	VDD33L	VDD12H	VDD12L1	VDD12L0

Table 2-10: BOD Interrupt Flag Register (BODIF) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	BODINT	RO	0x0	Latched BOD interrupt flag 0: BOD interrupt does not occur 1: BOD interrupt occurred. Further interrupt will not be generated until this bit is cleared.
4	VDD33H	RO	0x0	Latched VDD33H assertion 0: VDD33H is never asserted 1: VDD33H has been asserted. Further event will not generate interrupt until this bit is cleared.
3	VDD33L	RO	0x0	Latched VDD33L assertion 0: VDD33L is never asserted 1: VDD33L has been asserted. Further event will not generate interrupt until this bit is cleared.
2	VDD12H	RO	0x0	Latched VDD12H assertion 0: VDD12H is never asserted 1: VDD12H has been asserted. Further event will not generate interrupt until this bit is cleared.
1	VDD12L1	RO	0x0	Latched VDD12L1 assertion 0: VDD12L1 is never asserted 1: VDD12L1 has been asserted. Further event will not generate interrupt until this bit is cleared.
0	VDD12L0	RO	0x0	Latched VDD12L0 assertion 0: VDD12L0 is never asserted 1: VDD12L0 has been asserted. Further event will not generate interrupt until this bit is cleared.

SPINTROL

2.5.2.5 BOD Interrupt Clear Register (BODIC)

Table 2-11: BOD Interrupt Clear Register (BODIC) Layout

BODIC (BOD Interrupt Clear Register) Offset: 0x14 Default: 0x00000000 Access: POWER -> BODIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		BODINT	VDD33H	VDD33L	VDD12H	VDD12L1	VDD12L0

Table 2-12: BOD Interrupt Clear Register (BODIC) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	BODINT	W1C	0x0	BOD interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the BODIF.BODINT This bit is self-cleared to 0.
4	VDD33H	W1C	0x0	VDD33H interrupt flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the BODIF.VDD33H This bit is self-cleared to 0.
3	VDD33L	W1C	0x0	VDD33L interrupt flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the BODIF.VDD33L This bit is self-cleared to 0.
2	VDD12H	W1C	0x0	VDD12H interrupt flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the BODIF.VDD12H This bit is self-cleared to 0.
1	VDD12L1	W1C	0x0	VDD12L1 interrupt flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the BODIF.VDD12L1 This bit is self-cleared to 0.
0	VDD12L0	W1C	0x0	VDD12L0 interrupt flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the BODIF.VDD12L0 This bit is self-cleared to 0.

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2.5.2.6 BOD Interrupt Enable Register (BODIE)

Table 2-13: BOD Interrupt Enable Register (BODIE) Layout

BODIE (BOD Interrupt Enable Register) Offset: 0x18 Default: 0x00000000 Access: POWER -> BODIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			VDD33H	VDD33L	VDD12H	VDD12L1	VDD12L0

Table 2-14: BOD Interrupt Enable Register (BODIE) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4	VDD33H	RW	0x0	VDD33H interrupt enable 0: VDD33H event does not generate interrupt 1: VDD33H event generates interrupt
3	VDD33L	RW	0x0	VDD33L interrupt enable 0: VDD33L event does not generate interrupt 1: VDD33L event generates interrupt
2	VDD12H	RW	0x0	VDD12H interrupt enable 0: VDD12H event does not generate interrupt 1: VDD12H event generates interrupt
1	VDD12L1	RW	0x0	VDD12L1 interrupt enable 0: VDD12L1 event does not generate interrupt 1: VDD12L1 event generates interrupt
0	VDD12L0	RW	0x0	VDD12L0 interrupt enable 0: VDD12L0 event does not generate interrupt 1: VDD12L0 event generates interrupt

SPINTROL

2.5.2.7 BOD Control Register (BODCTL)

Table 2-15: BOD Control Register (BODCTL) Layout

BODCTL (BOD Control Register) Offset: 0x1C Default: 0x00000007 Access: POWER -> BODCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				VREFTRIM			

Table 2-16: BOD Control Register (BODCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3:0	VREFTRIM	RW	0x7	BOD reference voltage trim 0000: 1.062V 0001: 1.082V 0010: 1.102V 0011: 1.122V 0100: 1.143V 0101: 1.163V 0110: 1.183V 0111: 1.203V 1000: 1.223V 1001: 1.243V 1010: 1.263V 1011: 1.283V 1100: 1.303V 1101: 1.323V 1110: 1.343V 1111: 1.363V

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2.5.2.8 3.3V BOD Control Register (BOD33CTL)

Table 2-17: 3.3V BOD Control Register (BOD33CTL) Layout

BOD33CTL (3.3V BOD Control Register) Offset: 0x20 Default: 0x00006E10 Access: POWER -> BOD33CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED	DEVTHH			ASVTHH			ENH
7	6	5	4	3	2	1	0
RESERVED	DEVTHL			ASVTHL			ENL

Table 2-18: 3.3V BOD Control Register (BOD33CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:15	RESERVED_31_15	RO	0x0	Reserved
14:12	DEVTHH	RW	0x6	Select the threshold voltage to deassert VDD33H when 3.3V supply is going low 000: 3.31V 001: 3.42V 010: 3.53V 011: 3.66V 100: 3.79V 101: 3.93V 110: 4.08V 111: 4.24V
11:9	ASVTHH	RW	0x7	Select the threshold voltage to assert VDD33H when 3.3V supply is going high 000: 3.31V 001: 3.42V 010: 3.53V 011: 3.66V 100: 3.79V 101: 3.93V 110: 4.08V 111: 4.24V
8	ENH	RW	0x0	VDD33H BOD enable 0: Disable 1: Enable
7	RESERVED_7	RO	0x0	Reserved
6:4	DEVTHL	RW	0x1	Select the threshold voltage to deassert VDD33L when 3.3V supply is going high 000: 2.58V 001: 2.65V

SPINTROL

Bits	Field Name	Type	Reset	Description
				010: 2.72V 011: 2.79V 100: 2.86V 101: 2.94V 110: 3.03V 111: 3.12V
3:1	ASVTHL	RW	0x0	Select the threshold voltage to assert VDD33L when 3.3V supply is going low 000: 2.58V 001: 2.65V 010: 2.72V 011: 2.79V 100: 2.86V 101: 2.94V 110: 3.03V 111: 3.12V
0	ENL	RW	0x0	VDD33L BOD enable 0: Disable 1: Enable

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2.5.2.9 1.2V BOD Control Register (BOD12CTL)

Table 2-19: 1.2V BOD Control Register (BOD12CTL) Layout

BOD12CTL (1.2V BOD Control Register) Offset: 0x24 Default: 0x006E1010 Access: POWER -> BOD12CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED	DEVTHH			ASVTHH			ENH
15	14	13	12	11	10	9	8
RESERVED	DEVTHL1			ASVTHL1			ENL1
7	6	5	4	3	2	1	0
RESERVED	DEVTHL0			ASVTHL0			ENL0

Table 2-20: 1.2V BOD Control Register (BOD12CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:23	RESERVED_31_23	RO	0x0	Reserved
22:20	DEVTHH	RW	0x6	Select the threshold voltage to deassert VDD12H when 1.2V supply is going low 000: 1.31V 001: 1.33V 010: 1.36V 011: 1.38V 100: 1.41V 101: 1.43V 110: 1.46V 111: 1.49V
19:17	ASVTHH	RW	0x7	Select the threshold voltage to assert VDD12H when 1.2V supply is going high 000: 1.31V 001: 1.33V 010: 1.36V 011: 1.38V 100: 1.41V 101: 1.43V 110: 1.46V 111: 1.49V
16	ENH	RW	0x0	VDD12H BOD enable 0: Disable 1: Enable
15	RESERVED_15	RO	0x0	Reserved
14:12	DEVTHL1	RW	0x1	Select the threshold voltage to deassert VDD12L1 when 1.2V supply is going high 000: 0.94V 001: 0.97V

SPINTROL

Bits	Field Name	Type	Reset	Description
				010: 0.99V 011: 1.02V 100: 1.04V 101: 1.07V 110: 1.10V 111: 1.14V
11:9	ASVTHL1	RW	0x0	Select the threshold voltage to assert VDD12L1 when 1.2V supply is going low 000: 0.94V 001: 0.97V 010: 0.99V 011: 1.02V 100: 1.04V 101: 1.07V 110: 1.10V 111: 1.14V
8	ENL1	RW	0x0	VDD12L1 BOD enable 0: Disable 1: Enable
7	RESERVED_7	RO	0x0	Reserved
6:4	DEVTHL0	RW	0x1	Select the threshold voltage to deassert VDD12L0 when 1.2V supply is going high 000: 0.94V 001: 0.97V 010: 0.99V 011: 1.02V 100: 1.04V 101: 1.07V 110: 1.10V 111: 1.14V
3:1	ASVTHL0	RW	0x0	Select the threshold voltage to assert VDD12L0 when 1.2V supply is going low 000: 0.94V 001: 0.97V 010: 0.99V 011: 1.02V 100: 1.04V 101: 1.07V 110: 1.10V 111: 1.14V
0	ENL0	RW	0x0	VDD12L0 BOD enable 0: Disable 1: Enable

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2.5.2.10 Deep Sleep Enable Key Register (DPSLPKEY)

Table 2-21: Deep Sleep Enable Key Register (DPSLPKEY) Layout

DPSLPKEY (Deep Sleep Enable Key Register) Offset: 0x28 Default: 0x00000000 Access: POWER -> DPSLPKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 2-22: Deep Sleep Enable Key Register (DPSLPKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x0	Write 0x51ee9 to force the system go into deep sleep

2.5.2.11 Power Register Write-Allow KEY Register (PWRREGKEY)

Table 2-23: Power Register Write-Allow KEY Register (PWRREGKEY) Layout

PWRREGKEY (Power Register Write-Allow Key Register) Offset: 0x2C Default: 0x1ACCE551 Access: POWER -> PWRREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 2-24: Power Register Write-Allow KEY Register (PWRREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected power registers

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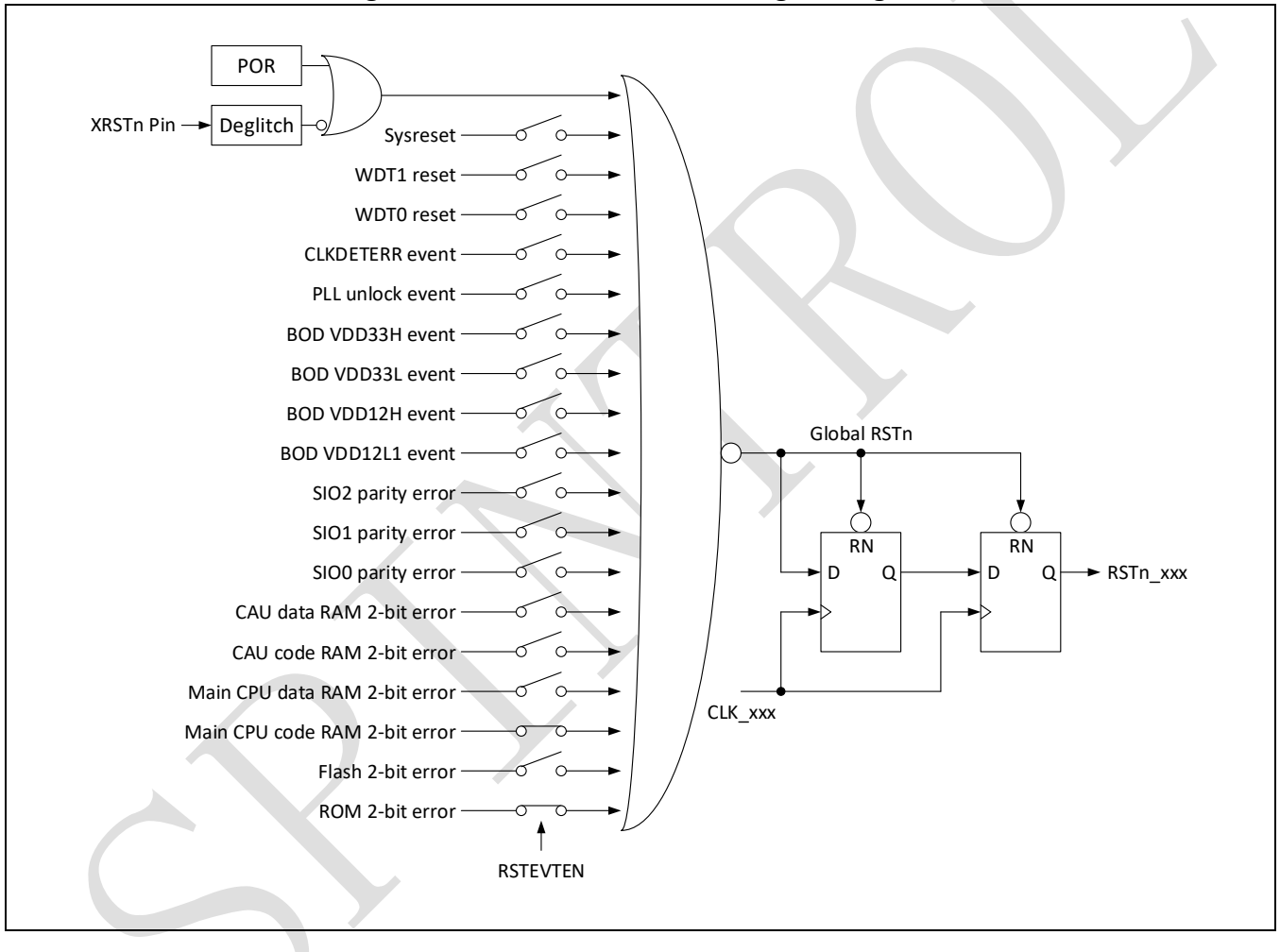
3 Clocks and reset

3.1 Reset architecture

The global active low reset signal of the SPC2168 is a logic NOR of the reset signals from the power-on-reset (POR) block, the XRSTn pin and the functional logic as shown in Figure 3-1. The functional reset source can be the memory errors, the brown-out detector events, the clock error events, the watchdogs, and the Cortex-M4 SYSRESET request.

Figure 3-1: Active-low POR reset signal diagram



As a diagnosis feature, RSTEVTSTS register records the functional reset events, which can be cleared by corresponding bits in RSTEVTCLR register. Besides, the functional reset sources are programmable via RSTEVTEN register. Details are shown in Table 22-29 to Table 22-34.

3.2 Pin reset

The XRSTn pin of the SPC2168 provides super-set global reset for all function blocks, core and analog blocks. It is pull-up internally to make the chip in normal operation mode. The original XRSTn signal goes through a glitch filter with programmable window size as shown in Table 3-1. Both rising and falling edge glitches are filtered. To assert a valid reset, the XRSTn pin should be kept low for time longer than the window size. By default, the window size is 500us.

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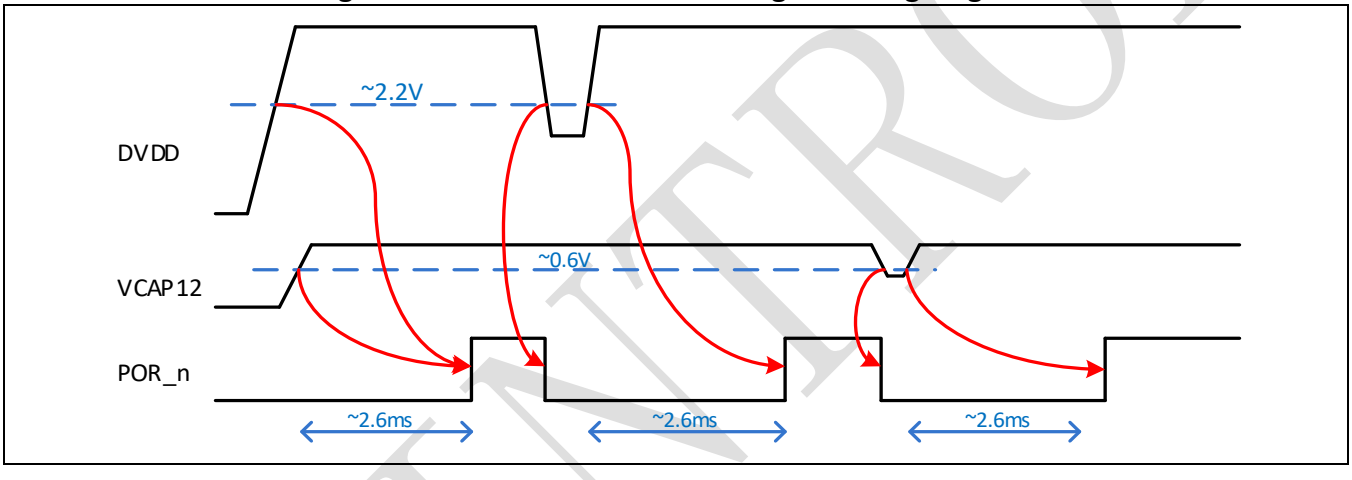
Table 3-1: Pin reset glitch filter window size options

PORCTL.XRSTFILT	Typical Pin Rest Glitch Filter Delay
0	500us
1	1ms
2	2ms
3	4ms

3.3 POR reset

The built-in POR circuits in the SPC2168 guarantee all power up reset sequence requirements and make chip easy to use. It will be asserted for about 2.6ms after power up. The global active-low reset POR_n will go low whenever power levels of DVDD and VCAP12 are below approximately 2.2V and 0.6V respectively as shown in Figure 3-2.

Figure 3-2: Active-low POR reset signal timing diagram



3.4 Clock architecture

The SPC2168 can be clocked by either of the two internal zero-pin RC oscillators, an external oscillator, or by a crystal attached to the on-chip oscillator circuit. A PLL is provided to support high frequency clock from 25MHz to 200MHz while the input frequency for the PLL can be from 4MHz to 56MHz. Combined with programmable dividers and gating blocks, a flexible clock tree is implemented in SPC2168 as shown in Figure 3-3.

Note: The clocks can be brought out to GPIO11 for observation. Refer to Table 4-1 for details.

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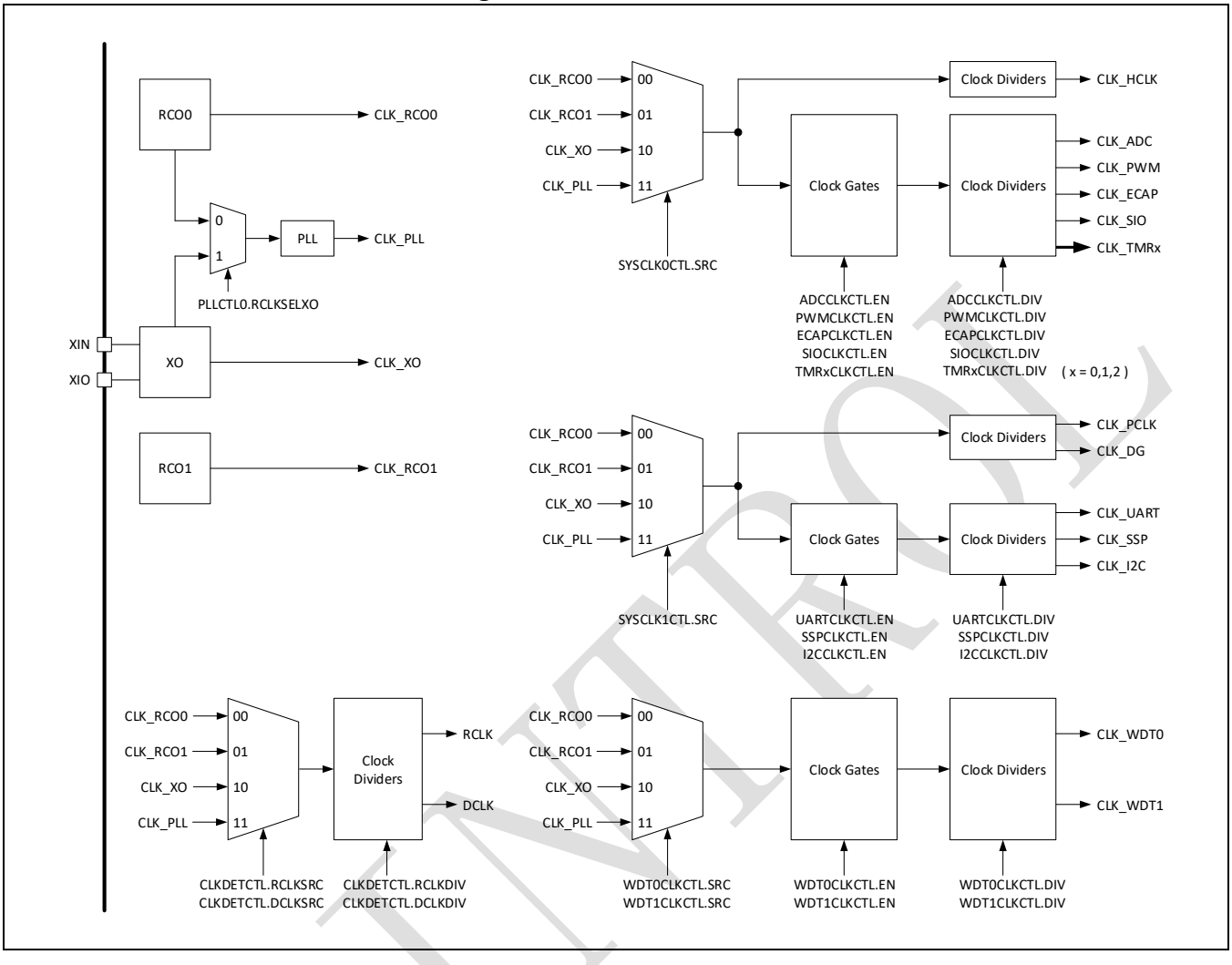
Figure 3-3: Clock overview



3.5 High frequency RC oscillator

There are two identical zero-pin RC oscillators implemented on SPC2168 for clock safety. Both of them have been trimmed for minimum frequency variation over temperature and centered at 32MHz. Optional low frequency mode can be enabled to make each one oscillates at about 270kHz for power saving.

3.6 On-chip crystal oscillator and external clock

Both on-chip and external modes can be used for the crystal oscillator. For the on-chip mode, a crystal is attached as shown in Figure 3-4.

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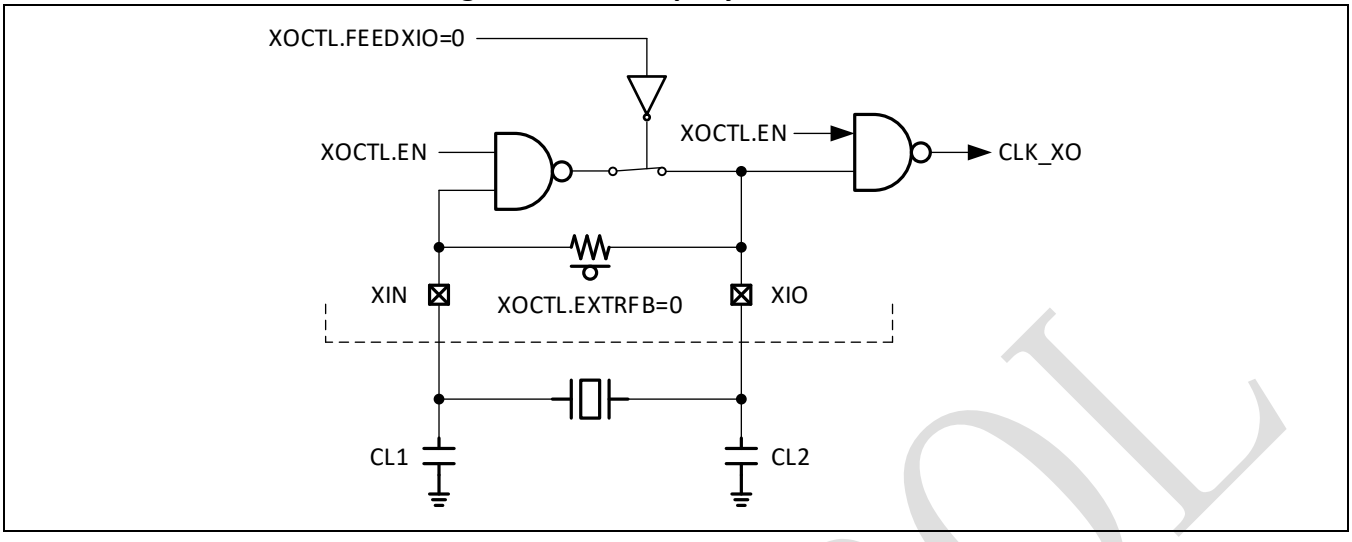
Figure 3-4: On-chip crystal oscillator



To bias the inverter in the high gain region, a feedback resistor Rf is needed which is normally 1MΩ. SPC2168 provides a built-in feedback resistor by default to save the off-chip components. Please refer to the XO characteristics section of the chip datasheet to select an appropriate crystal and the loading capacitor(CL_eff). The loading capacitor CL_eff is defined as the series combination of CL1 and CL2 as shoiwn in Figure 3-4.

For the external clock mode, no extra software configuration is needed compared with the on-chip mode. Depending on XOCTL.FEEDXIO setup, the clock can be fed in via XIN pin (XIO pin is left open) or XIO pin (XIN pin can be used as normal GPIO) as shown in Figure 3-5.

Since the XIN and XIO are pin shared with GPIO20/GPIO21, the pinmux should be configured correctly before setting XOCTL.EN. For safety concern, XOCTL.EN cannot be written to 1 if GPIO20/GPIO21 pinmux is not a valid configuration for either on-chip or external clock mode. And when XOCTL.EN is 1 so that the XO clock is running, the required GPIO20/GPIO21 pinmux configuration cannot be changed.

Note: If the CLK_XO is used as reference for PLL, the external clock frequency should be within from 4MHz to 56MHz.

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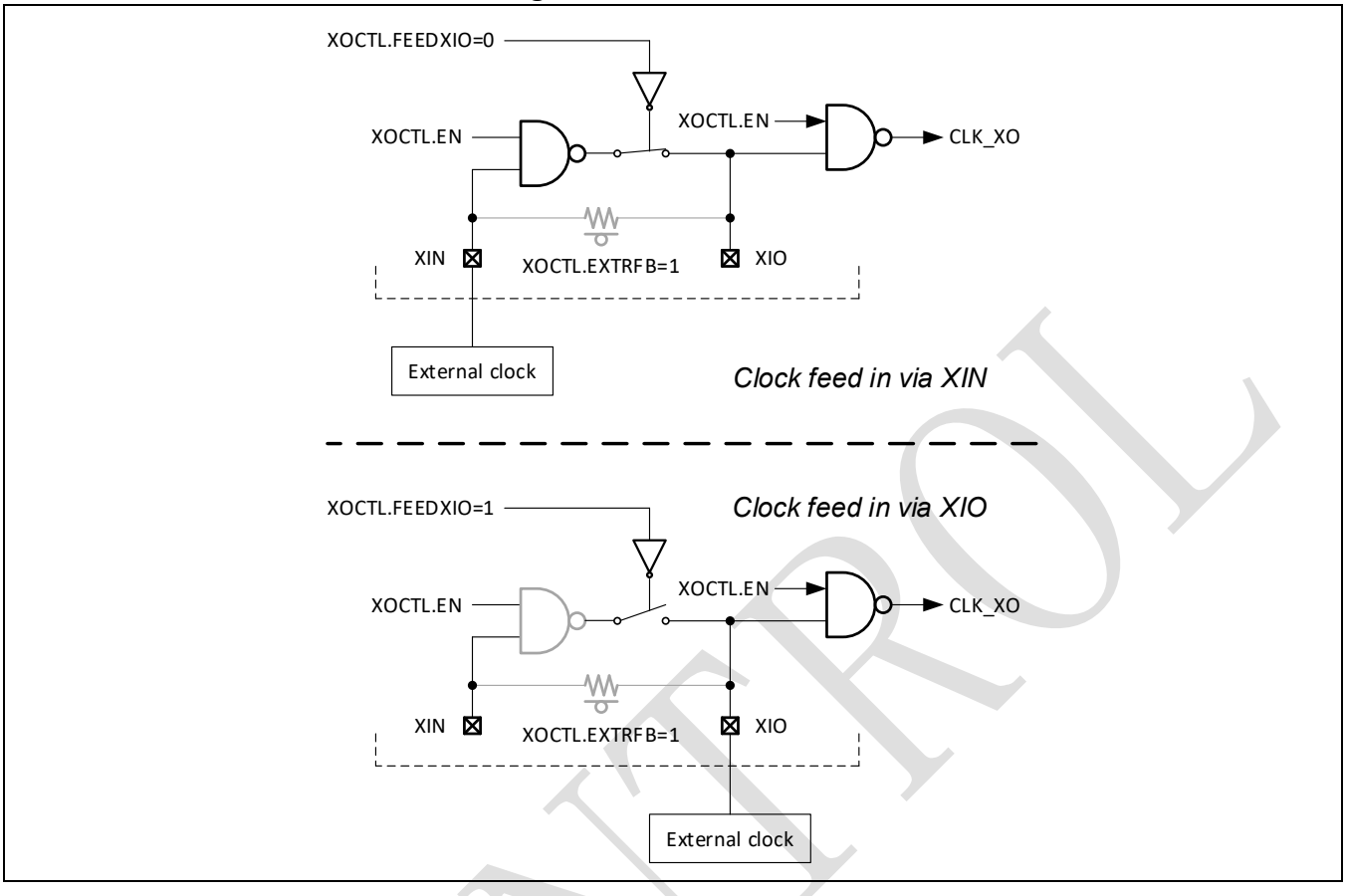
Figure 3-5: External clock

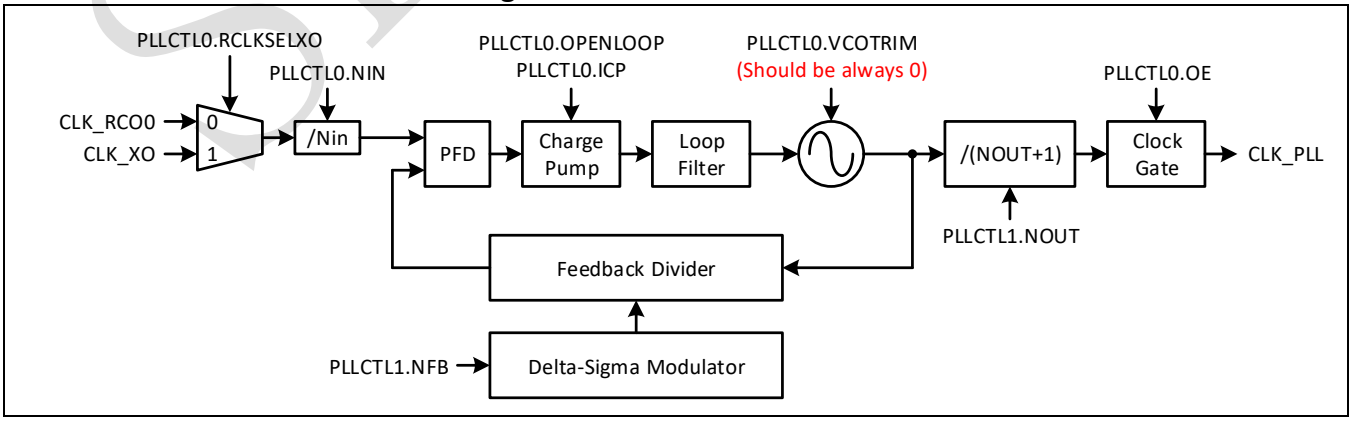


3.7 PLL clock

The architecture of the phase-locked loop in SPC2168 is shown in Figure 3-6. It can take the clock from RCO0 or crystal oscillator as input reference. While the loop is locked, the VCO frequency will be from 400MHz to 600MHz. It is then divided down by programmable divider to provide typically 25MHz to 200MHz clock. The output frequency is given by:

$$f_{PLL} = \frac{f_{REF}}{NIN} \times \frac{NFB}{65536} \times \frac{1}{NOUT + 1}$$

Figure 3-6: PLL clock overview



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3.7.1 Reference input and divider

The PLL is designed to take input clock frequency (Fin) from 4MHz to 56MHz, while the reference clock at PFD input (Fpfd) is from 4MHz to 8MHz. Therefore, the input dividing ratio (Fin/Fpfd) should be configured according to Table 3-2.

Table 3-2: Input dividing ratio configuration

Input Frequency (MHz)	Input Dividing Ratio
4~8	1
8~16	2
16~24	3
24~32	4
32~40	5
40~48	6
48~56	7

3.7.2 Output divider

The tuning range of the VCO is designed to be 400MHz to 600MHz. Combined with the output divider, the output clock frequency at CLK_PLL is shown in Table 3-3.

Table 3-3: Output dividing ratio and clock frequency

Desired Output Frequency			Dividing Ratio (NOUT+1)
400MHz	~	600MHz	1
200MHz	~	300MHz	2
150MHz	~	200MHz	3
100MHz	~	150MHz	4
75MHz	~	100MHz	6
50MHz	~	75MHz	8
37.5MHz	~	50MHz	12
25MHz	~	37.5MHz	16

3.7.3 Feedback divider

Based on the criterion on NIN & NOUT derived from Table 3-2 and Table 3-3, the NFB bit in PLLCTL1 register can be calculated as:

$$NFB = \frac{f_{PLL} \times (NOUT + 1)}{f_{REF} \,/\, NIN} \times 65536$$

3.7.4 PLL unlock detection

A loop unlock detector is included in the phase-frequency detector (PFD) of SPC2168 to provide the diagnosis information for PLL locking status. For the two clocks at the PFD input, if there are two or more rising edges of one clock appears between the two adjacent rising edges of the other clock, internal PLLFAST/PLLSLOW pulse will be generated. These pulses will update the corresponding bit in CLKSTS register. The status bit can be cleared via write a 1 to CLKIC.PLLUNLOCK. Figure 3-7 illustrates a timing diagram for the scenario that reference clock is faster than the divider clock and CLKSTS.PLLSLOW bit is updated.

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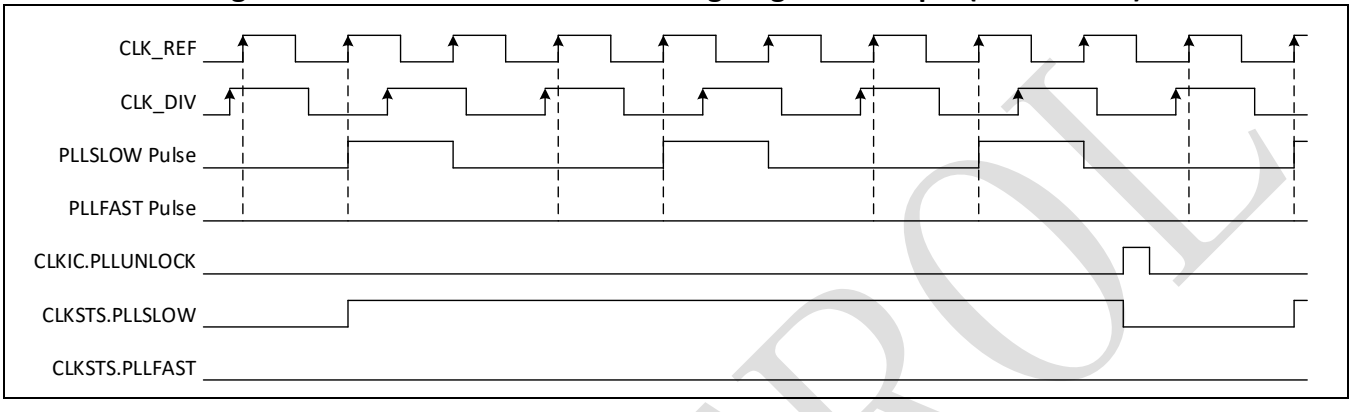
During the initial locking or a significant change on the feedback dividing ratio of a locked PLL, the frequency of the reference clock and divider clock are different and there will be inevitable PLLFAST or PLLSLOW events latched into CLKSTS register. To avoid false alarm, it should wait some time (about 10us) for the loop to be settled and then assert a CLKIC.PLLUNLOCK to clear the latched status and enable interrupt upon PLL unlock event via CLKIE.PLLUNLOCK if wanted. Neither CLKSTS.PLLFAST nor CLKSTS.PLLSLOW will be set afterwards if the PLL is locked.

Figure 3-7: PLL unlock detection timing diagram example (FREF > FDIV)



3.8 Regulator for PLL and RC Oscillator

To have better isolation of the clock generation circuits from the other blocks, the SPC2168 provides dedicated regulator for PLL and RC oscillators. It also makes the supply of the clock generation circuits can be independently configured.

By default, the regulator is bypassed and the power rail of the clock generation circuits is directly tied to the 1.2V power rail of the whole chip.

Note: Before using regulator for the PLL or the RC oscillator, it should be guaranteed that the regulator is enabled and fully settled (CLKSTS.CLKREGRDY=1).

3.9 Clock multiplexers and dividers

3.9.1 Clock smooth Mux

The smooth clock multiplexers are designed to support glitch-free switch on the fly. To avoid switching to an idle clock and makes the CPU stuck, the multiplexer keeps selecting current clock regardless of the control until the target clock is ready. If the currect selecting clock source is RCO0 and RCO0 has failed, the multiplexer will select RCO1 as current clock source and avoid CPU stucked; Meanwhile, a clock detection error event will be generated if clock detection function enabled. It further triggers a CPU interrupt or a PWM trip-zone event if as enabled by corresponding bit in CLKIE and CLKTZE registers.

3.9.2 HCLK

HCLK is the key clock of the SPC2168 that drives the CPU, AHB, memory, AES and CRC blocks. It is divided down from the always-on clock selected via a smooth multiplexer as shown in Figure 3-8. The maximum allowed frequency of HCLK is 200MHz.

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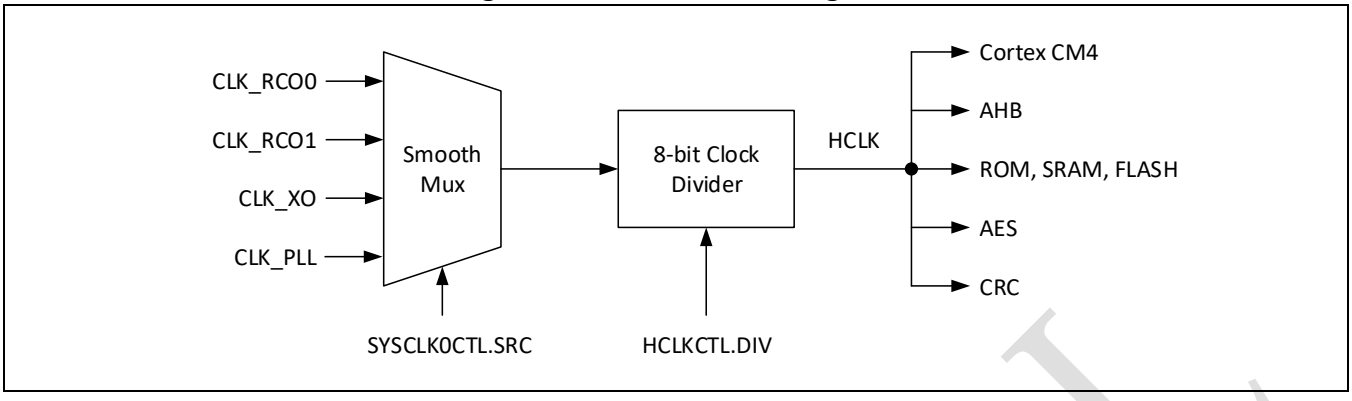
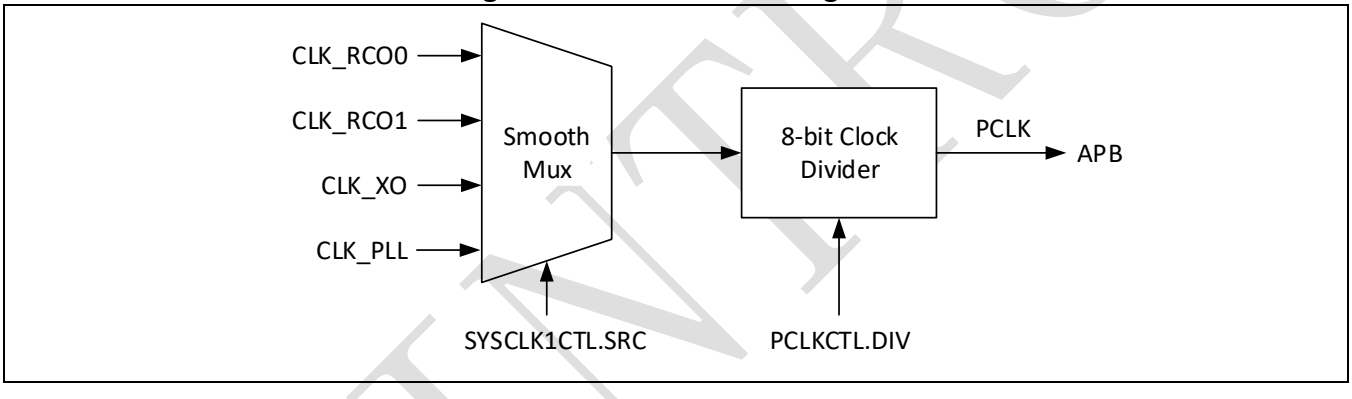
Figure 3-8: HCLK control diagram



3.9.3 APB clock

The APB is driven by PCLK, which is divided down from the always-on clock as shown in Figure 3-9. The maximum allowed frequency of PCLK is 50MHz.

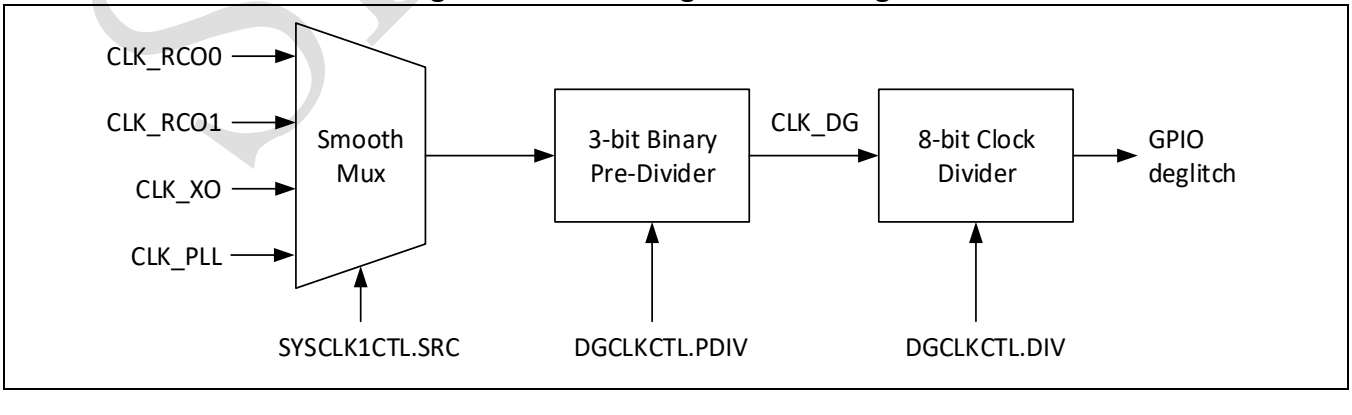
Figure 3-9: PCLK control diagram



3.9.4 GPIO deglitch clock

The GPIO deglitch clock is divided down from the always-on clock by a binary pre-divider and a common 8-bit divider as shown in Figure 3-10. It is used by the GPIOs for input re-timing to filter out the glitches and improve signal integrity. There are 3 clock cycles input delay due to the deglitch filter. The maximum allowed frequency of CLK_DG is 50MHz.

Figure 3-10: GPIO deglitch clock diagram



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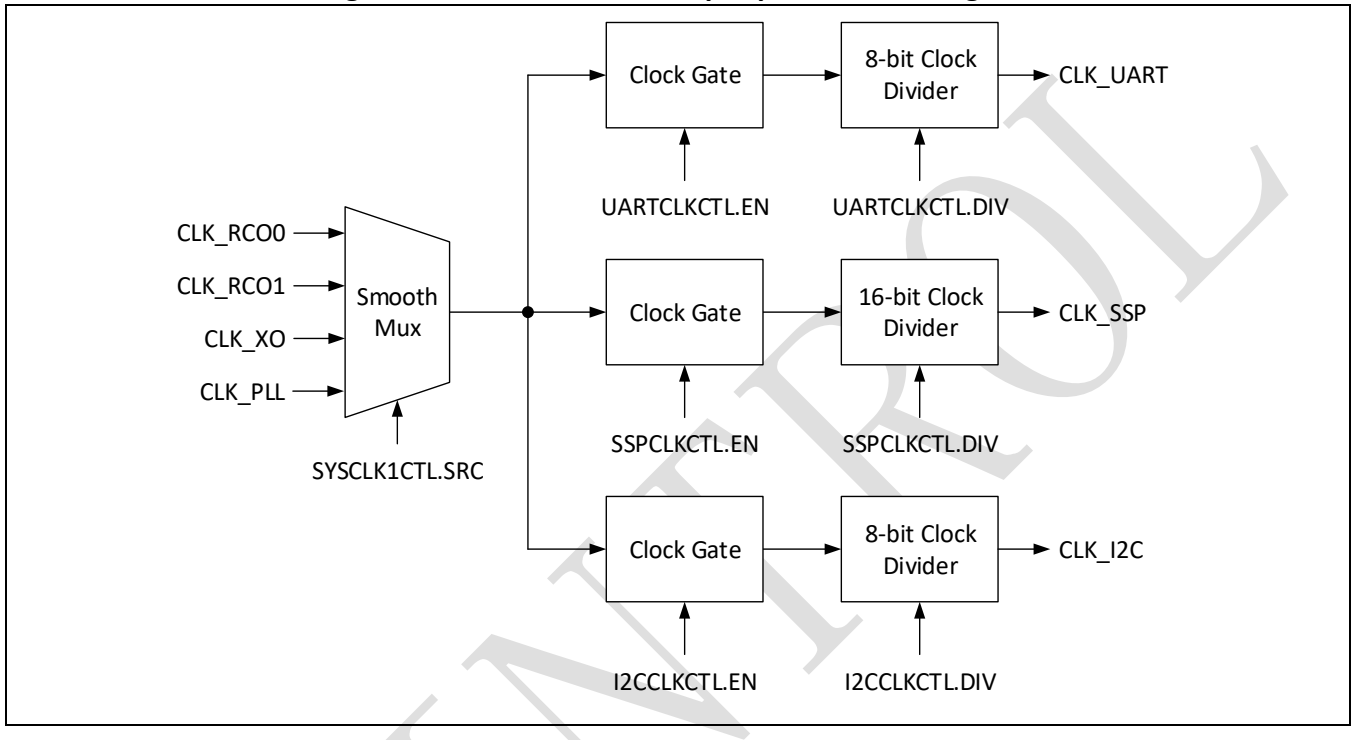
3.9.5 Communication peripheral clock

The SPC2168 provides SSP, UART and I2C interfaces for serial communication. The corresponding clocks are divided down from the selected system clock and can be gated for power saving as shown in Figure 3-11. The maximum allowed frequency for CLK_UART is 200MHz while the maximum allowed frequency for CLK_SSP and CLK_I2C is 50MHz.

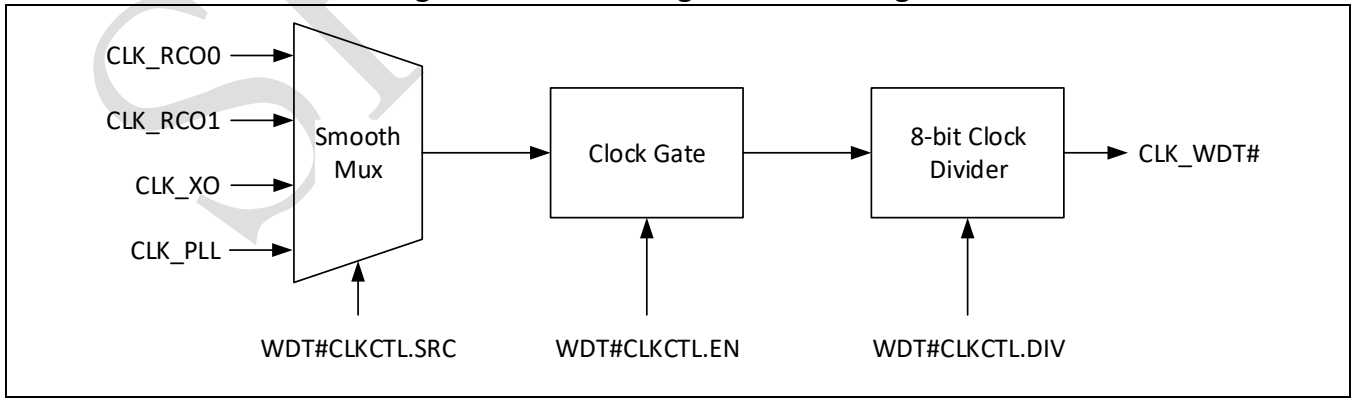
Figure 3-11: Communication peripheral clock diagram



3.9.6 Watchdog timer clock

SPC2168 provides two watchdog timers while each has a dedicated clock that is selected from the four root clocks, gated and divided down as shown in Figure 3-12. The maximum allowed frequency for watchdog timer clock is 200MHz.

Figure 3-12: Watchdog timer clock diagram



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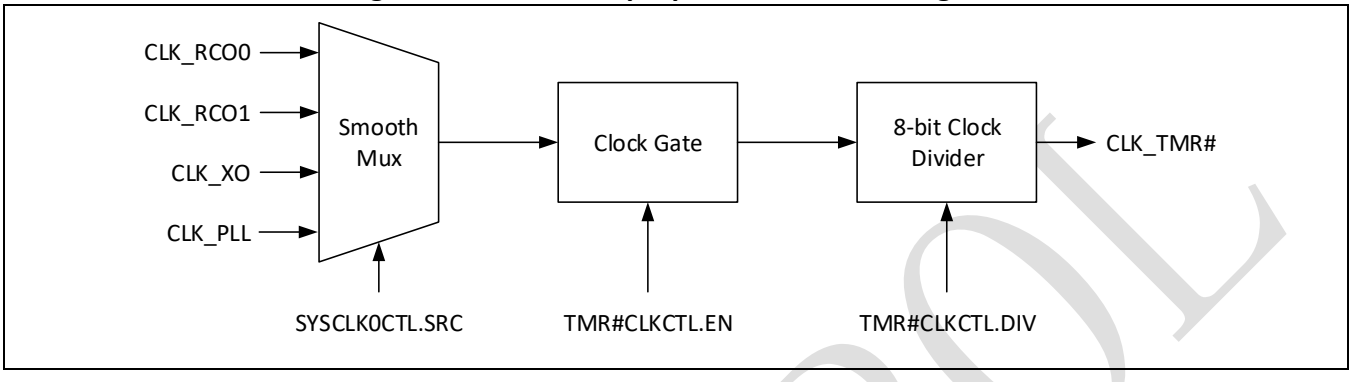
3.9.7 General-purpose timer clock

SPC2168 provides three general timers while each has a dedicated clock that is selected from the four root clocks, gated and divided down as shown in Figure 3-13. The maximum allowed frequency for general timer clock is 200MHz.

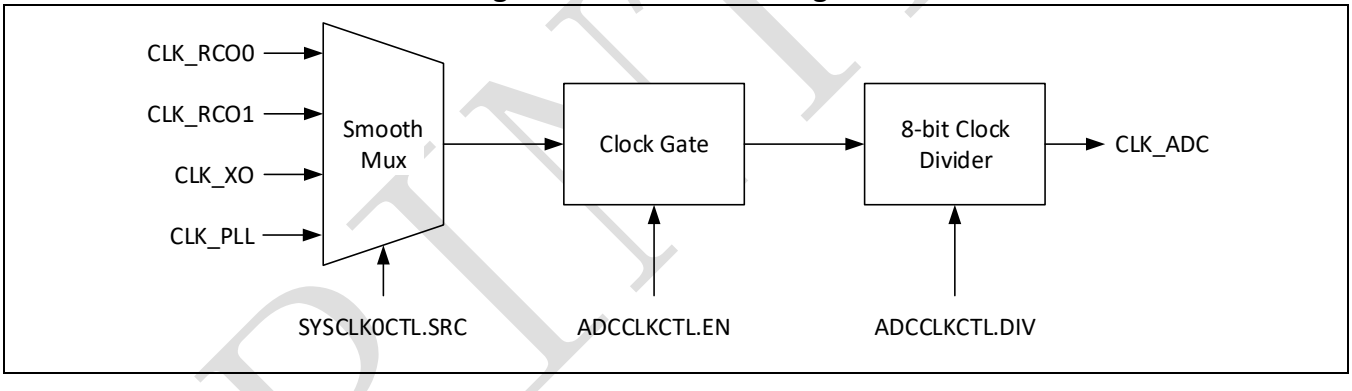
Figure 3-13: General-purpose timer clock diagram



3.9.8 ADC clock

ADC clock is selected from the four root clocks, gated and divided down as shown in Figure 3-14. The maximum allowed frequency is 200MHz.

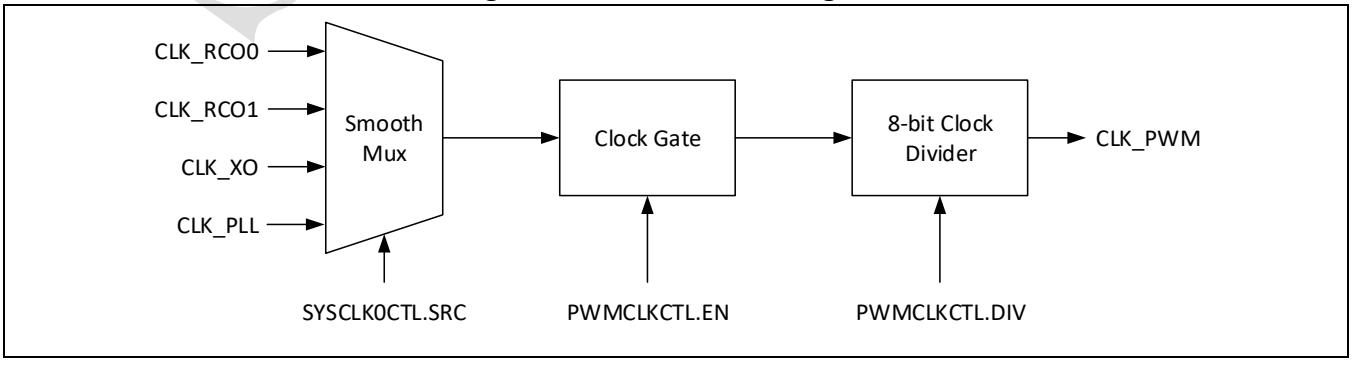
Figure 3-14: ADC clock diagram



3.9.9 PWM clock

The SPC2168 has 8 PWM modules (numbered as from 0 to 7). They share the same clock selected from the four root clocks, gated and divided down as shown in Figure 3-15. The maximum allowed frequency is 200MHz.

Figure 3-15: PWM clock diagram



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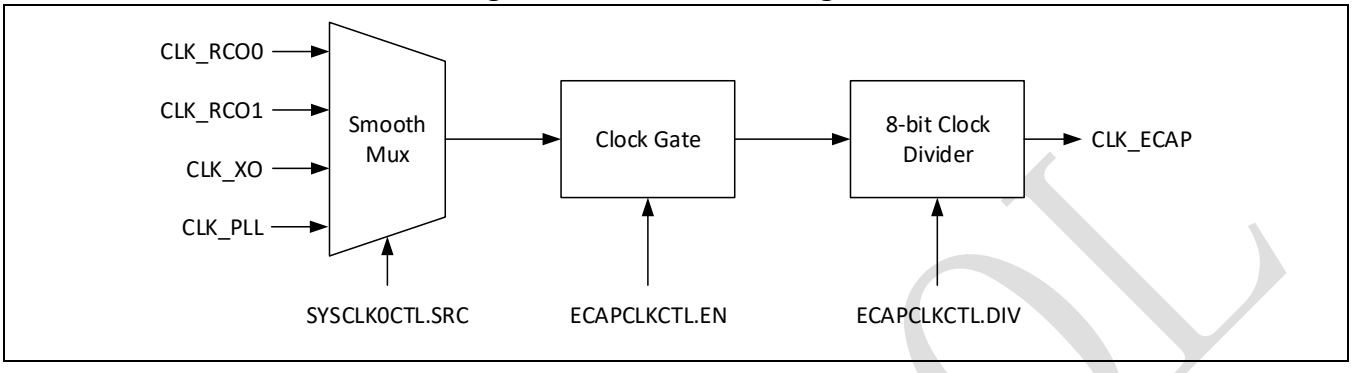
3.9.10 ECAP clock

ECAP clock is selected from the four root clocks, gated and divided down as shown in Figure 3-16. The maximum allowed frequency is 200MHz.

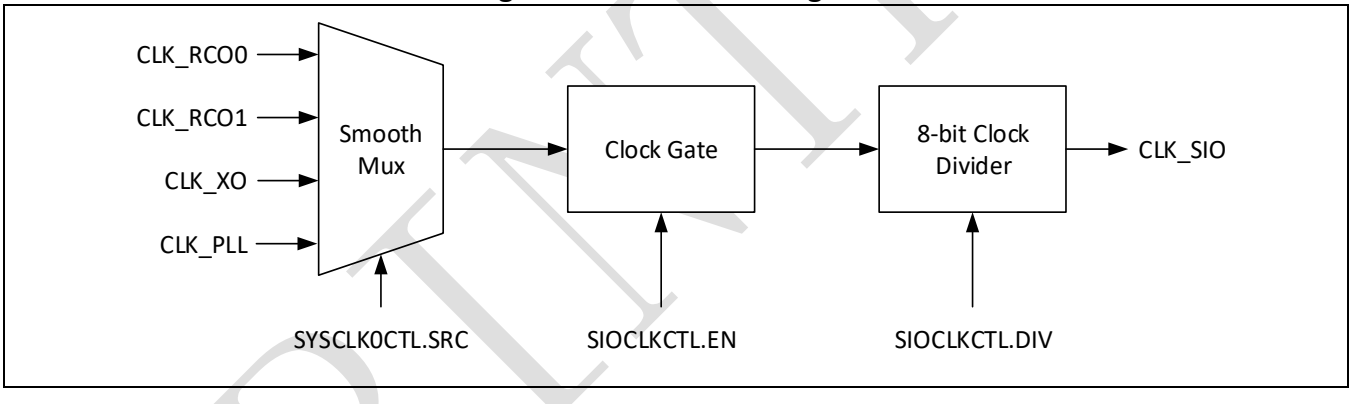
Figure 3-16: ECAP clock diagram



3.9.11 SIO clock

SIO clock is selected from the four root clocks, gated and divided down as shown in Figure 3-17. The maximum allowed frequency is 100MHz.

Figure 3-17: SIO clock diagram



3.10 Clock safety

The SPC2168 provides clock cross-detection circuits for clock safety concern. As shown in Figure 3-18, reference clock and detected clock are selected independently. Each of them will go through a binary divider to get the RCLK and DCLK. The RCLK is used to generate the time window, during which period the DCLK is counting. When the counting window is finished, the final value of DCLK counter is latched into CLKDETCNT register. The counted value is also compared with the high and low threshold given in CLKDETCTH register and the error status is latched into CLKIF.CLKDETERR if the value is out of the boundary. It further triggers a CPU interrupt or a PWM trip-zone event if as enabled by corresponding bit in CLKIE and CLKTZE registers. The DCLK can be brought out to GPIO11 by setting GPIO11.MUXSEL=3.

CLKDETCNT value is calculated as follows:

$$\text{CLKDETCNT} = \frac{f_{DCLK}}{f_{RCLK}} \times 65536$$

where f_{DCLK} and f_{RCLK} are the frequency of DCLK and RCLK separately, as shown in Figure 3-18.

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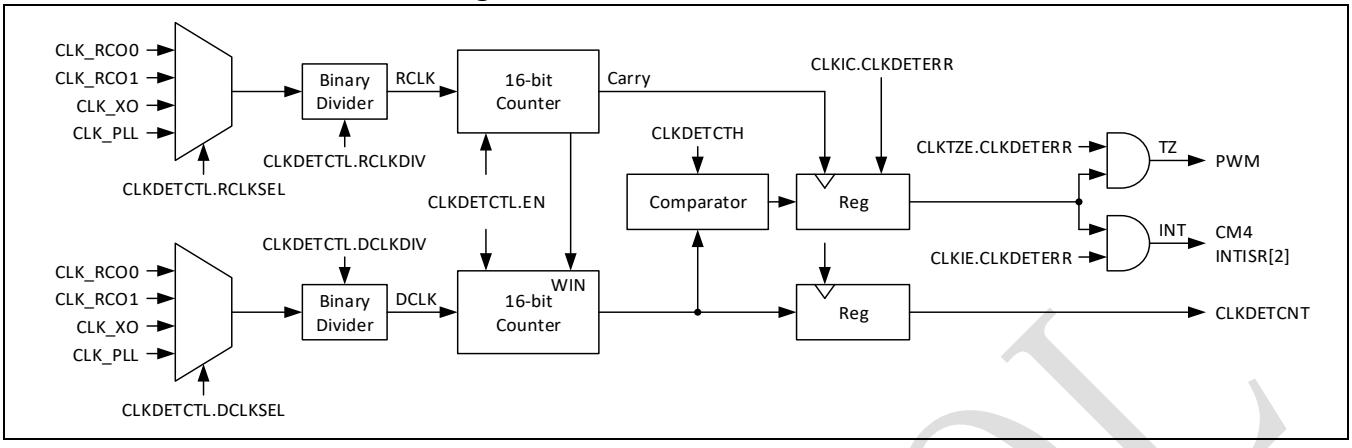
Figure 3-18: Clock cross-detection



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3.11 Registers

3.11.1 Clock register map

Table 3-4: CLOCK Module Base Address

Peripheral Module	Base Address
CLOCK	0x4000 0200

Table 3-5: CLOCK Register Map

Register	Offset	Description	Reset Value
CLKSTS	0x00	Clock Status Register	0x00000003
CLKREGCTL*	0x04	Clock Regulator Control Register	0x0000001C
RCO0CTL*	0x08	RCO0 Control Register	0x00000579
RCO1CTL*	0x0C	RCO1 Control Register	0x00000579
XOCTL*	0x10	Crystal Oscillator Control Register	0x00000FF2
PLLCTL0*	0x14	PLL Control Register 0	0x00000C40
PLLCTL1*	0x18	PLL Control Register 1	0x0C320000
CLKDETCTL*	0x1C	Clock Detection Control Register	0x00000000
CLKDETCTH*	0x20	Clock Detection Counter Threshold Register	0x00000000
CLKDETCNT	0x24	Clock Detection Counter Register	0x00000000
CLKIF	0x28	Clock Interrupt Flag Register	0x00000000
CLKIC	0x2C	Clock Interrupt Clear Register	0x00000000
CLKIE*	0x30	Clock Interrupt Enable Register	0x00000000
CLKTZE*	0x34	Clock Trip-zone Event Enable Register	0x00000000
SYSCLK0CTL*	0x38	SYSCLK0 Control Register	0x00000000
HCLKCTL*	0x3C	HCLK Control Register	0x00000000
ADCCLKCTL*	0x40	ADC Clock Control Register	0x00000000
PWMCLKCTL*	0x44	PWM Clock Control Register	0x00000000
ECAPCLKCTL*	0x48	ECAP Clock Control Register	0x00000000
TMR0CLKCTL*	0x4C	Timer 0 Clock Control Register	0x00000000
TMR1CLKCTL*	0x50	Timer 1 Clock Control Register	0x00000000
TMR2CLKCTL*	0x54	Timer 2 Clock Control Register	0x00000000
SIOCLKCTL*	0x58	SIO Clock Control Register	0x00000000
SYSCLK1CTL*	0x5C	SYSCLK1 Control Register	0x00000000
PCLKCTL*	0x60	PCLK Control Register	0x00000000
DGCLKCTL*	0x64	Deglitch Clock Control Register	0x00000200
UARTCLKCTL*	0x68	UART Clock Control Register	0x00000000
SSPCLKCTL*	0x6C	SSP Clock Control Register	0x00000000
I2CCLKCTL*	0x70	I2C Clock Control Register	0x00000000
WDT0CLKCTL*	0x74	WDT0 Clock Control Register	0x00000100
WDT1CLKCTL*	0x78	WDT1 Clock Control Register	0x00000300
CLKREGKEY	0x7C	Clock Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the CLKREGKEY=0x1ACCE551.

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3.11.2 Clock registers

3.11.2.1 Clock Status Register (CLKSTS)

Table 3-6: Clock Status Register (CLKSTS) Layout

CLKSTS (Clock Status Register) Offset: 0x0 Default: 0x00000003 Access: CLOCK -> CLKSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						CLKREGRDY	CLKDETERR
7	6	5	4	3	2	1	0
PLLSLOW	PLLFAST	VCOFREQVLD	VCOFREQ	PLLRDY	XORDY	RCO1RDY	RCO0RDY

Table 3-7: Clock Status Register (CLKSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9	CLKREGRDY	RO	0x0	Clock regulator ready indicator 0: Not ready 1: Ready
8	CLKDETERR	RO	0x0	Indicate error detected by CLKDET 0: No error is detected by CLKDET 1: Error has been detected by CLKDET
7	PLLSLOW	RO	0x0	Indicate PLL is unlocked and slower than expected. Possible reason can be: (1) Fin/NIN*NFB/65536 is higher than 600MHz (upper boundary of VCO free-run frequency) (2) VCO fails to oscillate (3) Malfunction of feedback divider so that there is no output or the equivalent dividing ratio is higher than expected 0: PLL is never too slow than expected 1: PLL is too slow than expected
6	PLLFAST	RO	0x0	Indicate PLL is unlocked and faster than expected. Possible reason can be: (1) Fin/NIN*NFB/65536 is lower than 400MHz (lower boundary of VCO free-run frequency) (2) The reference clock input is somehow missing (3) Malfunction of feedback divider so that the equivalent dividing ratio is lower than expected.

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Bits	Field Name	Type	Reset	Description
				0: PLL is never too fast than expected 1: PLL is too fast than expected
5	VCOFREQVLD	RO	0x0	VCOFREQ flag valid indicator 0: VCOFREQ is invalid 1: VCOFREQ is valid
4	VCOFREQ	RO	0x0	VCO frequency flag for trimming 0: VCO in PLL is too slow 1: VCO in PLL is too fast
3	PLLRDY	RO	0x0	PLL analog clock ready indicator 0: Not ready 1: Ready
2	XORDY	RO	0x0	XO clock ready indicator 0: Not ready 1: Ready
1	RCO1RDY	RO	0x1	RCO1 clock ready indicator 0: Not ready 1: Ready
0	RCO0RDY	RO	0x1	RCO0 clock ready indicator 0: Not ready 1: Ready

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3.11.2.2 Clock Regulator Control Register (CLKREGCTL)

Table 3-8: Clock Regulator Control Register (CLKREGCTL) Layout

CLKREGCTL (Clock Regulator Control Register) Offset: 0x4 Default: 0x0000001C Access: CLOCK -> CLKREGCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		VREFTRIM				USEADCBG	EN

Table 3-9: Clock Regulator Control Register (CLKREGCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5:2	VREFTRIM	RW	0x7	Reference voltage select 0000: 1.06V 0001: 1.08V 0010: 1.10V 0011: 1.12V 0100: 1.14V 0101: 1.16V 0110: 1.18V 0111: 1.20V 1000: 1.22V 1001: 1.24V 1010: 1.26V 1011: 1.28V 1100: 1.30V 1101: 1.32V 1110: 1.34V 1111: 1.36V
1	USEADCBG	RW	0x0	Use ADC bandgap to provide the bias current 0: Bias current is from system bandgap 1: Bias current is from ADC bandgap
0	EN	RW	0x0	Clock regulator enable 0: Disable 1: Enable

SPINTROL

3.11.2.3 RCO0 Control Register (RCO0CTL)

Table 3-10: RCO0 Control Register (RCO0CTL) Layout

RCO0CTL (RCO0 Control Register) Offset: 0x8 Default: 0x00000579 Access: CLOCK -> RCO0CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				LOCALREG	FREQTRIM		
7	6	5	4	3	2	1	0
FREQTRIM						LFMODE	EN

Table 3-11: RCO0 Control Register (RCO0CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11	LOCALREG	RW	0x0	Local clock regulator enable 0: RCO0 is powered by global 1.2V LDO 1: RCO0 is powered by local 1.2V clock regulator
10:2	FREQTRIM	RW	0x15E	RCO0 frequency trimming Frequency increases for larger code
1	LFMODE	RW	0x0	RCO0 low frequency mode 0: Normal 32MHz mode (Trimmed) 1: Low frequency mode at ~270kHz (Not trimmed)
0	EN	RW	0x1	RCO0 enable 0: Disable 1: Enable

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3.11.2.4 RCO1 Control Register (RCO1CTL)

Table 3-12: RCO1 Control Register (RCO1CTL) Layout

RCO1CTL (RCO1 Control Register) Offset: 0xC Default: 0x00000579 Access: CLOCK -> RCO1CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				LOCALREG	FREQTRIM		
7	6	5	4	3	2	1	0
FREQTRIM						LFMODE	EN

Table 3-13: RCO1 Control Register (RCO1CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11	LOCALREG	RW	0x0	Local clock regulator enable 0: RCO1 is powered by global 1.2V LDO 1: RCO1 is powered by local 1.2V clock regulator
10:2	FREQTRIM	RW	0x15E	RCO1 frequency trimming Frequency increases for larger code
1	LFMODE	RW	0x0	RCO1 low frequency mode 0: Normal 32MHz mode (Trimmed) 1: Low frequency mode at ~270kHz (Not trimmed)
0	EN	RW	0x1	RCO1 enable 0: Disable 1: Enable

SPINTROL

3.11.2.5 Crystal Oscillator Control Register (XOCTL)

Table 3-14: Crystal Oscillator Control Register (XOCTL) Layout

XOCTL (Crystal Oscillator Control Register) Offset: 0x10 Default: 0x00000FF2 Access: CLOCK -> XOCTL.all							
31	30	29	28	27	26	25	24
RESERVED_31_14							
23	22	21	20	19	18	17	16
RESERVED_31_14							
15	14	13	12	11	10	9	8
RESERVED_31_14		FEEDXIO	EXTRFB	PRECNT			
7	6	5	4	3	2	1	0
PRECNT				RESERVED_3_2		FASTEN	EN

Table 3-15: Crystal Oscillator Control Register (XOCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:14	RESERVED_31_14	RO	0x0	Reserved.
13	FEEDXIO	RW	0x0	External clock feed into XIO pin 0: External clock feed into XIN pin 1: External clock feed into XIO pin
12	EXTRFB	RW	0x0	Use external feedback resistor 0: Use internal feedback resistor 1: Use external feedback resistor
11:4	PRECNT	RW	0xFF	Pre-counted target value before XO clock is regarded as ready: Target = 1024 * PRECNT
3:2	RESERVED_3_2	RW	0x0	Reserved.
1	FASTEN	RW	0x1	Enable noise injection for fast startup 0: Disable 1: Enable
0	EN	RW	0x0	Crystal oscillator clock enable 0: Disable 1: Enable

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3.11.2.6 PLL Control Register 0 (PLLCTL0)

Table 3-16: PLL Control Register 0 (PLLCTL0) Layout

PLLCTL0 (PLL Control Register 0) Offset: 0x14 Default: 0x00000C40 Access: CLOCK -> PLLCTL0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
LOCALREG	USEADCBG	ICP					OPENLOOP
7	6	5	4	3	2	1	0
RCLKSELXO	VCOTRIM			FCALWIN	FCALEN	OE	EN

Table 3-17: PLL Control Register 0 (PLLCTL0) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	LOCALREG	RW	0x0	Local clock regulator enable 0: PLL is powered by global 1.2V LDO 1: PLL is powered by local 1.2V clock regulator
14	USEADCBG	RW	0x0	Use ADC bandgap to provide the bias current 0: Bias current is from system bandgap 1: Bias current is from ADC bandgap
13:9	ICP	RW	0x6	PLL charge pump current setting Must be set to 0.96*Fvco/Fpfd/(14-FREQTRIM)
8	OPENLOOP	RW	0x0	PLL open-loop mode (to trim vco) 0: Close loop 1: Open loop
7	RCLKSELXO	RW	0x0	PLL reference clock select 0: CLK_RCO0 (RC oscillator 0) 1: CLK_XO (Crystal oscillator)
6:4	VCOTRIM	RW	0x0	Should be always kept as 0
3	FCALWIN	RW	0x0	PLL frequency calibration time window For each calibration cycle, keep it as 1 until VCOFREQVLD=1 and release it as 0 0: Window is disabled 1: Window is enabled
2	FCALEN	RW	0x0	PLL frequency calibration enable 0: Disable 1: Enable
1	OE	RW	0x0	PLL digital clock output enable

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Disable 1: Enable
0	EN	RW	0x0	PLL enable 0: Disable 1: Enable

3.11.2.7 PLL Control Register 1 (PLLCTL1)

Table 3-18: PLL Control Register 1 (PLLCTL1) Layout

PLLCTL1 (PLL Control Register 1) Offset: 0x18 Default: 0x0C320000
Access: CLOCK -> PLLCTL1.all

31	30	29	28	27	26	25	24
RESERVED	NOUT				NIN		
23	22	21	20	19	18	17	16
NFB							
15	14	13	12	11	10	9	8
NFB							
7	6	5	4	3	2	1	0
NFB							

Table 3-19: PLL Control Register 1 (PLLCTL1) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:27	NOUT	RW	0x1	Set VCO to PLL output clock dividing ratio (Fvco/Fpll) to (NOUT+1)
26:24	NIN	RW	0x4	PLL input clock dividing ratio (Fin/Fpfd) 000: Invalid 001: Set to 1 if Fin(MHz) is in [4, 8]: Fin/Fpfd=1 010: Set to 2 if Fin(MHz) is in (8, 16): Fin/Fpfd=2 011: Set to 3 if Fin(MHz) is in (16, 24): Fin/Fpfd=3 100: Set to 4 if Fin(MHz) is in (24, 32): Fin/Fpfd=4 101: Set to 5 if Fin(MHz) is in (32, 40): Fin/Fpfd=5 110: Set to 6 if Fin(MHz) is in (40, 48): Fin/Fpfd=6 111: Set to 1 if Fin(MHz) is in (48, 56): Fin/Fpfd=7
23:0	NFB	RW	0x320000	Feedback dividing ratio (Fvco/Fpfd) scaled by 65536

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3.11.2.8 Clock Detection Control Register (CLKDETCTL)

Table 3-20: Clock Detection Control Register (CLKDETCTL) Layout

CLKDETCTL (Clock Detection Control Register) Offset: 0x1C Default: 0x00000000 Access: CLOCK -> CLKDETCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					EN	DCLKDIV	
7	6	5	4	3	2	1	0
DCLKDIV	DCLKSEL		RCLKDIV			RCLKSEL	

Table 3-21: Clock Detection Control Register (CLKDETCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	EN	RW	0x0	Clock detection enable When disabled, the interrupts and the clock error events will be cleared 0: Disable clock detection 1: Enable clock detection
9:7	DCLKDIV	RW	0x0	Detected clock dividing ratio 000: Divide by 1 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 101: Divide by 32 110: Divide by 64 111: Divide by 128
6:5	DCLKSEL	RW	0x0	Detected clock select 00: CLK_RCO0 01: CLK_RCO1 10: CLK_XO 11: CLK_PLL
4:2	RCLKDIV	RW	0x0	Reference clock dividing ratio 000: Divide by 1 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 101: Divide by 32

SPINTROL

Bits	Field Name	Type	Reset	Description
				110: Divide by 64 111: Divide by 128
1:0	RCLKSEL	RW	0x0	Reference clock select 00: CLK_RCO0 01: CLK_RCO1 10: CLK_XO 11: CLK_PLL

3.11.2.9 Clock Detection Counter Threshold Register (CLKDETCTH)

Table 3-22: Clock Detection Counter Threshold Register (CLKDETCTH) Layout

CLKDETCTH (Clock Detection Counter Threshold Register) Offset: 0x20 Default: 0x00000000 Access: CLOCK -> CLKDETCTH.all							
31	30	29	28	27	26	25	24
HI							
23	22	21	20	19	18	17	16
HI							
15	14	13	12	11	10	9	8
LO							
7	6	5	4	3	2	1	0
LO							

Table 3-23: Clock Detection Counter Threshold Register (CLKDETCTH) Field Description

Bits	Field Name	Type	Reset	Description
31:16	HI	RW	0x0	Upper counter threshold for clock detect If the final counter value > HI, a trip-zone event will be generated for PWM
15:0	LO	RW	0x0	Lower counter threshold for clock detect If the final counter value < LO, a trip-zone event will be generated for PWM

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3.11.2.10 Clock Detection Counter Register (CLKDETCNT)

Table 3-24: Clock Detection Counter Register (CLKDETCNT) Layout

CLKDETCNT (Clock Detection Counter Register) Offset: 0x24 Default: 0x00000000 Access: CLOCK -> CLKDETCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 3-25: Clock Detection Counter Register (CLKDETCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Final counter value of the clock detect

SPINTROL

3.11.2.11 Clock Interrupt Flag Register (CLKIF)

Table 3-26: Clock Interrupt Flag Register (CLKIF) Layout

CLKIF (Clock Interrupt Flag Register) Offset: 0x28 Default: 0x00000000 Access: CLOCK -> CLKIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					CLKINT	CLKDETERR	PLLUNLOCK

Table 3-27: Clock Interrupt Flag Register (CLKIF) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	CLKINT	RO	0x0	Latched clock interrupt 0: No clock interrupt occurred 1: Clock interrupt occurred Further interrupt will not be generated until this bit is cleared.
1	CLKDETERR	RO	0x0	Latched CLKDET error flag, namely the CLKDETCNT is out of the range defined by CLKDETCTH 0: CLKDETCNT is within the expected range 1: CLKDETCNT is out of the expected range Further event will not generate interrupt until this bit is cleared
0	PLLUNLOCK	RO	0x0	Latched PLL unlock flag Detailed reason can be referred to CLKSTS.PLLFAST and CLKSTS.PLLSLOW 0: PLL is locked 1: PLL is unlocked Further event will not generate interrupt until this bit is cleared

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3.11.2.12 Clock Interrupt Clear Register (CLKIC)

Table 3-28: Clock Interrupt Clear Register (CLKIC) Layout

CLKIC (Clock Interrupt Clear Register) Offset: 0x2C Default: 0x00000000 Access: CLOCK -> CLKIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					CLKINT	CLKDETERR	PLLUNLOCK

Table 3-29: Clock Interrupt Clear Register (CLKIC) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	CLKINT	W1C	0x0	Clock interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the CLKIF.CLKINT This bit is self-cleared to 0.
1	CLKDETERR	W1C	0x0	CLKDET error interrupt flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the CLKIF.CLKDETERR This bit is self-cleared to 0.
0	PLLUNLOCK	W1C	0x0	PLL unlock interrupt flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clear the CLKIF.PLLUNLOCK, CLKSTS.PLLFAST, CLKSTS.PLLSLOW. This bit is self-cleared to 0.

SPINTROL

3.11.2.13 Clock Interrupt Enable Register (CLKIE)

Table 3-30: Clock Interrupt Enable Register (CLKIE) Layout

CLKIE (Clock Interrupt Enable Register) Offset: 0x30 Default: 0x00000000 Access: CLOCK -> CLKIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED						CLKDETERR	PLLUNLOCK

Table 3-31: Clock Interrupt Enable Register (CLKIE) Field Description

Bits	Field Name	Type	Reset	Description
31:2	RESERVED_31_2	RO	0x0	Reserved
1	CLKDETERR	RW	0x0	CLKDET error interrupt enable 0: CLKDET error will not trigger clock interrupt 1: CLKDET error triggers clock interrupt
0	PLLUNLOCK	RW	0x0	PLL unlock interrupt enable 0: PLL unlock will not trigger clock interrupt 1: PLL unlock triggers clock interrupt

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3.11.2.14 Clock Trip-Zone Event Enable Register (CLKTZE)

Table 3-32: Clock Trip-Zone Event Enable Register (CLKTZE) Layout

CLKTZE (Clock Trip-zone Event Enable Register) Offset: 0x34 Default: 0x00000000 Access: CLOCK -> CLKTZE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED						CLKDETERR	PLLUNLOCK

Table 3-33: Clock Trip-Zone Event Enable Register (CLKTZE) Field Description

Bits	Field Name	Type	Reset	Description
31:2	RESERVED_31_2	RO	0x0	Reserved
1	CLKDETERR	RW	0x0	CLKDET error trip-zone event enable 0: CLKDET error will not trigger PWM trip-zone 1: CLKDET error triggers PWM trip-zone
0	PLLUNLOCK	RW	0x0	PLL unlock trip-zone event enable 0: PLL unlock will not trigger PWM trip-zone 1: PLL unlock triggers PWM trip-zone

SPINTROL

3.11.2.15 SYSCLK0 Control Register (SYSCLK0CTL)

Table 3-34: SYSCLK0 Control Register (SYSCLK0CTL) Layout

SYSCLK0CTL (SYSCLK0 Control Register) Offset: 0x38 Default: 0x00000000 Access: CLOCK -> SYSCLK0CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					SRC		RESERVED
7	6	5	4	3	2	1	0
RESERVED							

Table 3-35: SYSCLK0 Control Register (SYSCLK0CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10:9	SRC	RW	0x0	Clock source select 00: RCO0 01: RCO1 10: XO 11: PLL
8:0	RESERVED_8_0	RO	0x0	Reserved

3.11.2.16 HCLK Control Register (HCLKCTL)

Table 3-36: HCLK Control Register (HCLKCTL) Layout

HCLKCTL (HCLK Control Register) Offset: 0x3C Default: 0x00000000 Access: CLOCK -> HCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
DIV							

Table 3-37: HCLK Control Register (HCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:0	DIV	RW	0x0	Clock dividing ratio from system clock is (DIV+1)

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3.11.2.17 ADC Clock Control Register (ADCCLKCTL)

Table 3-38: ADC Clock Control Register (ADCCLKCTL) Layout

ADCCLKCTL (ADC Clock Control Register) Offset: 0x40 Default: 0x00000000 Access: CLOCK -> ADCCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-39: ADC Clock Control Register (ADCCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

3.11.2.18 PWM Clock Control Register (PWMCLKCTL)

Table 3-40: PWM Clock Control Register (PWMCLKCTL) Layout

PWMCLKCTL (PWM Clock Control Register) Offset: 0x44 Default: 0x00000000 Access: CLOCK -> PWMCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-41: PWM Clock Control Register (PWMCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

SPINTROL

3.11.2.19 ECAP Clock Control Register (ECAPCLKCTL)

Table 3-42: ECAP Clock Control Register (ECAPCLKCTL) Layout

ECAPCLKCTL (ECAP Clock Control Register) Offset: 0x48 Default: 0x00000000 Access: CLOCK -> ECAPCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-43: ECAP Clock Control Register (ECAPCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

3.11.2.20 Timer 0 Clock Control Register (TMR0CLKCTL)

Table 3-44: Timer 0 Clock Control Register (TMR0CLKCTL) Layout

TMR0CLKCTL (Timer 0 Clock Control Register) Offset: 0x4C Default: 0x00000000 Access: CLOCK -> TMR0CLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-45: Timer 0 Clock Control Register (TMR0CLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

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3.11.2.21 Timer 1 Clock Control Register (TMR1CLKCTL)

Table 3-46: Timer 1 Clock Control Register (TMR1CLKCTL) Layout

TMR1CLKCTL (Timer 1 Clock Control Register) Offset: 0x50 Default: 0x00000000 Access: CLOCK -> TMR1CLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-47: Timer 1 Clock Control Register (TMR1CLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

3.11.2.22 Timer 2 Clock Control Register (TMR2CLKCTL)

Table 3-48: Timer 2 Clock Control Register (TMR2CLKCTL) Layout

TMR2CLKCTL (Timer 2 Clock Control Register) Offset: 0x54 Default: 0x00000000 Access: CLOCK -> TMR2CLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-49: Timer 2 Clock Control Register (TMR2CLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

SPINTROL

3.11.2.23 SIO Clock Control Register (SIOCLKCTL)

Table 3-50: SIO Clock Control Register (SIOCLKCTL) Layout

SIOCLKCTL (SIO Clock Control Register) Offset: 0x58 Default: 0x00000000 Access: CLOCK -> SIOCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-51: SIO Clock Control Register (SIOCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

3.11.2.24 SYSCLK1 Control Register (SYSCLK1CTL)

Table 3-52: SYSCLK1 Control Register (SYSCLK1CTL) Layout

SYSCLK1CTL (SYSCLK1 Control Register) Offset: 0x5C Default: 0x00000000 Access: CLOCK -> SYSCLK1CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					SRC		RESERVED
7	6	5	4	3	2	1	0
RESERVED							

Table 3-53: SYSCLK1 Control Register (SYSCLK1CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10:9	SRC	RW	0x0	Clock source select 00: RCO0 01: RCO1 10: XO 11: PLL
8:0	RESERVED_8_0	RO	0x0	Reserved

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3.11.2.25 PCLK Control Register (PCLKCTL)

Table 3-54: PCLK Control Register (PCLKCTL) Layout

PCLKCTL (PCLK Control Register) Offset: 0x60 Default: 0x00000000 Access: CLOCK -> PCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
DIV							

Table 3-55: PCLK Control Register (PCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:0	DIV	RW	0x0	Clock dividing ratio from system clock is (DIV+1)

3.11.2.26 Deglitch Clock Control Register (DGCLKCTL)

Table 3-56: Deglitch Clock Control Register (DGCLKCTL) Layout

DGCLKCTL (Deglitch Clock Control Register) Offset: 0x64 Default: 0x00000200 Access: CLOCK -> DGCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					PDIV		
7	6	5	4	3	2	1	0
DIV							

Table 3-57: Deglitch Clock Control Register (DGCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10:8	PDIV	RW	0x2	Clock binary pre-dividing ratio from system clock 000: Divide by 1 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 101: Divide by 32 110: Divide by 64 111: Divide by 128
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

SPINTROL

3.11.2.27 UART Clock Control Register (UARTCLKCTL)

Table 3-58: UART Clock Control Register (UARTCLKCTL) Layout

UARTCLKCTL (UART Clock Control Register) Offset: 0x68 Default: 0x00000000 Access: CLOCK -> UARTCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-59: UART Clock Control Register (UARTCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

3.11.2.28 SSP Clock Control Register (SSPCLKCTL)

Table 3-60: SSP Clock Control Register (SSPCLKCTL) Layout

SSPCLKCTL (SSP Clock Control Register) Offset: 0x6C Default: 0x00000000 Access: CLOCK -> SSPCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							EN
15	14	13	12	11	10	9	8
DIV							
7	6	5	4	3	2	1	0
DIV							

Table 3-61: SSP Clock Control Register (SSPCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:17	RESERVED_31_17	RO	0x0	Reserved
16	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
15:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

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3.11.2.29 I2C Clock Control Register (I2CCLKCTL)

Table 3-62: I2C Clock Control Register (I2CCLKCTL) Layout

I2CCLKCTL (I2C Clock Control Register) Offset: 0x70 Default: 0x00000000 Access: CLOCK -> I2CCLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							EN
7	6	5	4	3	2	1	0
DIV							

Table 3-63: I2C Clock Control Register (I2CCLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	EN	RW	0x0	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

SPINTROL

3.11.2.30 WDT0 Clock Control Register (WDT0CLKCTL)

Table 3-64: WDT0 Clock Control Register (WDT0CLKCTL) Layout

WDT0CLKCTL (WDT0 Clock Control Register) Offset: 0x74 Default: 0x00000100 Access: CLOCK -> WDT0CLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					SRC		EN
7	6	5	4	3	2	1	0
DIV							

Table 3-65: WDT0 Clock Control Register (WDT0CLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10:9	SRC	RW	0x0	Clock source select 00: RCO0 01: RCO1 10: XO 11: PLL
8	EN	RW	0x1	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

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3.11.2.31 WDT1 Clock Control Register (WDT1CLKCTL)

Table 3-66: WDT1 Clock Control Register (WDT1CLKCTL) Layout

WDT1CLKCTL (WDT1 Clock Control Register) Offset: 0x78 Default: 0x00000300 Access: CLOCK -> WDT1CLKCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					SRC		EN
7	6	5	4	3	2	1	0
DIV							

Table 3-67: WDT1 Clock Control Register (WDT1CLKCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10:9	SRC	RW	0x1	Clock source select 00: RCO0 01: RCO1 10: XO 11: PLL
8	EN	RW	0x1	Clock output enable 0: Disable clock output 1: Enable clock output
7:0	DIV	RW	0x0	Clock dividing ratio is (DIV+1)

3.11.2.32 Clock Register Write-Allow Key Register (CLKREGKEY)

Table 3-68: Clock Register Write-Allow Key Register (CLKREGKEY) Layout

CLKREGKEY (Clock Register Write-Allow Key Register) Offset: 0x7C Default: 0x1ACCE551 Access: CLOCK -> CLKREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 3-69: Clock Register Write-Allow Key Register (CLKREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected clock registers

SPINTROL

4 General-purpose I/O (GPIO)

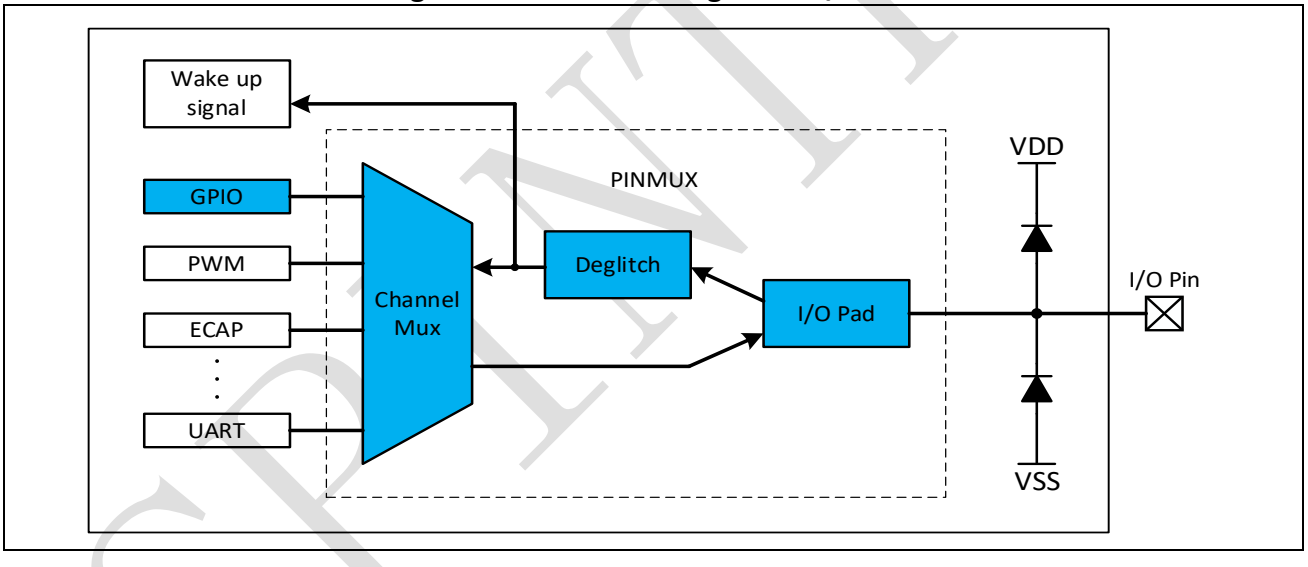
4.1 Overview

The SPC2168 provides 61 I/O pins, while the BOOT pin can be used as GPIO47 with several limitations. These I/O pins are multiplexed so that they can be configured as either general-purpose I/Os or any one of the alternative functions. Each I/O pin can be programmed and used independently.

This chapter describes the detailed I/O control, including pin multiplexing and GPIO-related functions. Figure 4-1 is the structure diagram of the I/O control, which consists of two parts:

- PINMUX module
  - I/O Pad: Pull-up/pull-down control, input/output control, Schmitt input control and output driving strength control
  - Deglitch: Input deglitch control
  - MUX: Pin multiplexing
- GPIO module
  - GPIO function IP control

Figure 4-1: Structure diagram of I/O control



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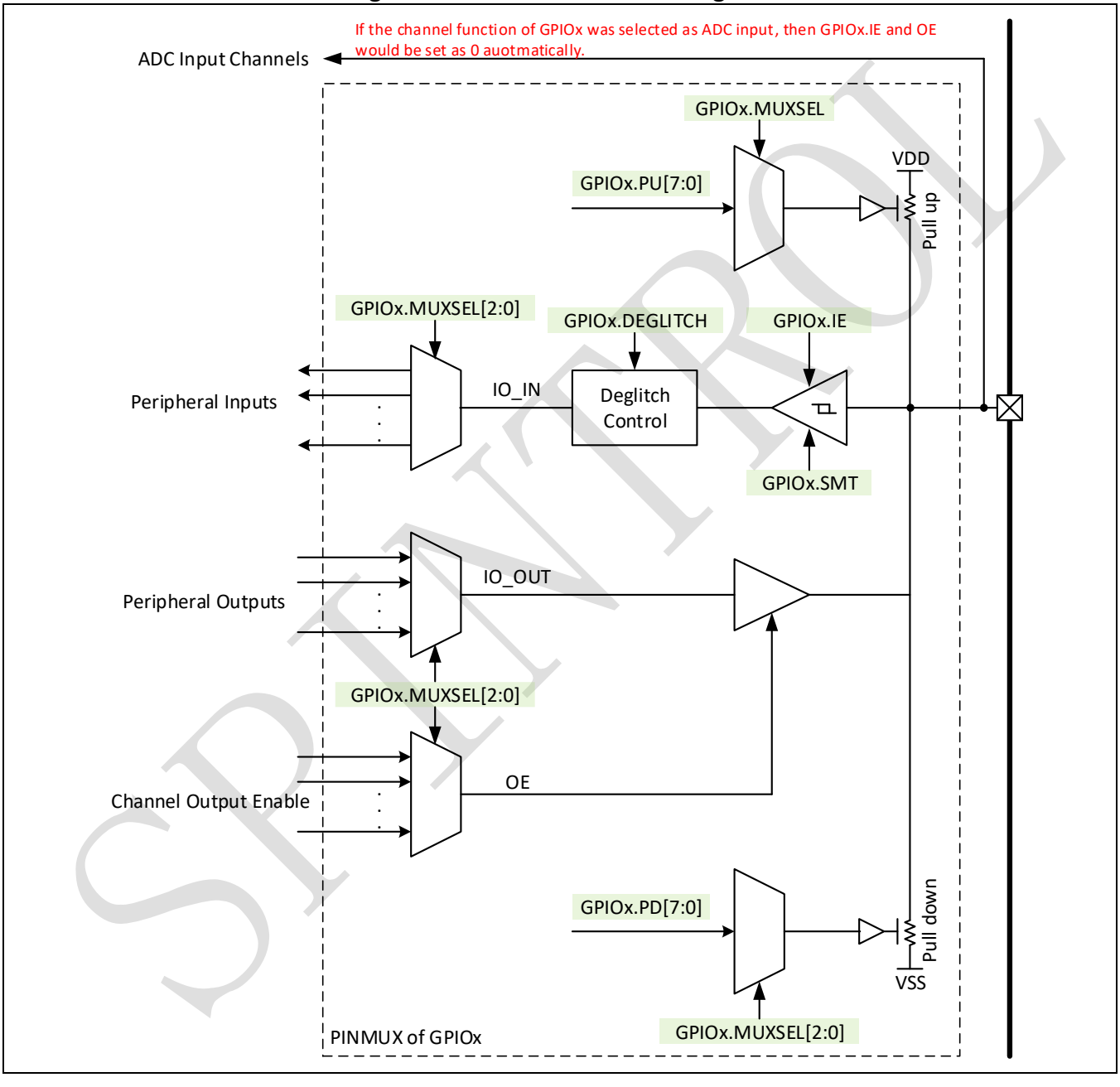
4.2 Pin multiplexing (PINMUX)

Figure 4-2 is the structure diagram of the PINMUX. Multiplexers are used for each I/O pin to support overall 8 function channels. The function channel can be either input or output. If the I/O pin is used as input, the output buffer will be disabled and set into high-impedance state. The input signal can also pass through a Schmitt trigger or a re-sampling block to suppress the possible glitches.

Figure 4-2: PINMUX structure diagram



Note: If the channel of the GPIOx selects the ADC input function, then GPIOx.IE is set to 0 and the output function is turned off.
When GPIO20, GPIO21 are configured to XIN and XOUT, the external crystal and the internal clock circuit are directly connected, and there is no input-output relationship in Figure 4-2.

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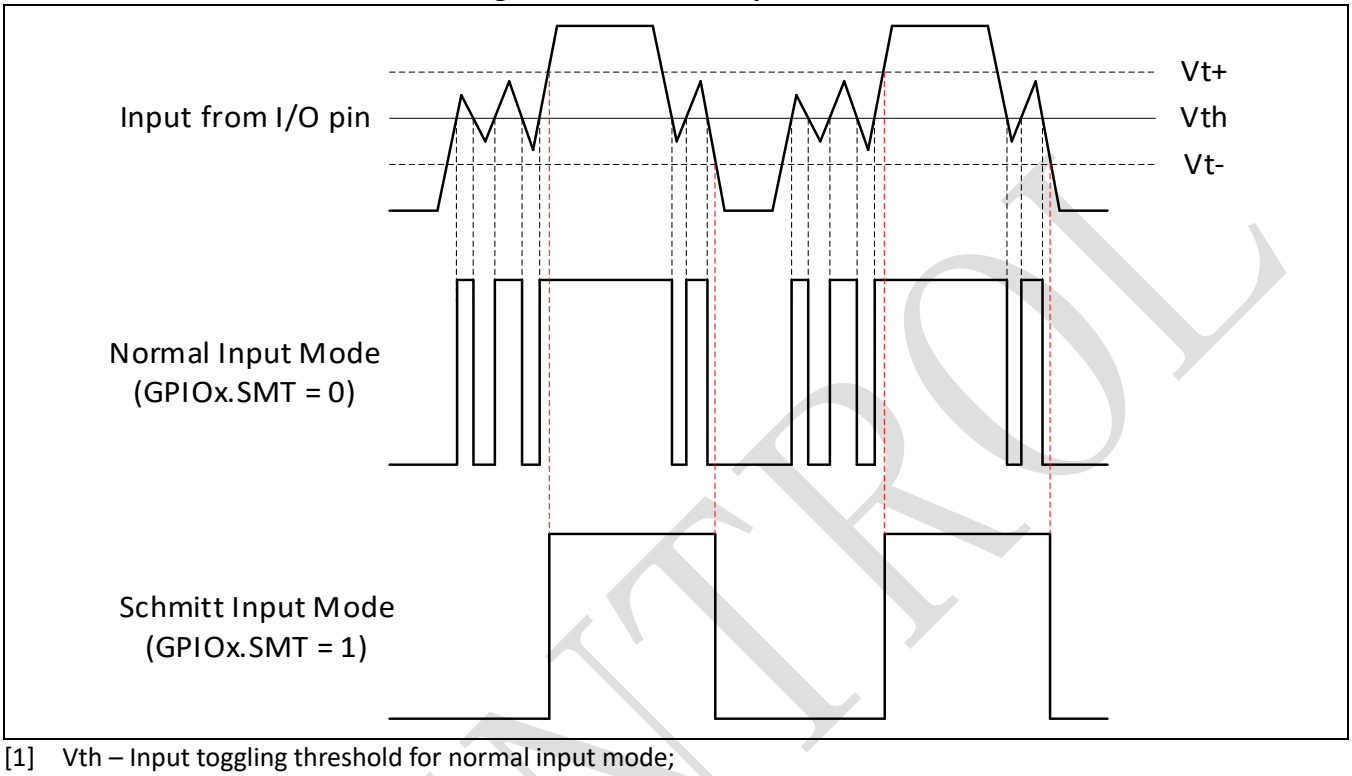
4.2.1 Schmitt control

The Schimtt input mode can be enabled by setting register GPIOx.SMT. As shown in Figure 4-3, Schmitt input mode can prevent false triggering due to small noise fluctuations (noise) on the input.

Figure 4-3: Schmitt input mode

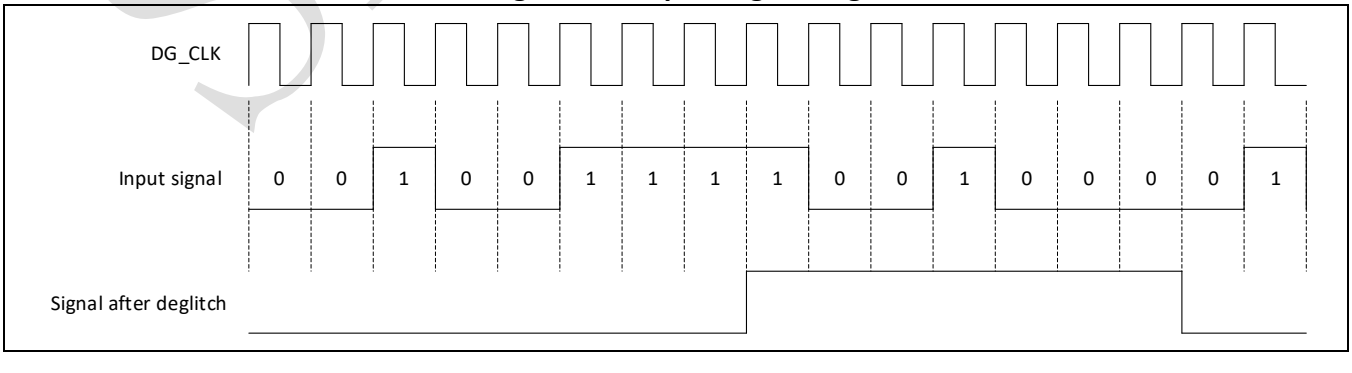


[1] Vth – Input toggling threshold for normal input mode;
[2] Vt+ - Input upper toggling threshold for Schmitt input mode; Vt- - Input lower toggling threshold for Schmitt input mode;
[3] Typically, Vth = 1.5V, Vt+ = 1.67V, Vt- = 1.38V.

4.2.2 Deglitch control

The input deglitching can be enabled by setting register GPIOx.DEGLITCH. Figure 4-4 shows the principle of input deglitching. When the input signal of the Deglitch module remains a value unchanged for 3 consecutive DG_CLK cycles, the output of the Deglitch module will change to this value, otherwise the output of the Deglitch module remains the original value.

Figure 4-4: Input deglitching



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4.2.3 I/O alternate functions

The channel function for all the I/O pins are summarized in Table 4-1.

Table 4-1: I/O function channel definition

Name	Channel (Default channel is highlight in red)							
	0	1	2	3	4	5	6	7
GPIO0	GPIO0	**ADC0**	COMP0H				SIO0_0	ECAPO
GPIO1	GPIO1	**ADC1**	COMP0L				SIO0_1	ECAPO
GPIO2	GPIO2	**ADC2**	COMP1H				SIO0_2	ECAPO
GPIO3	GPIO3	**ADC3**	COMP1L				SIO0_3	ECAPO
GPIO4	GPIO4	**ADC4**	COMP2H				SIO0_4	ECAPO
GPIO5	GPIO5	**ADC5**	COMP2L				SIO0_5	ECAPO
GPIO6	GPIO6	**ADC6**					SIO0_6	ECAPO
GPIO7	GPIO7	**ADC7**					SIO0_7	ECAPO
GPIO8	GPIO8	**ADC8**					SIO0_8	ECAPO
GPIO9	GPIO9	**ADC9**					SIO0_9	ECAPO
GPIO10	GPIO10	**ADC10**	COMP3H				SIO0_10	ECAPO
GPIO11	GPIO11	**ADC11**	COMP3L	DCLK			SIO0_11	ECAPO
GPIO12	GPIO12	**ADC12**	COMP4H				SIO0_12	ECAPO
GPIO13	GPIO13	**ADC13**	COMP4L				SIO0_13	ECAPO
GPIO14	GPIO14	**ADC14**	COMP5H				SIO0_14	ECAPO
GPIO15	GPIO15	**ADC15**	COMP5L				SIO0_15	ECAPO
GPIO16	GPIO16	**ADC16**	COMP6H				SIO0_16	ECAPO
GPIO17	GPIO17	**ADC17**	COMP6L				SIO0_17	ECAPO
GPIO18	GPIO18	**ADC18**	COMP7H				SIO0_0	ECAPO
GPIO19	GPIO19	**ADC19**	COMP7L				SIO0_1	ECAPO
GPIO20	**GPIO20**	XIN	SPI_SCLK	I2C_SCL	UART_TXD	PWMSYNCO	SIO0_2	ECAPO
GPIO21	**GPIO21**	XIO	SPI_SFRM	I2C_SDA	UART_RXD	PWMSOC	SIO0_3	ECAPO
GPIO22	**GPIO22**		SPI_MOSI	SPI_MISO			SIO0_4	ECAPO
GPIO23	**GPIO23**		SPI_MISO	SPI_MOSI			SIO0_5	ECAPO
GPIO24	**GPIO24**		COMP0H		PWM1A	PWM1A	SIO0_6	ECAPO
GPIO25	**GPIO25**		COMP0L		PWM2A	PWM1B	SIO0_7	ECAPO
GPIO26	**GPIO26**		COMP1H		PWM3A	PWM2A	SIO1_0	ECAPO
GPIO27	**GPIO27**		COMP1L		PWM1B	PWM2B	SIO1_1	ECAPO
GPIO28	**GPIO28**		COMP2H		PWM2B	PWM3A	SIO1_2	ECAPO
GPIO29	**GPIO29**		COMP2L		PWM3B	PWM3B	SIO1_3	ECAPO
GPIO30	**GPIO30**	I2C_SCL					SIO1_4	ECAPO
GPIO31	**GPIO31**	I2C_SDA					SIO1_5	ECAPO
GPIO32	**GPIO32**		COMP3H	PWMSYNCO	PWM4A	PWM4A	SIO1_6	ECAPO
GPIO33	**GPIO33**		COMP3L	PWMSOC	PWM5A	PWM4B	SIO1_7	ECAPO
GPIO34	**GPIO34**		COMP4H	PWM0A	PWM6A	PWM5A	SIO1_8	ECAPO
GPIO35	**GPIO35**		COMP4L	PWM0B	PWM4B	PWM5B	SIO1_9	ECAPO

SPINTROL

Name	Channel (Default channel is highlight in red)							
	0	1	2	3	4	5	6	7
GPIO36	GPIO36		COMP5H	PWM7A	PWM5B	PWM6A	SIO1_10	ECAPO
GPIO37	GPIO37		COMP5L	PWM7B	PWM6B	PWM6B	SIO1_11	ECAPO
GPIO38	GPIO38	SPI_SCLK	UART_TXD	UART_RXD	PWMSOCA		SIO1_12	ECAPO
GPIO39	GPIO39	SPI_SFRM	UART_RXD	UART_TXD	PWMSOCB		SIO1_13	ECAPO
GPIO40	GPIO40	SPI_MOSI	SPI_MISO	I2C_SCL	PWMSOCC		SIO1_14	ECAPO
GPIO41	GPIO41	SPI_MISO	SPI_MOSI	I2C_SDA	PWMSYNCO		SIO1_15	ECAPO
GPIO42	GPIO42	I2C_SCL		COMP6H	SPI_SCLK		SIO1_16	ECAPO
GPIO43	GPIO43	I2C_SDA		COMP6L	SPI_SFRM		SIO1_17	ECAPO
GPIO44	GPIO44	UART_TXD	UART_RXD	COMP7H	SPI_MOSI	SPI_MISO	SIO2_0	ECAPO
GPIO45	GPIO45	UART_RXD	UART_TXD	COMP7L	SPI_MISO	SPI_MOSI	SIO2_1	ECAPO
GPIO46	GPIO46						SIO2_2	ECAPO
GPIO47	GPIO47						SIO2_3	ECAPO
GPIO48	GPIO48	TCK/SWCK			COMP0H	COMP3H	SIO2_4	ECAPO
GPIO49	GPIO49	TMS/SWD			COMP0L	COMP3L	SIO2_5	ECAPO
GPIO50	GPIO50	TDI	CAU_SWCK		COMP1H	COMP4H	SIO2_6	ECAPO
GPIO51	GPIO51	TDO	CAU_SWD		COMP1L	COMP4L	SIO2_7	ECAPO
GPIO52	GPIO52			PWM0A	COMP2H	COMP5H	SIO2_8	ECAPO
GPIO53	GPIO53			PWM0B	COMP2L	COMP5L	SIO2_9	ECAPO
GPIO54	GPIO54			PWM7A	PWM4A	PWM4A	SIO2_10	ECAPO
GPIO55	GPIO55			PWM7B	PWM5A	PWM4B	SIO2_11	ECAPO
GPIO56	GPIO56				PWM4A	PWM4A	SIO2_12	ECAPO
GPIO57	GPIO57				PWM5A	PWM4B	SIO2_13	ECAPO
GPIO58	GPIO58				PWM6A	PWM5A	SIO2_14	ECAPO
GPIO59	GPIO59				PWM4B	PWM5B	SIO2_15	ECAPO
GPIO60	GPIO60				PWM5B	PWM6A	SIO2_16	ECAPO
GPIO61	GPIO61				PWM6B	PWM6B	SIO2_17	ECAPO

[1] NOTE: GPIO47 is a BOOT pin and must not be configured for any other function during the chip startup phase, otherwise it will result in a constant level on GPIO47, which will affect the entry of ISP mode or Flash startup mode.

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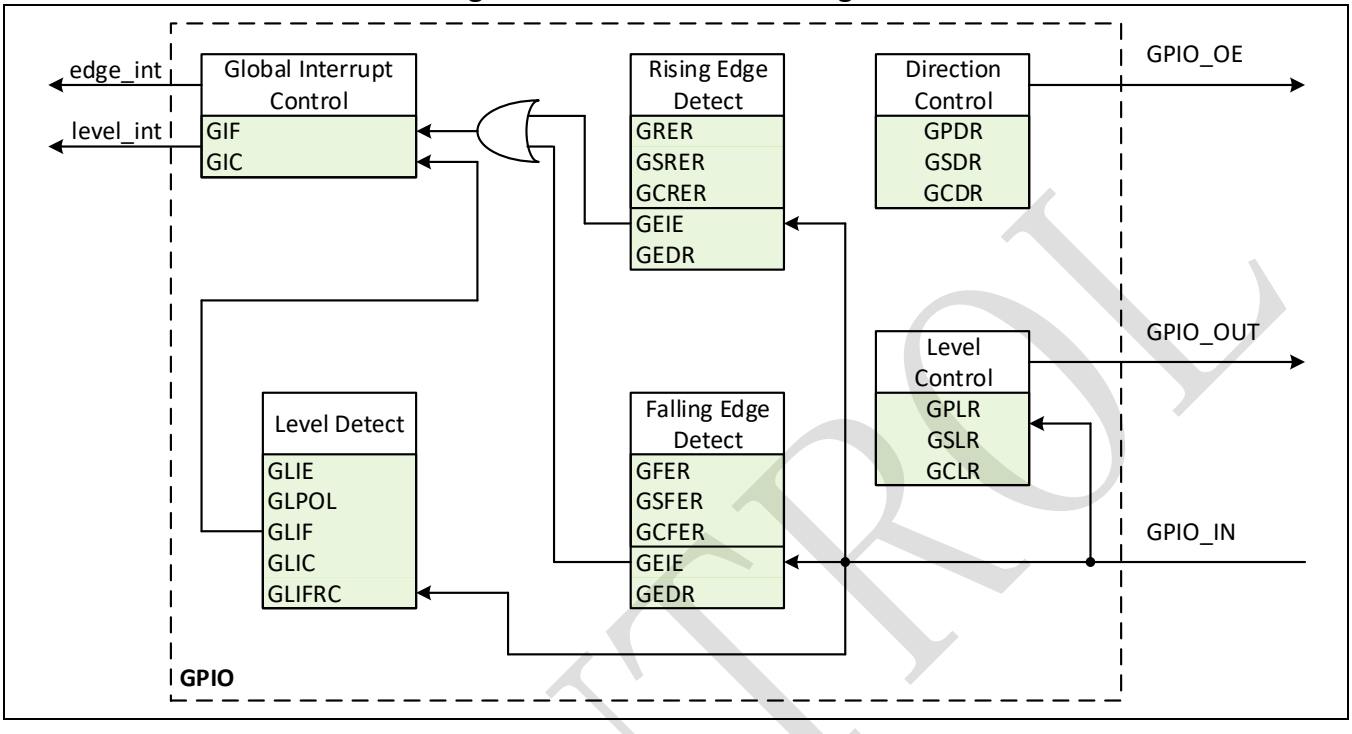
4.3 GPIO function IP (GPIO)

Figure 4-5 is the structure diagram of the GPIO.

Figure 4-5: GPIO structure diagram



The GPIO ports are mapped to two groups: GPIO_PORT0 and GPIO_PORT1. Each group is 32 bits width and support bitwise control, but only low 30 bits are used in GPIO_PORT1.

All the GPIO pins are inputs by default. The direction of the GPIO pins is configured by programming the GPIO Pin Direction Register (GPDR0 / GPDR1) or GPIO Set Direction Register (GSDR0 / GSDR1) or GPIO Clear Direction Register (GCDR0 / GCDR1). GSDR and GCDR are bitwise registers, and for each bit in these registers, writing 0 has no effect.

When configured as output pin, programming GPIO Pin Level Register (GPLR0 / GPLR1) or GPIO Set Level Register (GSLR0 / GSLR1) or GPIO Clear Level Register (GCLR0 / GCLR1) determines the GPIO output port status. GSLR and GCLR are bitwise registers, and for each bit in these registers, writing 0 has no effect.

Note: No matter what has been written to GPLR register or GPDR register, readback from GPLR will always reflect the GPIO ports staus, i.e. the status of I/O pads.

4.3.1 GPIO edge-triggered interrupt

Edge detect module will run when GPIO Rising-edge Detect Enable Register (GRER0 / GRER1) or GPIO Falling-edge Detect Enable Register (GFER0 / GFER1) is set. GSRER, GCRER, GSFER and GCFER are bitwise registers, and for each bit in these registers, writing 0 has no effect.

GPIO Edge Detect Register (GEDR0 / GEDR1) will show the edge detect results. Writing GEDR bit with 1 will clear the associated bit edge detect flag and writing 0 has no effect. The edge event is detected by APB clock synchronize GPIO inputs.

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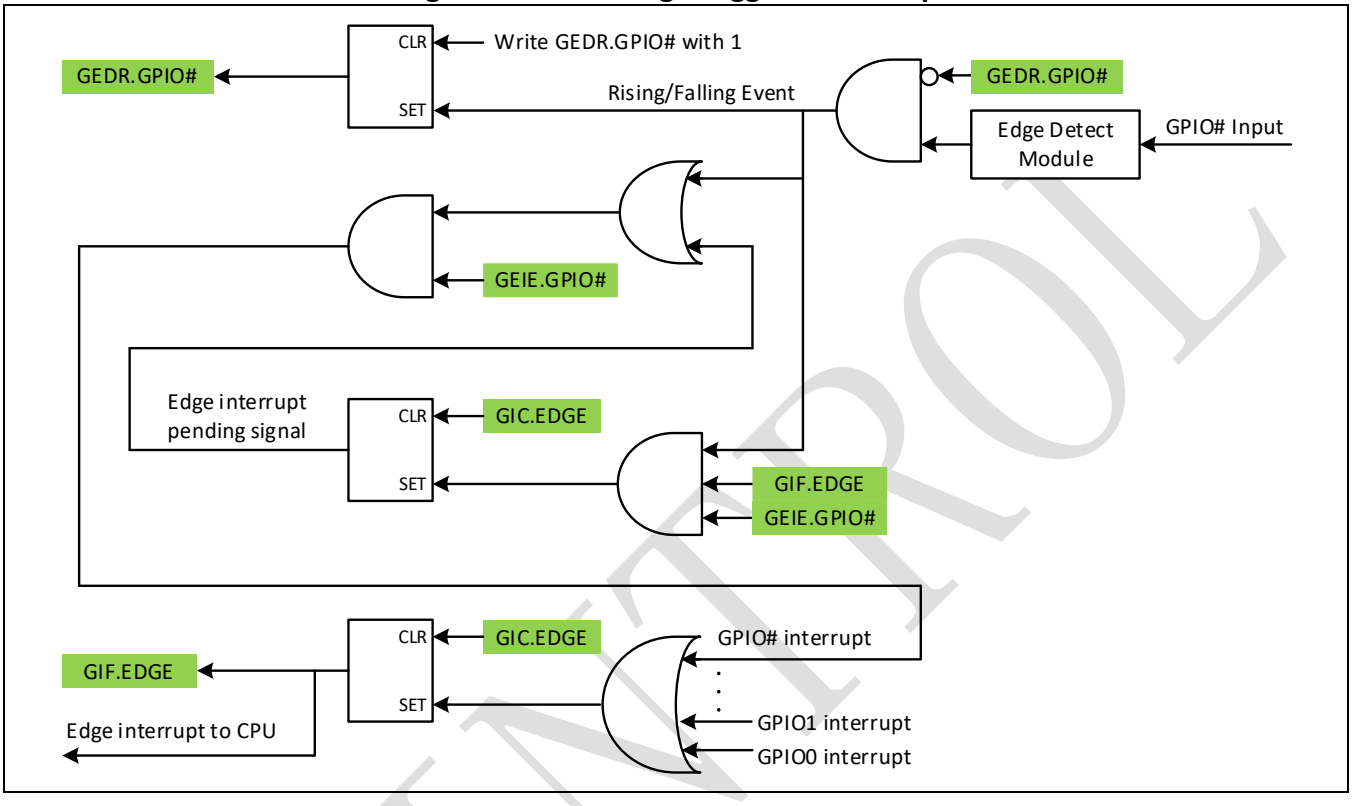
The GPIO edge detect interrupt to CPU will be triggered and the edge detect interrupt flag in GPIO Interrupt Flag Register (GIF.EDGE) will be set if the associated GPIO Edge Interrupt Enable Register (GEIE0 / GEIE1) bit and GEDR bit are all HIGH, as shown in Figure 4-6. Writing 1 to GIC.EDGE will clear the GPIO edge-triggered interrupt flag.

Figure 4-6: GPIO edge-triggered interrupt



If GIF.EDGE is HIGH, another GPIO pin edge detect event has occurred and its associated bit in GEDR is LOW at present, this will cause edge detect interrupt pending issue. The pending GPIO edge detect interrupt will be released after GIF.EDGE is cleared, and program will enter ISR again for the pending interrupt request. However, if the GPIO pin has been edge-triggered and its associated bit in GEDR is HIGH at present, this pin's event will not trigger interrupt or interrupt pending issue to CPU. Therefore, the program should clear both GEDR and GIF.EDGE before exiting ISR.

4.3.2 GPIO level-triggered interrupt

GPIO level detect module will run when GPIO Level Interrupt Enable Register (GLIE0 / GLIE1) is enabled. Before setting GLIE, GPIO level detected polarity should be determined by programming GPIO Level Interrupt Polarity register (GLIPOL0 / GLIPOL1). Then GPIO level events will trigger level detect interrupt to CPU. The events are recorded by GPIO Level Interrupt Flag Register (GLIF0 / GLIF1) and level detect interrupt flag in GPIO Interrupt Flag Register (GIF.LEVEL). Program can also write GPIO Level Interrupt Force Register (GLIFRC0 / GLIFRC1) to force level event. As shown in Figure 4-7, Writing 1 to GLIC0 or GLIC1 will clear GPIO level-triggered interrupt flag in GLIF0 or GLIF1 and writing 0 has no effect; Writing 1 to GIC.LEVEL will clear GIF.LEVEL. GPIO level-triggered interrupt pending action is similar with edge-triggered interrupt pending issue.

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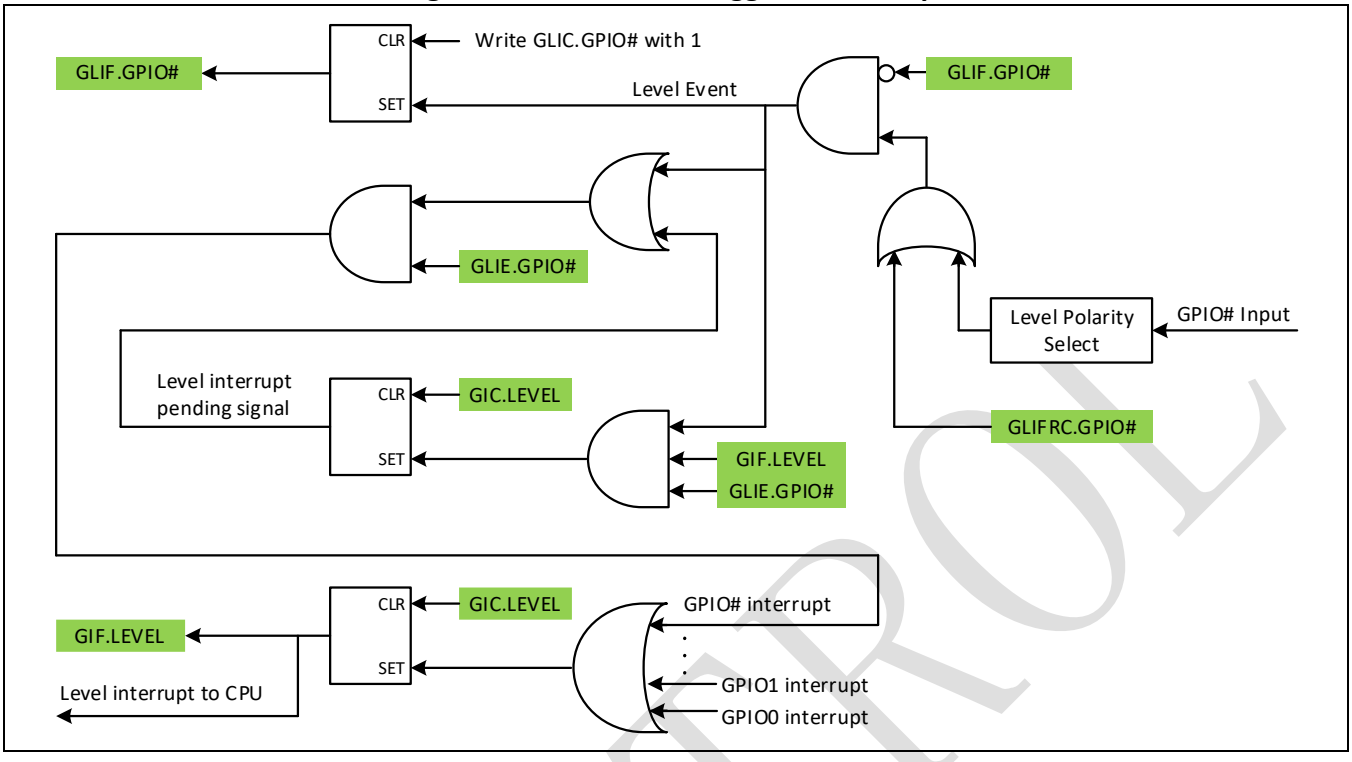
Figure 4-7: GPIO level-triggered interrupt



SPINTROL

4.4 Registers

4.4.1 PINMUX register map

Table 4-2: PINMUX Module Base Address

Peripheral Module	Base Address
PINMUX	0x4000 0300

Table 4-3: PINMUX Register Map

Register	Offset	Description	Reset Value
GPIO0*	0x00	GPIO0 Pin Control Register	0x01000019
GPIO1*	0x04	GPIO1 Pin Control Register	0x01000019
GPIO2*	0x08	GPIO2 Pin Control Register	0x01000019
GPIO3*	0x0C	GPIO3 Pin Control Register	0x01000019
GPIO4*	0x10	GPIO4 Pin Control Register	0x01000019
GPIO5*	0x14	GPIO5 Pin Control Register	0x01000019
GPIO6*	0x18	GPIO6 Pin Control Register	0x01000019
GPIO7*	0x1C	GPIO7 Pin Control Register	0x01000019
GPIO8*	0x20	GPIO8 Pin Control Register	0x01000019
GPIO9*	0x24	GPIO9 Pin Control Register	0x01000019
GPIO10*	0x28	GPIO10 Pin Control Register	0x01000019
GPIO11*	0x2C	GPIO11 Pin Control Register	0x01000019
GPIO12*	0x30	GPIO12 Pin Control Register	0x01000019
GPIO13*	0x34	GPIO13 Pin Control Register	0x01000019
GPIO14*	0x38	GPIO14 Pin Control Register	0x01000019
GPIO15*	0x3C	GPIO15 Pin Control Register	0x01000019
GPIO16*	0x40	GPIO16 Pin Control Register	0x01000019
GPIO17*	0x44	GPIO17 Pin Control Register	0x01000019
GPIO18*	0x48	GPIO18 Pin Control Register	0x01000019
GPIO19*	0x4C	GPIO19 Pin Control Register	0x01000019
GPIO20*	0x50	GPIO20 Pin Control Register	0x09000818
GPIO21*	0x54	GPIO21 Pin Control Register	0x19001818
GPIO22*	0x58	GPIO22 Pin Control Register	0x01000018
GPIO23*	0x5C	GPIO23 Pin Control Register	0x01000018
GPIO24*	0x60	GPIO24 Pin Control Register	0x00000018
GPIO25*	0x64	GPIO25 Pin Control Register	0x00000018
GPIO26*	0x68	GPIO26 Pin Control Register	0x00000018
GPIO27*	0x6C	GPIO27 Pin Control Register	0x00000018
GPIO28*	0x70	GPIO28 Pin Control Register	0x00000018
GPIO29*	0x74	GPIO29 Pin Control Register	0x00000018
GPIO30*	0x78	GPIO30 Pin Control Register	0x03000218
GPIO31*	0x7C	GPIO31 Pin Control Register	0x03000218
GPIO32*	0x80	GPIO32 Pin Control Register	0x00000018

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Register	Offset	Description	Reset Value
GPIO33*	0x84	GPIO33 Pin Control Register	0x00000018
GPIO34*	0x88	GPIO34 Pin Control Register	0x00000018
GPIO35*	0x8C	GPIO35 Pin Control Register	0x00000018
GPIO36*	0x90	GPIO36 Pin Control Register	0x00000018
GPIO37*	0x94	GPIO37 Pin Control Register	0x00000018
GPIO38*	0x98	GPIO38 Pin Control Register	0x09000818
GPIO39*	0x9C	GPIO39 Pin Control Register	0x05000418
GPIO40*	0xA0	GPIO40 Pin Control Register	0x09000818
GPIO41*	0xA4	GPIO41 Pin Control Register	0x09000818
GPIO42*	0xA8	GPIO42 Pin Control Register	0x03000218
GPIO43*	0xAC	GPIO43 Pin Control Register	0x03000218
GPIO44*	0xB0	GPIO44 Pin Control Register	0x05000418
GPIO45*	0xB4	GPIO45 Pin Control Register	0x03000218
GPIO46*	0xB8	GPIO46 Pin Control Register	0x01000018
GPIO47*	0xBC	GPIO47 Pin Control Register	0x01000018
GPIO48*	0xC0	GPIO48 Pin Control Register	0x03000018
GPIO49*	0xC4	GPIO49 Pin Control Register	0x03000018
GPIO50*	0xC8	GPIO50 Pin Control Register	0x07000018
GPIO51*	0xCC	GPIO51 Pin Control Register	0x05000018
GPIO52*	0xD0	GPIO52 Pin Control Register	0x00000018
GPIO53*	0xD4	GPIO53 Pin Control Register	0x00000018
GPIO54*	0xD8	GPIO54 Pin Control Register	0x00000018
GPIO55*	0xDC	GPIO55 Pin Control Register	0x00000018
GPIO56*	0xE0	GPIO56 Pin Control Register	0x00000018
GPIO57*	0xE4	GPIO57 Pin Control Register	0x00000018
GPIO58*	0xE8	GPIO58 Pin Control Register	0x00000018
GPIO59*	0xEC	GPIO59 Pin Control Register	0x00000018
GPIO60*	0xF0	GPIO60 Pin Control Register	0x00000018
GPIO61*	0xF4	GPIO61 Pin Control Register	0x00000018
PINMUXREGKEY	0xF8	PINMUX Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the PINMUXREGKEY=0x1ACCE551.

SPINTROL

4.4.2 PINMUX registers

4.4.2.1 GPIO# Pin Control Register (GPIO#)

Table 4-4: GPIO# Pin Control Register (GPIO#) Layout (# = 0 ~61)

GPIO# (GPIO# Pin Control Register) Offset: # * 4 Access: PINMUX -> GPIO#.all							
31	30	29	28	27	26	25	24
PU							
23	22	21	20	19	18	17	16
PD							
15	14	13	12	11	10	9	8
CHDFLTVAL							
7	6	5	4	3	2	1	0
STRENGTH		DEGLITCH	SMT	IE	MUXSEL		

Table 4-5: GPIO# Pin Control Register (GPIO#) Field Description (# = 0 ~61)

Bits	Field Name	Type	Reset	Description
31:24	PU	RW	–	Pull up enable Enable channel n pull-up if PU[n]=1
23:16	PD	RW	–	Pull down enable Enable channel n pull-down if PD[n]=1
15:8	CHDFLTVAL	RW	–	Default value for each demuxed input channel Channel n input = CHDFLTVAL[n] if MUXSEL != n (n=0~7)
7:6	STRENGTH	RW	–	Output driving strength 00: 5mA 01: 10mA 10: 15mA 11: 20mA
5	DEGLITCH	RW	–	Input deglitch 0: Disable input deglitch 1: Enable input deglitch
4	SMT	RW	–	Switch normal/schmitt input 0: Normal input 1: Schmitt input
3	IE	RW	–	Input enable 0: Input is always 0 1: Enable input
2:0	MUXSEL	RW	–	Channel select The channel definition for each GPIO is shown in Table 4-1.

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4.4.2.2 PINMUX Register Write-Allow Key Register (PINMUXREGKEY)

Table 4-6: PINMUX Register Write-Allow Key Register (PINMUXREGKEY) Layout

PINMUXREGKEY (PINMUX Register Write-Allow Key Register) Offset: 0xF8 Default: 0x1ACCE551 Access: PINMUX -> PINMUXREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 4-7: PINMUX Register Write-Allow Key Register (PINMUXREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected pinmux registers

SPINTROL

4.4.3 GPIO register map

Table 4-8: GPIO Module Base Address

Peripheral Module	Base Address
GPIO	0x4000 3000

Table 4-9: GPIO Register Map

Register	Offset	Description	Reset Value
GPLR0*	0x00	GPIO Pin Level Register 0	0x00030000
GPLR1*	0x04	GPIO Pin Level Register 1	0x000001CC
GPDR0*	0x0C	GPIO Pin Direction Register 0	0x00000000
GPDR1*	0x10	GPIO Pin Direction Register 1	0x00000000
GSLR0*	0x18	GPIO Pin Output Set Register 0	0x00000000
GSLR1*	0x1C	GPIO Pin Output Set Register 1	0x00000000
GCLR0*	0x24	GPIO Pin Output Clear Register 0	0x00000000
GCLR1*	0x28	GPIO Pin Output Clear Register 1	0x00000000
GRER0*	0x30	GPIO Rising Edge Detect Enable Register 0	0x00000000
GRER1*	0x34	GPIO Rising Edge Detect Enable Register 1	0x00000000
GFER0*	0x3C	GPIO Falling Edge Detect Enable Register 0	0x00000000
GFER1*	0x40	GPIO Falling Edge Detect Enable Register 1	0x00000000
GEDR0	0x48	GPIO Edge Detect Status Register 0	0x00000000
GEDR1	0x4C	GPIO Edge Detect Status Register 1	0x00000000
GSDR0*	0x54	GPIO Pin Bitwise Set Direction Register 0	0x00000000
GSDR1*	0x58	GPIO Pin Bitwise Set Direction Register 1	0x00000000
GCDR0*	0x60	GPIO Pin Bitwise Clear Direction Register 0	0x00000000
GCDR1*	0x64	GPIO Pin Bitwise Clear Direction Register 1	0x00000000
GSRER0*	0x6C	GPIO Bitwise Set Rising Edge Detect Enable Register 0	0x00000000
GSRER1*	0x70	GPIO Bitwise Set Rising Edge Detect Enable Register 1	0x00000000
GCRER0*	0x78	GPIO Bitwise Clear Rising Edge Detect Enable Register 0	0x00000000
GCRER1*	0x7C	GPIO Bitwise Clear Rising Edge Detect Enable Register 1	0x00000000
GSFER0*	0x84	GPIO Bitwise Set Falling Edge Detect Enable Register 0	0x00000000
GSFER1*	0x88	GPIO Bitwise Set Falling Edge Detect Enable Register 1	0x00000000
GCFER0*	0x90	GPIO Bitwise Clear Falling Edge Detect Enable Register 0	0x00000000
GCFER1*	0x94	GPIO Bitwise Clear Falling Edge Detect Enable Register 1	0x00000000
GEIE0*	0x9C	GPIO Edge-Triggered Interrupt Enable Register 0	0x00000000
GEIE1*	0xA0	GPIO Edge-Triggered Interrupt Enable Register 1	0x00000000
GLIF0*	0xA8	GPIO Level-Triggered Interrupt Flag Register 0	0x00000000
GLIF1*	0xAC	GPIO Level-Triggered Interrupt Flag Register 1	0x00000000
GLIE0*	0xB4	GPIO Level-Triggered Interrupt Enable Register 0	0x00000000
GLIE1*	0xB8	GPIO Level-Triggered Interrupt Enable Register 1	0x00000000
GLIC0	0xC0	GPIO Level-Triggered Interrupt Clear Register 0	0x00000000
GLIC1	0xC4	GPIO Level-Triggered Interrupt Clear Register 1	0x00000000
GLIFRC0*	0xCC	GPIO Level-Triggered Interrupt Force Register 0	0x00000000
GLIFRC1*	0xD0	GPIO Level-Triggered Interrupt Force Register 1	0x00000000

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Register	Offset	Description	Reset Value
GLIPOL0*	0xD8	GPIO Level-Triggered Interrupt Polarity Register 0	0x00000000
GLIPOL1*	0xDC	GPIO Level-Triggered Interrupt Polarity Register 1	0x00000000
GIF	0xE4	GPIO Interrupt Flag Register	0x00000000
GIC	0xE8	GPIO Interrupt Flag Clear Register	0x00000000
GPIOREGKEY	0xEC	GPIO Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the GPIOREGKEY=0x1ACCE551.

SPINTROL

4.4.4 GPIO registers

4.4.4.1 GPIO Pin Level Register 0 (GPLR0)

Table 4-10: GPIO Pin Level Register 0 (GPLR0) Layout

GPLR0 (GPIO Pin Level Register 0) Offset: 0x0 Default: 0x00030000 Access: GPIO -> GPLR0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-11: GPIO Pin Level Register 0 (GPLR0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x30000	GPIOn pin level (n = 0~31) 0: Write a 0 sets the pin level to low Read a 0 indicates current pin level is low 1: Write a 1 sets the pin level to high Read a 1 indicates current pin level is high

4.4.4.2 GPIO Pin Level Register 1 (GPLR1)

Table 4-12: GPIO Pin Level Register 1 (GPLR1) Layout

GPLR1 (GPIO Pin Level Register 1) Offset: 0x4 Default: 0x000FFFC0 Access: GPIO -> GPLR1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-13: GPIO Pin Level Register 1 (GPLR1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RW	0x1CC	GPIOn pin level(n = 32~61) 0: Write a 0 sets the pin level to low Read a 0 indicates current pin level is low 1: Write a 1 sets the pin level to high Read a 1 indicates current pin level is high

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4.4.4.3 GPIO Pin Direction Register 0 (GPDR0)

Table 4-14: GPIO Pin Direction Register 0 (GPDR0) Layout

GPDR0 (GPIO Pin Direction Register 0) Offset: 0xC Default: 0x00000000 Access: GPIO -> GPDR0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-15: GPIO Pin Direction Register 0 (GPDR0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Set GPIOn direction (n = 0~31) 0: Set GPIOn as input 1: Set GPIOn as output

4.4.4.4 GPIO Pin Direction Register 1 (GPDR1)

Table 4-16: GPIO Pin Direction Register 1 (GPDR1) Layout

GPDR1 (GPIO Pin Direction Register 1) Offset: 0x10 Default: 0x00000000 Access: GPIO -> GPDR1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-17: GPIO Pin Direction Register 1 (GPDR1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RW	0x0	Set GPIOn direction (n = 32~61) 0: Set GPIOn as input 1: Set GPIOn as output

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4.4.4.5 GPIO Pin Output Set Register 0 (GSLR0)

Table 4-18: GPIO Pin Output Set Register 0 (GSLR0) Layout

GSLR0 (GPIO Pin Output Set Register 0) Offset: 0x18 Default: 0x00000000 Access: GPIO -> GSLR0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-19: GPIO Pin Output Set Register 0 (GSLR0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1S	0x0	Set GPIOn output to high (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GPIOn output to high This bit is self-cleared to 0

4.4.4.6 GPIO Pin Output Set Register 1 (GSLR1)

Table 4-20: GPIO Pin Output Set Register 1 (GSLR1) Layout

GSLR1 (GPIO Pin Output Set Register 1) Offset: 0x1C Default: 0x00000000 Access: GPIO -> GSLR1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-21: GPIO Pin Output Set Register 1 (GSLR1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1S	0x0	Set GPIOn output to high (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GPIOn output to high This bit is self-cleared to 0

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4.4.4.7 GPIO Pin Output Clear Register 0 (GCLR0)

Table 4-22: GPIO Pin Output Clear Register 0 (GCLR0) Layout

GCLR0 (GPIO Pin Output Clear Register 0) Offset: 0x24 Default: 0x00000000 Access: GPIO -> GCLR0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-23: GPIO Pin Output Clear Register 0 (GCLR0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1C	0x0	Clear GPIOn output to low (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GPIOn output to low This bit is self-cleared to 0

4.4.4.8 GPIO Pin Output Clear Register 1 (GCLR1)

Table 4-24: GPIO Pin Output Clear Register 1 (GCLR1) Layout

GCLR1 (GPIO Pin Output Clear Register 1) Offset: 0x28 Default: 0x00000000 Access: GPIO -> GCLR1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-25: GPIO Pin Output Clear Register 1 (GCLR1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1C	0x0	Clear GPIOn output to low (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GPIOn output to low This bit is self-cleared to 0

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4.4.4.9 GPIO Rising Edge Detect Enable Register 0 (GRER0)

Table 4-26: GPIO Rising Edge Detect Enable Register 0 (GRER0) Layout

GRER0 (GPIO Rising Edge Detect Enable Register 0) Offset: 0x30 Default: 0x00000000 Access: GPIO -> GRER0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-27: GPIO Rising Edge Detect Enable Register 0 (GRER0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Enable GPIOn rising edge detection (n = 0~31) 0: Disable rising edge detection on GPIOn 1: Enable rising edge detection on GPIOn

4.4.4.10 GPIO Rising Edge Detect Enable Register 1 (GRER1)

Table 4-28: GPIO Rising Edge Detect Enable Register 1 (GRER1) Layout

GRER1 (GPIO Rising Edge Detect Enable Register 1) Offset: 0x34 Default: 0x00000000 Access: GPIO -> GRER1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-29: GPIO Rising Edge Detect Enable Register 1 (GRER1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RW	0x0	Enable GPIOn rising edge detection (n = 32~61) 0: Disable rising edge detection on GPIOn 1: Enable rising edge detection on GPIOn

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4.4.4.11 GPIO Falling Edge Detect Enable Register 0 (GFER0)

Table 4-30: GPIO Falling Edge Detect Enable Register 0 (GFER0) Layout

GFER0 (GPIO Falling Edge Detect Enable Register 0) Offset: 0x3C Default: 0x00000000 Access: GPIO -> GFER0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-31: GPIO Falling Edge Detect Enable Register 0 (GFER0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Enable GPIOn falling edge detection (n = 0~31) 0: Disable falling edge detection on GPIOn 1: Enable falling edge detection on GPIOn

4.4.4.12 GPIO Falling Edge Detect Enable Register 1 (GFER1)

Table 4-32: GPIO Falling Edge Detect Enable Register 1 (GFER1) Layout

GFER1 (GPIO Falling Edge Detect Enable Register 1) Offset: 0x40 Default: 0x00000000 Access: GPIO -> GFER1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-33: GPIO Falling Edge Detect Enable Register 1 (GFER1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RW	0x0	Enable GPIOn falling edge detection (n = 32~61) 0: Disable falling edge detection on GPIOn 1: Enable falling edge detection on GPIOn

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4.4.4.13 GPIO Edge Detect Status Register 0 (GEDR0)

Table 4-34: GPIO Edge Detect Status Register 0 (GEDR0) Layout

GEDR0 (GPIO Edge Detect Status Register 0) Offset: 0x48 Default: 0x00000000 Access: GPIO -> GEDR0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-35: GPIO Edge Detect Status Register 0 (GEDR0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1C	0x0	GPIOn edge detect status (n = 0~31) 0: Read 0 indicates no detected rising or falling edge Write 0 has no effect 1: Read 1 indicates edge was detected Write 1 clears the latched status

4.4.4.14 GPIO Edge Detect Status Register 1 (GEDR1)

Table 4-36: GPIO Edge Detect Status Register 1 (GEDR1) Layout

GEDR1 (GPIO Edge Detect Status Register 1) Offset: 0x4C Default: 0x00000000 Access: GPIO -> GEDR1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-37: GPIO Edge Detect Status Register 1 (GEDR1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1C	0x0	GPIOn edge detect status (n = 32~61) 0: Read 0 indicates no detected rising or falling edge Write 0 has no effect 1: Read 1 indicates edge was detected Write 1 clears the latched status

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4.4.4.15 GPIO Pin Bitwise Set Direction Register 0 (GSDR0)

Table 4-38: GPIO Pin Bitwise Set Direction Register 0 (GSDR0) Layout

GSDR0 (GPIO Pin Bitwise Set Direction Register 0) Offset: 0x54 Default: 0x00000000 Access: GPIO -> GSDR0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-39: GPIO Pin Bitwise Set Direction Register 0 (GSDR0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1S	0x0	Set GPDR0 register bit (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GPDR0 bit (sets GPIOn as output) This bit is self-cleared to 0

4.4.4.16 GPIO Pin Bitwise Set Direction Register 1 (GSDR1)

Table 4-40: GPIO Pin Bitwise Set Direction Register 1 (GSDR1) Layout

GSDR1 (GPIO Pin Bitwise Set Direction Register 1) Offset: 0x58 Default: 0x00000000 Access: GPIO -> GSDR1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-41: GPIO Pin Bitwise Set Direction Register 1 (GSDR1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1S	0x0	Set GPDR1 register bit (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GPDR1 bit (sets GPIOn as output) This bit is self-cleared to 0

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4.4.4.17 GPIO Pin Bitwise Clear Direction Register 0 (GCDR0)

Table 4-42: GPIO Pin Bitwise Clear Direction Register 0 (GCDR0) Layout

GCDR0 (GPIO Pin Bitwise Clear Direction Register 0) Offset: 0x60 Default: 0x00000000 Access: GPIO -> GCDR0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-43: GPIO Pin Bitwise Clear Direction Register 0 (GCDR0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1C	0x0	Clear GPDR0 register bit (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GPDR0 bit (sets GPIOn as input) This bit is self-cleared to 0

4.4.4.18 GPIO Pin Bitwise Clear Direction Register 1 (GCDR1)

Table 4-44: GPIO Pin Bitwise Clear Direction Register 1 (GCDR1) Layout

GCDR1 (GPIO Pin Bitwise Clear Direction Register 1) Offset: 0x64 Default: 0x00000000 Access: GPIO -> GCDR1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-45: GPIO Pin Bitwise Clear Direction Register 1 (GCDR1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1C	0x0	Clear GPDR1 register bit (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GPDR1 bit (sets GPIOn as input) This bit is self-cleared to 0

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4.4.4.19 GPIO Bitwise Set Rising Edge Detect Enable Register 0 (GSRER0)

Table 4-46: GPIO Bitwise Set Rising Edge Detect Enable Register 0 (GSRER0) Layout

GSRER0 (GPIO Bitwise Set Rising Edge Detect Enable Register 0) Offset: 0x6C Default: 0x00000000 Access: GPIO -> GSRER0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-47: GPIO Bitwise Set Rising Edge Detect Enable Register 0 (GSRER0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1S	0x0	Set GRER0 register bit (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GRER0 bit (enable rising edge detection on GPIOn) This bit is self-cleared to 0

4.4.4.20 GPIO Bitwise Set Rising Edge Detect Enable Register 1 (GSRER1)

Table 4-48: GPIO Bitwise Set Rising Edge Detect Enable Register 1 (GSRER1) Layout

GSRER1 (GPIO Bitwise Set Rising Edge Detect Enable Register 1) Offset: 0x70 Default: 0x00000000 Access: GPIO -> GSRER1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-49: GPIO Bitwise Set Rising Edge Detect Enable Register 1 (GSRER1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1S	0x0	Set GRER1 register bit (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GRER1 bit (enable rising edge detection on GPIOn) This bit is self-cleared to 0

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4.4.4.21 GPIO Bitwise Clear Rising Edge Detect Enable Register 0 (GCRER0)

Table 4-50: GPIO Bitwise Clear Rising Edge Detect Enable Register 0 (GCRER0) Layout

GCRER0 (GPIO Bitwise Clear Rising Edge Detect Enable Register 0) Offset: 0x78 Default: 0x00000000 Access: GPIO -> GCRER0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-51: GPIO Bitwise Clear Rising Edge Detect Enable Register 0 (GCRER0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1C	0x0	Clear GRER0 register bit (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GRER0 bit (disable rising edge detection on GPIOn) This bit is self-cleared to 0

4.4.4.22 GPIO Bitwise Clear Rising Edge Detect Enable Register 1 (GCRER1)

Table 4-52: GPIO Bitwise Clear Rising Edge Detect Enable Register 1 (GCRER1) Layout

GCRER1 (GPIO Bitwise Clear Rising Edge Detect Enable Register 1) Offset: 0x7C Default: 0x00000000 Access: GPIO -> GCRER1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-53: GPIO Bitwise Clear Rising Edge Detect Enable Register 1 (GCRER1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1C	0x0	Clear GRER1 register bit (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GRER1 bit (disable rising edge detection on GPIOn) This bit is self-cleared to 0

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4.4.4.23 GPIO Bitwise Set Falling Edge Detect Enable Register 0 (GSFER0)

Table 4-54: GPIO Bitwise Set Falling Edge Detect Enable Register 0 (GSFER0) Layout

GSFER0 (GPIO Bitwise Set Falling Edge Detect Enable Register 0) Offset: 0x84 Default: 0x00000000 Access: GPIO -> GSFER0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-55: GPIO Bitwise Set Falling Edge Detect Enable Register 0 (GSFER0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1S	0x0	Set GFER0 register bit (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GFER0 bit (enable falling edge detection on GPIOn) This bit is self-cleared to 0

4.4.4.24 GPIO Bitwise Set Falling Edge Detect Enable Register 1 (GSFER1)

Table 4-56: GPIO Bitwise Set Falling Edge Detect Enable Register 1 (GSFER1) Layout

GSFER1 (GPIO Bitwise Set Falling Edge Detect Enable Register 1) Offset: 0x88 Default: 0x00000000 Access: GPIO -> GSFER1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-57: GPIO Bitwise Set Falling Edge Detect Enable Register 1 (GSFER1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1S	0x0	Set GFER1 register bit (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 sets GFER1 bit (enable falling edge detection on GPIOn) This bit is self-cleared to 0

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4.4.4.25 GPIO Bitwise Clear Falling Edge Detect Enable Register 0 (GCFER0)

Table 4-58: GPIO Bitwise Clear Falling Edge Detect Enable Register 0 (GCFER0) Layout

GCFER0 (GPIO Bitwise Clear Falling Edge Detect Enable Register 0) Offset: 0x90 Default: 0x00000000 Access: GPIO -> GCFER0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-59: GPIO Bitwise Clear Falling Edge Detect Enable Register 0 (GCFER0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1C	0x0	Clear GFER0 register bit (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GFER0 bit (disable falling edge detection on GPIOn) This bit is self-cleared to 0

4.4.4.26 GPIO Bitwise Clear Falling Edge Detect Enable Register 1 (GCFER1)

Table 4-60: GPIO Bitwise Clear Falling Edge Detect Enable Register 1 (GCFER1) Layout

GCFER1 (GPIO Bitwise Clear Falling Edge Detect Enable Register 1) Offset: 0x94 Default: 0x00000000 Access: GPIO -> GCFER1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-61: GPIO Bitwise Clear Falling Edge Detect Enable Register 1 (GCFER1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1C	0x0	Clear GFER1 register bit (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears GFER1 bit (disable falling edge detection on GPIOn) This bit is self-cleared to 0

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4.4.4.27 GPIO Edge-Triggered Interrupt Enable Register 0 (GEIE0)

Table 4-62: GPIO Edge-Triggered Interrupt Enable Register 0 (GEIE0) Layout

GEIE0 (GPIO Edge-Triggered Interrupt Enable Register 0) Offset: 0x9C Default: 0x00000000 Access: GPIO -> GEIE0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-63: GPIO Edge-Triggered Interrupt Enable Register 0 (GEIE0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	GPIOn edge-triggered interrupt enable (n = 0~31) 0: Disable GPIOn edge-triggered interrupt 1: Enable GPIOn edge-triggered interrupt

4.4.4.28 GPIO Edge-Triggered Interrupt Enable Register 1 (GEIE1)

Table 4-64: GPIO Edge-Triggered Interrupt Enable Register 1 (GEIE1) Layout

GEIE1 (GPIO Edge-Triggered Interrupt Enable Register 1) Offset: 0xA0 Default: 0x00000000 Access: GPIO -> GEIE1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-65: GPIO Edge-Triggered Interrupt Enable Register 1 (GEIE1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RW	0x0	GPIOn edge-triggered interrupt enable (n = 32~61) 0: Disable GPIOn edge-triggered interrupt 1: Enable GPIOn edge-triggered interrupt

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4.4.4.29 GPIO Level-Triggered Interrupt Flag Register 0 (GLIF0)

Table 4-66: GPIO Level-Triggered Interrupt Flag Register 0 (GLIF0) Layout

GLIF0 (GPIO Level-Triggered Interrupt Flag Register 0) Offset: 0xA8 Default: 0x00000000 Access: GPIO -> GLIF0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-67: GPIO Level-Triggered Interrupt Flag Register 0 (GLIF0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	GPIOn level-triggered interrupt flag (n = 0~31) 0: GPIOn level-triggered interrupt does not occur 1: GPIOn level-triggered interrupt occurred

4.4.4.30 GPIO Level-Triggered Interrupt Flag Register 1 (GLIF1)

Table 4-68: GPIO Level-Triggered Interrupt Flag Register 1 (GLIF1) Layout

GLIF1 (GPIO Level-Triggered Interrupt Flag Register 1) Offset: 0xAC Default: 0x00000000 Access: GPIO -> GLIF1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-69: GPIO Level-Triggered Interrupt Flag Register 1 (GLIF1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RO	0x0	GPIOn level-triggered interrupt flag (n = 32~61) 0: GPIOn level-triggered interrupt does not occur 1: GPIOn level-triggered interrupt occurred

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4.4.4.31 GPIO Level-Triggered Interrupt Enable Register 0 (GLIE0)

Table 4-70: GPIO Level-Triggered Interrupt Enable Register 0 (GLIE0) Layout

GLIE0 (GPIO Level-Triggered Interrupt Enable Register 0) Offset: 0xB4 Default: 0x00000000 Access: GPIO -> GLIE0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-71: GPIO Level-Triggered Interrupt Enable Register 0 (GLIE0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	GPIOn level-triggered interrupt enable (n = 0~31) 0: Disable GPIOn level-triggered interrupt 1: Enable GPIOn level-triggered interrupt

4.4.4.32 GPIO Level-Triggered Interrupt Enable Register 1 (GLIE1)

Table 4-72: GPIO Level-Triggered Interrupt Enable Register 1 (GLIE1) Layout

GLIE1 (GPIO Level-Triggered Interrupt Enable Register 1) Offset: 0xB8 Default: 0x00000000 Access: GPIO -> GLIE1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-73: GPIO Level-Triggered Interrupt Enable Register 1 (GLIE1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RW	0x0	GPIOn level-triggered interrupt enable (n = 32~61) 0: Disable GPIOn level-triggered interrupt 1: Enable GPIOn level-triggered interrupt

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4.4.4.33 GPIO Level-Triggered Interrupt Clear Register 0 (GLIC0)

Table 4-74: GPIO Level-Triggered Interrupt Clear Register 0 (GLIC0) Layout

GLIC0 (GPIO Level-Triggered Interrupt Clear Register 0) Offset: 0xC0 Default: 0x00000000 Access: GPIO -> GLIC0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-75: GPIO Level-Triggered Interrupt Clear Register 0 (GLIC0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1C	0x0	GPIOn level-triggered interrupt clear (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the level-triggered interrupt flag This bit is self-cleared to 0

4.4.4.34 GPIO Level-Triggered Interrupt Clear Register 1 (GLIC1)

Table 4-76: GPIO Level-Triggered Interrupt Clear Register 1 (GLIC1) Layout

GLIC1 (GPIO Level-Triggered Interrupt Clear Register 1) Offset: 0xC4 Default: 0x00000000 Access: GPIO -> GLIC1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-77: GPIO Level-Triggered Interrupt Clear Register 1 (GLIC1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1C	0x0	GPIOn level-triggered interrupt clear (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the level-triggered interrupt flag This bit is self-cleared to 0

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4.4.4.35 GPIO Level-Triggered Interrupt Force Register 0 (GLIFRC0)

Table 4-78: GPIO Level-Triggered Interrupt Force Register 0 (GLIFRC0) Layout

GLIFRC0 (GPIO Level-Triggered Interrupt Force Register 0) Offset: 0xCC Default: 0x00000000 Access: GPIO -> GLIFRC0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-79: GPIO Level-Triggered Interrupt Force Register 0 (GLIFRC0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	W1S	0x0	GPIOn level-triggered interrupt force (n = 0~31) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 force the level-triggered interrupt flag This bit is self-cleared to 0

4.4.4.36 GPIO Level-Triggered Interrupt Force Register 1 (GLIFRC1)

Table 4-80: GPIO Level-Triggered Interrupt Force Register 1 (GLIFRC1) Layout

GLIFRC1 (GPIO Level-Triggered Interrupt Force Register 1) Offset: 0xD0 Default: 0x00000000 Access: GPIO -> GLIFRC1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-81: GPIO Level-Triggered Interrupt Force Register 1 (GLIFRC1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	W1S	0x0	GPIOn level-triggered interrupt force (n = 32~61) 0: Write a 0 has no effect and always reads back 0 1: Write a 1 force the level-triggered interrupt flag This bit is self-cleared to 0

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4.4.4.37 GPIO Level-Triggered Interrupt Polarity Register 0 (GLIPOL0)

Table 4-82: GPIO Level-Triggered Interrupt Polarity Register 0 (GLIPOL0) Layout

GLIPOL0 (GPIO Level-Triggered Interrupt Polarity Register 0) Offset: 0xD8 Default: 0x00000000 Access: GPIO -> GLIPOL0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-83: GPIO Level-Triggered Interrupt Polarity Register 0 (GLIPOL0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	GPIOn level-triggered interrupt polarity (n = 0~31) 0: Trigger interrupt when GPIOn is low 1: Trigger interrupt when GPIOn is high

4.4.4.38 GPIO Level-Triggered Interrupt Polarity Register 1 (GLIPOL1)

Table 4-84: GPIO Level-Triggered Interrupt Polarity Register 1 (GLIPOL1) Layout

GLIPOL1 (GPIO Level-Triggered Interrupt Polarity Register 1) Offset: 0xDC Default: 0x00000000 Access: GPIO -> GLIPOL1.all							
31	30	29	28	27	26	25	24
RESERVED		VAL					
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 4-85: GPIO Level-Triggered Interrupt Polarity Register 1 (GLIPOL1) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:0	VAL	RW	0x0	GPIOn level-triggered interrupt polarity (n = 32~61) 0: Trigger interrupt when GPIOn is low 1: Trigger interrupt when GPIOn is high

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4.4.4.39 GPIO Interrupt Flag Register (GIF)

Table 4-86: GPIO Interrupt Flag Register (GIF) Layout

GIF (GPIO Interrupt Flag Register) Offset: 0xE4 Default: 0x00000000 Access: GPIO -> GIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED						LEVEL	EDGE

Table 4-87: GPIO Interrupt Flag Register (GIF) Field Description

Bits	Field Name	Type	Reset	Description
31:2	RESERVED_31_2	RO	0x0	Reserved
1	LEVEL	RO	0x0	GPIO level-triggered interrupt flag 0: Not Occur 1: Occur
0	EDGE	RO	0x0	GPIO edge-triggered interrupt flag 0: Not Occur 1: Occur

SPINTROL

4.4.4.40 GPIO Interrupt Flag Clear Register (GIC)

Table 4-88: GPIO Interrupt Flag Clear Register (GIC) Layout

GIC (GPIO Interrupt Flag Clear Register) Offset: 0xE8 Default: 0x00000000 Access: GPIO -> GIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED						LEVEL	EDGE

Table 4-89: GPIO Interrupt Flag Clear Register (GIC) Field Description

Bits	Field Name	Type	Reset	Description
31:2	RESERVED_31_2	RO	0x0	Reserved
1	LEVEL	W1C	0x0	GPIO level-triggered interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
0	EDGE	W1C	0x0	GPIO edge-triggered interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.

4.4.4.41 GPIO Register Write-Allow Key Register (GPIOREGKEY)

Table 4-90: GPIO Register Write-Allow Key Register (GPIOREGKEY) Layout

GPIOREGKEY (GPIO Register Write-Allow Key Register) Offset: 0xEC Default: 0x1ACCE551 Access: GPIO -> GPIOREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 4-91: GPIO Register Write-Allow Key Register (GPIOREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected GPIO registers

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5 Interrupts and events

5.1 Nested vectored interrupt controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of ARM Cortex-M4 processor unit. Due to a tight coupling with the CPU, it provides the lowest interrupt latency and efficient processing of late arriving interrupts.

5.1.1 Features

The NVIC supports the following features:

- Up to 63 vectored interrupts (not including the sixteen Cortex-M4 interrupts)
- 16 programmable interrupt priority levels for each interrupt (4 bits of interrupt priority are used). A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority
- Controls system exceptions and peripheral interrupts
- Support for interrupt tail-chaining and late-arrival
- Support for interrupt lazy-stacking
- Support for NMI

5.1.2 Interrupt and exception vectors

When an exception event takes place and is being handled by the Cortex-M4, the processor will need to locate the starting address of the exception handler. Therefore, a vector table mechanism is used. The vector table is an array of word data inside the system memory, each representing the starting address of one exception. The vector table location is controlled by a programmable register in the NVIC called the VTOR (address 0xE000ED08). After reset, the VTOR is reset to 0; therefore, the vector table is located at address 0x0 after reset. The vector address is arranged according to the exception number times four. Table 5-1 is the vector table for SPC2168.

Table 5-1: Vector table for SPC2168

Vector#	IRQ#	Acronym	Priority	Description	Address Offset
-	-	MSP	-	Initial main stack pointer	0x0000_0000
1	-	Reset	-3, the highest	Reset vector	0x0000_0004
2	-14	NMI	-2	Non mask-able interrupt. The watchdog timer 0 is linked to the NMI vector.	0x0000_0008
3	-13	Hard Fault	-1	Hard fault	0x0000_000C
4	-12	MemManage	Configurable	Memory management	0x0000_00010
5	-11	Bus Fault	Configurable	Bus fault	0x0000_0014
6	-10	Usage Fault	Configurable	Usage fault	0x0000_0018
7-10	-	-	-	Reserved	0x0000_001C – 0x0000_002B
11	-5	SVCall	Configurable	Supervisor call	0x0000_002C

SPINTROL

Vector#	IRQ#	Acronym	Priority	Description	Address Offset
12	-4	Debug Monitor	Configurable	Debug monitor	0x0000_0030
13	-	-	-	Reserved	0x0000_0034
14	-2	PendSV	Configurable	Pendable service call	0x0000_0038
15	-1	SysTick	Configurable	SysTick timer interrupt	0x0000_003C
16	0	MEM	Configurable	Memory error interrupt	0x0000_0040
17	1	POWER	Configurable	Power error interrupt (BOD)	0x0000_0044
18	2	CLOCK	Configurable	Clock error interrupt	0x0000_0048
19	3	WDT1	Configurable	Watchdog timer 1 interrupt	0x0000_004C
20	4	GPIO_LEVEL	Configurable	GPIO level-trigger interrupt	0x0000_0050
21	5	GPIO_EDGE	Configurable	GPIO edge-trigger interrupt	0x0000_0054
22	6	SIO0A	Configurable	SIO0 interrupt A	0x0000_0058
23	7	SIO0B	Configurable	SIO0 interrupt B	0x0000_005C
24	8	SIO1A	Configurable	SIO1 interrupt A	0x0000_0060
25	9	SIO1B	Configurable	SIO1 interrupt B	0x0000_0064
26	10	SIO2A	Configurable	SIO2 interrupt A	0x0000_0068
27	11	SIO2B	Configurable	SIO2 interrupt B	0x0000_006C
28	12	UART	Configurable	UART interrupt	0x0000_0070
29	13	SSP	Configurable	SSP interrupt	0x0000_0074
30	14	I2C	Configurable	I2C interrupt	0x0000_0078
31	15	ADC0	Configurable	ADC SOC0 interrupt	0x0000_007C
32	16	ADC1	Configurable	ADC SOC1 interrupt	0x0000_0080
33	17	ADC2	Configurable	ADC SOC2 interrupt	0x0000_0084
34	18	ADC3	Configurable	ADC SOC3 interrupt	0x0000_0088
35	19	ADC4	Configurable	ADC SOC4 interrupt	0x0000_008C
36	20	ADC5	Configurable	ADC SOC5 interrupt	0x0000_0090
37	21	ADC6	Configurable	ADC SOC6 interrupt	0x0000_0094
38	22	ADC7	Configurable	ADC SOC7 interrupt	0x0000_0098
39	23	ADC8	Configurable	ADC SOC8 interrupt	0x0000_009C
40	24	ADC9	Configurable	ADC SOC9 interrupt	0x0000_00A0
41	25	ADC10	Configurable	ADC SOC10 interrupt	0x0000_00A4
42	26	ADC11	Configurable	ADC SOC11 interrupt	0x0000_00A8
43	27	ADC12	Configurable	ADC SOC12 interrupt	0x0000_00AC
44	28	ADC13	Configurable	ADC SOC13 interrupt	0x0000_00B0
45	29	ADC14	Configurable	ADC SOC14 interrupt	0x0000_00B4
46	30	ADC15	Configurable	ADC SOC15 interrupt	0x0000_00B8
47	31	ADCPPU0	Configurable	ADC post-process unit 0 interrupt	0x0000_00BC
48	32	ADCPPU1	Configurable	ADC post-process unit 1 interrupt	0x0000_00C0
49	33	ADCPPU2	Configurable	ADC post-process unit 2 interrupt	0x0000_00C4
50	34	ADCPPU3	Configurable	ADC post-process unit 3 interrupt	0x0000_00C8
51	35	ADCPPU4	Configurable	ADC post-process unit 4 interrupt	0x0000_00CC
52	36	ADCPPU5	Configurable	ADC post-process unit 5 interrupt	0x0000_00D0

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Vector#	IRQ#	Acronym	Priority	Description	Address Offset
53	37	ADCPPU6	Configurable	ADC post-process unit 6 interrupt	0x0000_00D4
54	38	ADCPPU7	Configurable	ADC post-process unit 7 interrupt	0x0000_00D8
55	39	PWM0	Configurable	PWM0 interrupt	0x0000_00DC
56	40	PWM1	Configurable	PWM1 interrupt	0x0000_00E0
57	41	PWM2	Configurable	PWM2 interrupt	0x0000_00E4
58	42	PWM3	Configurable	PWM3 interrupt	0x0000_00E8
59	43	PWM4	Configurable	PWM4 interrupt	0x0000_00EC
60	44	PWM5	Configurable	PWM5 interrupt	0x0000_00F0
61	45	PWM6	Configurable	PWM6 interrupt	0x0000_00F4
62	46	PWM7	Configurable	PWM7 interrupt	0x0000_00F8
63	47	PWM0TZ	Configurable	PWM0 trip-zone interrupt	0x0000_00FC
64	48	PWM1TZ	Configurable	PWM1 trip-zone interrupt	0x0000_0100
65	49	PWM2TZ	Configurable	PWM2 trip-zone interrupt	0x0000_0104
66	50	PWM3TZ	Configurable	PWM3 trip-zone interrupt	0x0000_0108
67	51	PWM4TZ	Configurable	PWM4 trip-zone interrupt	0x0000_010C
68	52	PWM5TZ	Configurable	PWM5 trip-zone interrupt	0x0000_0110
69	53	PWM6TZ	Configurable	PWM6 trip-zone interrupt	0x0000_0114
70	54	PWM7TZ	Configurable	PWM7 trip-zone interrupt	0x0000_0118
71	55	ECAP	Configurable	ECAP interrupt	0x0000_011C
72	56	TIMER0	Configurable	General purpose timer 0 interrupt	0x0000_0120
73	57	TIMER1	Configurable	General purpose timer 1 interrupt	0x0000_0124
74	58	TIMER2	Configurable	General purpose timer 2 interrupt	0x0000_0128
75	59	CRC	Configurable	CRC interrupt	0x0000_012C
76	60	AES	Configurable	AES interrupt	0x0000_0130
77	61	DMAC	Configurable	DMA Controller interrupt	0x0000_0134
78	62	MAILBOX	Configurable	Mail-Box interrupt	0x0000_0138

5.1.3 NVIC interrupt configuration

NVIC interrupts can be enabled by writing to the SETENA register or disabled by writing to the CLRENA register. In this way, enabling or disabling an interrupt will not affect other interrupt enable states. The SETENA/CLRENA registers are 32 bits wide; each bit represents one interrupt input.

The NVIC interrupt-pending status can be accessed through the Interrupt Set Pending (SETPEND) and Interrupt Clear Pending (CLRPEND) registers. You can cancel a current pended exception through the CLRPEND register, or generate software interrupts through the SETPEND register.

Each external interrupt has an associated priority-level register, which has a maximum width of 8 bits and a minimum width of 3 bits. Each register can be further divided into preempt priority level and sub-priority level based on priority group settings. The SPC2168 implements 4 bits of priority level, so the chip supports 16 levels of programmable priority.

Please see ARM® released documents for more information of NVIC configurations.

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5.2 SysTick Timer

The Cortex-M4 processor includes an integrated system timer, called SysTick. The SYSTICK timer is a 24-bit down counter. Once it reaches zero, the counter loads the reload value from the RELOAD register. It does not stop until the enable bit in the SYSTICK Control and Status register is cleared.

When the SYSTICK timer changes from 1 to 0, it will set the COUNTFLAG bit in the SYSTICK Control and Status register. The COUNTFLAG can be cleared by one of the following:

- Read of the SYSTICK Control and Status register by the processor
- Clear of the SYSTICK counter value by writing any value to the SYSTICK Current Value register

The SYSTICK counter can be used to generate SYSTICK exceptions at regular intervals. This is often necessary for the OS, for task and resources management. To enable SYSTICK exception generation, the TICKINT bit should be set.

Please see ARM released documents for more information of SysTick Timer configurations.

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6 AES

6.1 AES overview

The SPC2168 implements an AES (Advanced Encryption Standard) engine to provide encryption and decryption services. The AES engine supports ECB, CBC, CTR, CCM* and MMO mode. The key length can be as many as 256 bits. The main features of the AES engine are:

- Supports as many as six block cipher modes: ECB, CBC, CTR, CCM*, MMO and Bypass
- 128, 192 and 256-bit key size
- Supports partial code
- Data IO by register interface
- Interrupt on completed AES operation (Output FIFO is empty and Input FIFO is full)
- Error indications for each block cipher mode
- Separate 4*32-bit input and output FIFOs
- Special feature for security mode
  - CTR: Supports counter modular from 16 to 128
  - CCM*: Supports 0 to (2^{32-1}) bytes associated string and message string
  - Supports 11-13 bytes nonce and supports L(15 – length of nonce) from 2 to 4

6.2 Functional description

The AES module implements ECB, CBC, CTR, CCM*, MMO and Bypass block cipher modes by efficient hardware.

6.2.1 AES operation flow

See Figure 6-1 for the AES operational flow.

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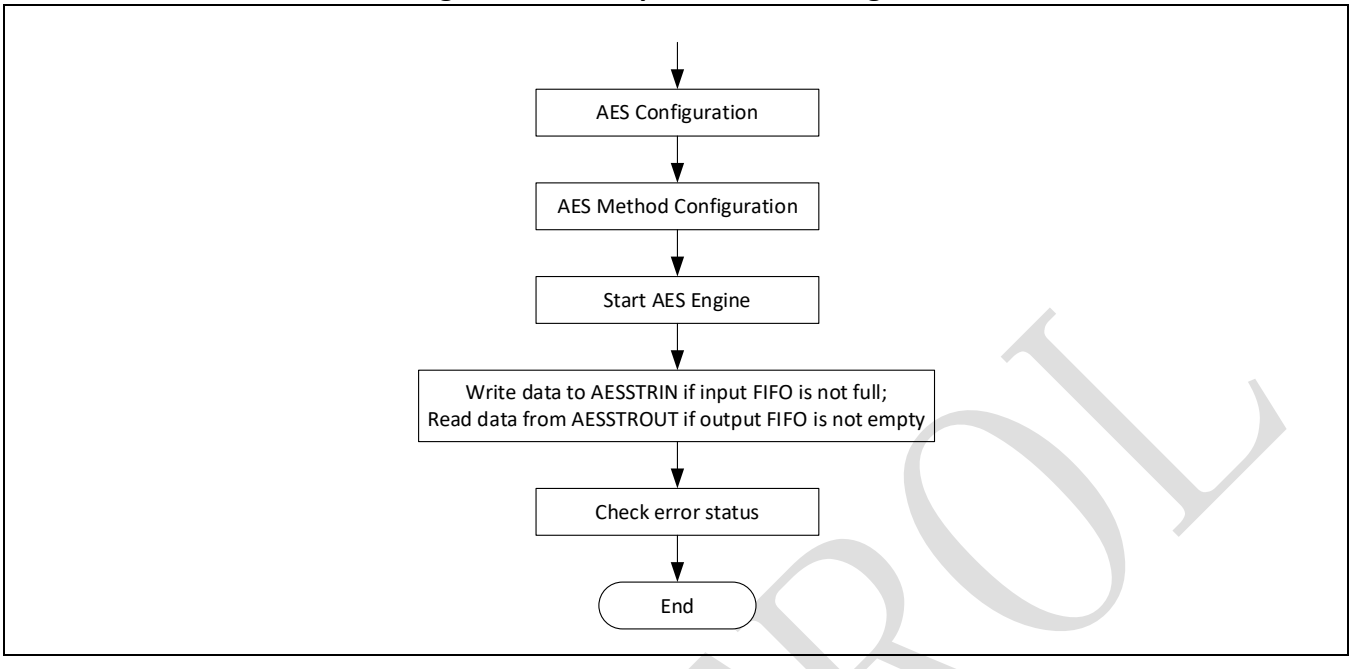
Figure 6-1: AES operation flow diagram



AES operation pseudo code

```
AES_Config_Type aesConfig

aesConfig.mode <- AES_MODE_CBC
aesConfig.encDecSel <- AES_MODE_ENCRYPTION
aesConfig.keySize <- keysize
aesConfig.mStrLen <- length

for i=1 to keysize do
aesConfig.key[i] = key[i]

for i=1 to 4 do
aesConfig.initVect[i] = vector[i]

while j<length or k<length do
if AES input fifo not full do
feed the data plain_text[j]
j++

if AES output fifo not empty do
read the encryption data
k++
```

6.2.2 AES configuration

Ensure correct configuration before starting the AES engine by following these steps:

- Set AES engine to encrypt or decrypt by clearing/setting AESCTL0.DECRYPTEN
- Configure AES block cipher mode by setting AESCTL0.MODE, 0 for ECB mode, 1 for CBC mode, 2 for CTR mode, 5 for CCM* mode, 6 for MMO mode and 7 for BYPASS mode

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- Configure AES key size. AES engine supports three types of key size: 128-, 192-, and 256- bit. Configure AES key size parameter by setting AESCTL0.KEYSIZE.
- Fill the key according to key size. AES engine contains eight 32-bit key registers defined as AESKEY0~7.
  - When key size is set to 128-bit, then AESKEY7/6/5/4 is used.
  - When the key size is set to 192-bit, then AESKEY7/6/5/4/3/2 is used.
  - When key size is set to 192-bit, then AESKEY7/6/5/4/3/2 is used.
  - When key size is set to 256-bit, then AESKEY7/6/5/4/3/2/1/0 is used.
  - MMO does not support 192- and 256- bit key size, and key size is ignored in Bypass mode.
- For all modes except CCM* mode, set input data size by setting AESMSTRLEN. For CCM* mode, set associate data size by setting AESASTRLEN, set message data size by setting AESMSTRLEN.
- If AES block cipher mode is CTR mode, set CTR mode's counter modular by setting AESCTL0.CTRMOD.
- For CCM* encryption or MMO mode, if MIC/HASH is needed, set AESCTL0.OUTMIC bit to 1 to append MIC/HASH at the end of output stream. If only MIC/HASH is needed, we can block the encrypted data into output FIFO (set AESCTL0.OUTMSG bit to 1), and get MIC/HASH from AESOV3/2/1/0.
- For CCM* encryption mode, set AESCTL0.OUTHDR bit to 1 to output B0 at the beginning of the output stream if it is necessary.
- Fill with initial value according to AES block cipher mode. AES engine contains four 32-bit initial vector registers naming by AESIV0/1/2/3.
  - ECB/MMO/BYPASS mode:
    No initial vectors needed to be configured.
  - CTR mode:
    Set AESIV0 = initial counter
    Set AESIV1 = Nonce[31:0]
    Set AESIV2 = Nonce[63:32]
    Set AESIV3 = Nonce[95:64]
  - For CCM* mode
    Set AESIV0 = Nonce[31:0]
    Set AESIV1 = Nonce[63:32]
    Set AESIV2 = Nonce[95:64]
    Set AESIV3[7:0] = Nonce[103:96]
    Set AESIV3[15:8] = [15-(Length of Nonce Bytes)]

Note: For Bypass mode, the AES engine ignores the input data; it passes it along unchanged to the output.

6.2.3 Data access method

The AES module contains separate 4*32-bit input and output FIFO. The input and output FIFO can be accessed by CPU.

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The CPU writes data into AESSTRIN if the input FIFO is not full; read data from AESSTROUT if output FIFO is not empty. The AES operation finishes as the transfer data size reaches input and output data size.

6.2.4 Starting the AES engine

Clear AES input and output FIFO and reset AES core before starting the AES engine. The AES input and output FIFO can be cleared by setting the AESCTL0.IFIFOCLR bit and AESCTL0.OFIFOCLR bit to 1.

6.2.5 Interrupt request

There are three interrupts for the AES engine: input FIFO full interrupt, output FIFO empty interrupt and AES operation done interrupt. Each interrupt can be enabled or cleared by setting AESIE/AESIC registers.

6.2.6 Partial code support

The AES engine can automatically pad the input data when the input data length is not multiple of 128 bits. The AES module supports the following padding scheme for different AES block cipher modes as shown in Table 6-1.

Table 6-1: Padding scheme

Mode	Description
CCM*	Automatically padding 0 for both A string and M string
MMO	Automatically padding “100…00”+2 bytes length information
CBC	Cipher stealing is performed to partial code word, which is proprietary, not according to NIST standard specification
CTR	Partial code word don’t affect the operation
ECB	Check partial case, assert error when partial cases detected

6.2.7 Error status check

Register AESSTS.ERRCODE records the error status for the AES engine when the AES operation has finished. Table 6-2 shows the error code for different AES block cipher modes.

Table 6-2: Error code for different AES block cipher modes

Mode	ERRCODE[2]	ERRCODE [1]	ERRCODE [0]
ECB	N/A	Data is not multiple of 16 bytes	Input data size less than 16 bytes
CBC	N/A	N/A	
CTR	N/A	N/A	
CCM*	MIC mismatch during decryption	N/A	N/A
MMO	N/A	Data is more than 2^{13}-1 bytes	N/A
Bypass	N/A	N/A	N/A

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6.2.8 Output vector

The output vector provides some useful information, such as the last cipher block in CBC mode, last counter in CTR mode, MIC value in CCM* mode and HASH value in MMO mode. Register AESOV3/2/1/0 records useful information for different AES block cipher modes. Table 6-3 shows the recorded information in AES output vector for different AES block cipher mode.

Table 6-3: AES output vector

Block Cipher Mode	Output Vector
ECB	N/A
CBC	Last cipher block AESOV0 = cipher[31:0] AESOV1 = cipher[63:32] AESOV2 = cipher[95:64] AESOV3 = cipher[127:96]
CTR	Last counter AESOV0 = counter[31:0] AESOV1 = counter[63:32] AESOV2 = counter[95:64] AESOV3 = counter[127:96]
CCM*	Encryption: MIC value. If MIC is less than 32 byte, always MSB byte is used. Example: 8 byte MIC AESOV2 = MIC[31:0] AESOV3 = MIC[63:32]
MMO	HASH value AESOV0 = HASH[31:0] AESOV1 = HASH[63:32] AESOV2 = HASH[95:64] AESOV3 = HASH[127:96]
Bypass	N/A

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6.3 Registers

6.3.1 AES register map

Table 6-4: AES Module Base Address

Peripheral Module	Base Address
AES	0x4000 8400

Table 6-5: AES Register Map

Register	Offset	Description	Reset Value
AESCTL0	0x00	AES Control Register 0	0x00004010
AESSTS	0x08	AES Status Register	0x00000081
AESASTRLEN	0x0C	AES Associate String Length Register	0x00000000
AESMSTRLEN	0x10	AES Message String Length Register	0x00000000
AESSTRIN	0x14	AES Input Message Word Register	0x00000000
AESIV0	0x18	AES Initial Vector Register 0	0x00000000
AESIV1	0x1C	AES Initial Vector Register 1	0x00000000
AESIV2	0x20	AES Initial Vector Register 2	0x00000000
AESIV3	0x24	AES Initial Vector Register 3	0x00000000
AESKEY0	0x28	AES Key Register 0	0x00000000
AESKEY1	0x2C	AES Key Register 1	0x00000000
AESKEY2	0x30	AES Key Register 2	0x00000000
AESKEY3	0x34	AES Key Register 3	0x00000000
AESKEY4	0x38	AES Key Register 4	0x00000000
AESKEY5	0x3C	AES Key Register 5	0x00000000
AESKEY6	0x40	AES Key Register 6	0x00000000
AESKEY7	0x44	AES Key Register 7	0x00000000
AESSTROUT	0x48	AES Output Message Word Register	0x00000000
AESOV0	0x4C	AES Output Vector Register 0	0x00000000
AESOV1	0x50	AES Output Vector Register 1	0x00000000
AESOV2	0x54	AES Output Vector Register 2	0x00000000
AESOV3	0x58	AES Output Vector Register 3	0x00000000
AESIF	0x5C	AES Interrupt Status Register	0x00000000
AESIE	0x60	AES Interrupt Enable Register	0x00000000
AESRAWIF	0x64	AES Interrupt Raw Status Register	0x00000000
AESIC	0x68	AES Interrupt Clear Register	0x00000000

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6.3.2 AES registers

6.3.2.1 AES Control Register 0 (AESCTL0)

Table 6-6: AES Control Register 0 (AESCTL0) Layout

AESCTL0 (AES Control Register 0) Offset: 0x0 Default: 0x00004010
Access: AES -> AESCTL0.all

31	30	29	28	27	26	25	24
RESERVED						CTRMOD	
23	22	21	20	19	18	17	16
CTRMOD					MODE		
15	14	13	12	11	10	9	8
DECRYPTEN	OUTMIC	MICLEN		KEYSIZE		RESERVED	RESERVED
7	6	5	4	3	2	1	0
RESERVED		OUTHDR	OUTMSG	OFIFOCLR	IFIFOCLR	RESERVED	START

Table 6-7: AES Control Register 0 (AESCTL0) Field Description

Bits	Field Name	Type	Reset	Description
31:26	RESERVED_31_26	RO	0x0	Reserved
25:19	CTRMOD	RW	0x0	CTR mode's counter modular 000xxxx: modular = 2^{128} Others: modular = $2^{CTRMODE}$
18:16	MODE	RW	0x0	AES running mode 000: ECB 001: CBC 010: CTR 011: RESERVED 100: RESERVED 101: CCM* 110: MMO 111: BYPASS
15	DECRYPTEN	RW	0x0	Decrypt operation. Ignored in MMO and BYPASS Mode. 0: Encryption 1: Decryption
14	OUTMIC	RW	0x1	Append MIC/HASH at the end of output stream in CCM* mode encryption/MMO mode. 0: Not append MIC/HASH at the end of output stream in CCM* mode encryption or MMO mode 1: Append MIC/HASH at the end of output stream in CCM* mode encryption or MMO mode
13:12	MICLEN	RW	0x0	Length of MIC field 00: 0 bytes 01: 4 bytes

SPINTROL

Bits	Field Name	Type	Reset	Description
				10: 8 bytes 11: 16 bytes
11:10	KEYSIZE	RW	0x0	Key size parameter 00: 16 bytes 01: 32 bytes 10: 24 bytes 11: Invalid
9	RESERVED_9	RW	0x0	Reserved
8	RESERVED_8	RW	0x0	Reserved
7:6	RESERVED_7_6	RO	0x0	Reserved
5	OUTHDR	RW	0x0	Output B0 and l(a) in CCM* mode 0: Don't output B0 and l(a) at the beginning of output stream 1: Output B0 and l(a) at the beginning of output stream
4	OUTMSG	RW	0x1	Output stream to output FIFO 0: Block output stream from output FIFO 1: Forward output stream to output FIFO
3	OFIFOCLR	W1C	0x0	Clear output FIFO 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears output FIFO This bit is self-cleared to 0
2	IFIFOCLR	W1C	0x0	Clear input FIFO 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears input FIFO This bit is self-cleared to 0
1	RESERVED_1	RO	0x0	Reserved
0	START	W1S	0x0	Start AES 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 starts AES operation This bit is self-cleared to 0

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6.3.2.2 AES Status Register (AESSTS)

Table 6-8: AES Status Register (AESSTS) Layout

AESSTS (AES Status Register) Offset: 0x8 Default: 0x00000081
Access: AES -> AESSTS.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED				OFIFODEPTH			IFIFODEPTH
15	14	13	12	11	10	9	8
IFIFODEPTH		ERRCODE			RESERVED		
7	6	5	4	3	2	1	0
OFIFOEMPTY	OFIFORDY	RESERVED	IFIFOFULL	RESERVED			DONE

Table 6-9: AES Status Register (AESSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19:17	OFIFODEPTH	RO	0x0	The output FIFO depth
16:14	IFIFODEPTH	RO	0x0	The input FIFO depth
13:11	ERRCODE	RO	0x0	AES operation error status 000: No operation error 001: Input stream size less than 16 byte in ECB, CBC and CTR mode 010: Data is not multiple of 16 bytes in ECB mode or Data is more than 2^{13}-1 bytes in MMO mode 011: Data is not multiple of 16 bytes and less than 16 bytes in ECB mode 100: MIC Mismatch during CCM* Decryption Others: Not valid
10:8	RESERVED_10_8	RO	0x0	Reserved
7	OFIFOEMPTY	RO	0x1	Output FIFO empty 0: Output FIFO is not empty 1: Output FIFO is empty
6	OFIFORDY	RO	0x0	Output FIFO is ready to read 0: Output FIFO is not ready to read 1: Output FIFO is ready to read
5	RESERVED_5	RO	0x0	Reserved
4	IFIFOFULL	RO	0x0	Input FIFO full 0: Input FIFO is not full 1: Input FIFO is full
3:1	RESERVED_3_1	RO	0x0	Reserved
0	DONE	RO	0x1	AES operation done 0: AES operation has not done yet 1: AES operation done

SPINTROL

6.3.2.3 AES Associate String Length Register (AESASTRLEN)

Table 6-10: AES Associate String Length Register (AESASTRLEN) Layout

AESASTRLEN (AES Associate String Length Register) Offset: 0xC Default: 0x00000000 Access: AES -> AESASTRLEN.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-11: AES Associate String Length Register (AESASTRLEN) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Size of associate string

6.3.2.4 AES Message String Length Register (AESMSTRLEN)

Table 6-12: AES Message String Length Register (AESMSTRLEN) Layout

AESMSTRLEN (AES Message String Length Register) Offset: 0x10 Default: 0x00000000 Access: AES -> AESMSTRLEN.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-13: AES Message String Length Register (AESMSTRLEN) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Size of message string

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6.3.2.5 AES Input Message Word Register (AESSTRIN)

Table 6-14: AES Input Message Word Register (AESSTRIN) Layout

AESSTRIN (AES Input Message Word Register) Offset: 0x14 Default: 0x00000000 Access: AES -> AESSTRIN.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-15: AES Input Message Word Register (AESSTRIN) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	WO	0x0	Input message word

6.3.2.6 AES Initial Vector Register 0 (AESIV0)

Table 6-16: AES Initial Vector Register 0 (AESIV0) Layout

AESIV0 (AES Initial Vector Register 0) Offset: 0x18 Default: 0x00000000 Access: AES -> AESIV0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-17: AES Initial Vector Register 0 (AESIV0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 0-3 of initial vector

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6.3.2.7 AES Initial Vector Register 1 (AESIV1)

Table 6-18: AES Initial Vector Register 1 (AESIV1) Layout

AESIV1 (AES Initial Vector Register 1) Offset: 0x1C Default: 0x00000000 Access: AES -> AESIV1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-19: AES Initial Vector Register 1 (AESIV1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 4-7 of initial vector

6.3.2.8 AES Initial Vector Register 2 (AESIV2)

Table 6-20: AES Initial Vector Register 2 (AESIV2) Layout

AESIV2 (AES Initial Vector Register 2) Offset: 0x20 Default: 0x00000000 Access: AES -> AESIV2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-21: AES Initial Vector Register 2 (AESIV2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 8-11 of initial vector

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6.3.2.9 AES Initial Vector Register 3 (AESIV3)

Table 6-22: AES Initial Vector Register 3 (AESIV3) Layout

AESIV3 (AES Initial Vector Register 3) Offset: 0x24 Default: 0x00000000 Access: AES -> AESIV3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-23: AES Initial Vector Register 3 (AESIV3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 12-15 of initial vector

6.3.2.10 AES Key Register 0 (AESKEY0)

Table 6-24: AES Key Register 0 (AESKEY0) Layout

AESKEY0 (AES Key Register 0) Offset: 0x28 Default: 0x00000000 Access: AES -> AESKEY0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-25: AES Key Register 0 (AESKEY0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 0-3 of key

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6.3.2.11 AES Key Register 1 (AESKEY1)

Table 6-26: AES Key Register 1 (AESKEY1) Layout

AESKEY1 (AES Key Register 1) Offset: 0x2C Default: 0x00000000 Access: AES -> AESKEY1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-27: AES Key Register 1 (AESKEY1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 4-7 of key

6.3.2.12 AES Key Register 2 (AESKEY2)

Table 6-28: AES Key Register 2 (AESKEY2) Layout

AESKEY2 (AES Key Register 2) Offset: 0x30 Default: 0x00000000 Access: AES -> AESKEY2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-29: AES Key Register 2 (AESKEY2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 8-11 of key

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6.3.2.13 AES Key Register 3 (AESKEY3)

Table 6-30: AES Key Register 3 (AESKEY3) Layout

AESKEY3 (AES Key Register 3) Offset: 0x34 Default: 0x00000000 Access: AES -> AESKEY3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-31: AES Key Register 3 (AESKEY3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 12-15 of key

6.3.2.14 AES Key Register 4 (AESKEY4)

Table 6-32: AES Key Register 4 (AESKEY4) Layout

AESKEY4 (AES Key Register 4) Offset: 0x38 Default: 0x00000000 Access: AES -> AESKEY4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-33: AES Key Register 4 (AESKEY4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte of 16-19 of key

SPINTROL

6.3.2.15 AES Key Register 5 (AESKEY5)

Table 6-34: AES Key Register 5 (AESKEY5) Layout

AESKEY5 (AES Key Register 5) Offset: 0x3C Default: 0x00000000 Access: AES -> AESKEY5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-35: AES Key Register 5 (AESKEY5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 20-23 of key

6.3.2.16 AES Key Register 6 (AESKEY6)

Table 6-36: AES Key Register 6 (AESKEY6) Layout

AESKEY6 (AES Key Register 6) Offset: 0x40 Default: 0x00000000 Access: AES -> AESKEY6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-37: AES Key Register 6 (AESKEY6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 24-27 of key

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6.3.2.17 AES Key Register 7 (AESKEY7)

Table 6-38: AES Key Register 7 (AESKEY7) Layout

AESKEY7 (AES Key Register 7) Offset: 0x44 Default: 0x00000000 Access: AES -> AESKEY7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-39: AES Key Register 7 (AESKEY7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Byte 28-31 of key

6.3.2.18 AES Output Message Word Register (AESSTROUT)

Table 6-40: AES Output Message Word Register (AESSTROUT) Layout

AESSTROUT (AES Output Message Word Register) Offset: 0x48 Default: 0x00000000 Access: AES -> AESSTROUT.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-41: AES Output Message Word Register (AESSTROUT) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Output message word

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6.3.2.19 AES Output Vector Register 0 (AESOV0)

Table 6-42: AES Output Vector Register 0 (AESOV0) Layout

AESOV0 (AES Output Vector Register 0) Offset: 0x4C Default: 0x00000000 Access: AES -> AESOV0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-43: AES Output Vector Register 0 (AESOV0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Byte 0-3 of output vector

6.3.2.20 AES Output Vector Register 1 (AESOV1)

Table 6-44: AES Output Vector Register 1 (AESOV1) Layout

AESOV1 (AES Output Vector Register 1) Offset: 0x50 Default: 0x00000000 Access: AES -> AESOV1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-45: AES Output Vector Register 1 (AESOV1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Byte 4-7 of output vector

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6.3.2.21 AES Output Vector Register 2 (AESOV2)

Table 6-46: AES Output Vector Register 2 (AESOV2) Layout

AESOV2 (AES Output Vector Register 2) Offset: 0x54 Default: 0x00000000 Access: AES -> AESOV2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-47: AES Output Vector Register 2 (AESOV2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Byte 8-11 of output vector

6.3.2.22 AES Output Vector Register 3 (AESOV3)

Table 6-48: AES Output Vector Register 3 (AESOV3) Layout

AESOV3 (AES Output Vector Register 3) Offset: 0x58 Default: 0x00000000 Access: AES -> AESOV3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 6-49: AES Output Vector Register 3 (AESOV3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Byte 12-15 of output vector

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6.3.2.23 AES Interrupt Status Register (AESIF)

Table 6-50: AES Interrupt Status Register (AESIF) Layout

AESIF (AES Interrupt Status Register) Offset: 0x5C Default: 0x00000000 Access: AES -> AESIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					OFIFOEMPTY	IFIFOFULL	DONE

Table 6-51: AES Interrupt Status Register (AESIF) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	OFIFOEMPTY	RO	0x0	Status of AES output FIFO empty interrupt 0: AES output FIFO empty interrupt not occurred 1: AES output FIFO empty interrupt occurred
1	IFIFOFULL	RO	0x0	Status of AES input FIFO full interrupt 0: AES input FIFO full interrupt not occurred 1: AES input FIFO full interrupt occurred
0	DONE	RO	0x0	Status of AES operation done interrupt 0: AES operation done interrupt not occurred 1: AES operation done interrupt occurred

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6.3.2.24 AES Interrupt Enable Register (AESIE)

Table 6-52: AES Interrupt Enable Register (AESIE) Layout

AESIE (AES Interrupt Enable Register) Offset: 0x60 Default: 0x00000000 Access: AES -> AESIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					OFIFOEMPTY	IFIFOFULL	DONE

Table 6-53: AES Interrupt Enable Register (AESIE) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	OFIFOEMPTY	RW	0x0	Enable AES output FIFO empty interrupt 0: Disable AES output FIFO empty interrupt 1: Enable AES output FIFO empty interrupt
1	IFIFOFULL	RW	0x0	Enable of AES input FIFO full interrupt 0: Disable AES input FIFO full interrupt 1: Enable AES input FIFO full interrupt
0	DONE	RW	0x0	Enable of AES operation done interrupt 0: Disable AES operation done interrupt 1: Enable AES operation done interrupt

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6.3.2.25 AES Interrupt Raw Status Register (AESRAWIF)

Table 6-54: AES Interrupt Raw Status Register (AESRAWIF) Layout

AESRAWIF (AES Interrupt RAW status Register) Offset: 0x64 Default: 0x00000000 Access: AES -> AESRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					OFIFOEMPTY	IFIFOFULL	DONE

Table 6-55: AES Interrupt Raw Status Register (AESRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	OFIFOEMPTY	RO	0x0	AES output FIFO empty interrupt raw status regardless of mask 0: AES output FIFO empty interrupt not occurred 1: AES output FIFO empty interrupt
1	IFIFOFULL	RO	0x0	AES input FIFO full interrupt raw status regardless of mask 0: AES no input FIFO full interrupt not occurred 1: AES no input FIFO full interrupt occurred
0	DONE	RO	0x0	AES operation done interrupt raw status regardless of mask 0: AES operation done interrupt not occurred 1: AES operation done interrupt occurred

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6.3.2.26 AES Interrupt Clear Register (AESIC)

Table 6-56: AES Interrupt Clear Register (AESIC) Layout

AESIC (AES Interrupt Clear Register) Offset: 0x68 Default: 0x00000000 Access: AES -> AESIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					OFIFOEMPTY	IFIFOFULL	DONE

Table 6-57: AES Interrupt Clear Register (AESIC) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	OFIFOEMPTY	W1C	0x0	Clearance of AES output FIFO empty interrupt status and raw status 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both AES output FIFO empty interrupt status and raw status This bit is self-cleared to 0
1	IFIFOFULL	W1C	0x0	Clearance of AES input FIFO full interrupt status and raw status 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both AES input FIFO full interrupt status and raw status This bit is self-cleared to 0
0	DONE	W1C	0x0	Clearance of AES operation done interrupt status and raw status 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both AES operation done interrupt status and raw status This bit is self-cleared to 0

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7 CRC

7.1 CRC overview

A Cyclic Redundancy Check (CRC) or polynomial code checksum is a hash function designed to detect accidental changes to raw computer data, and is used to verify data transmission or storage generates up to 32-bit CRC code for error detection.

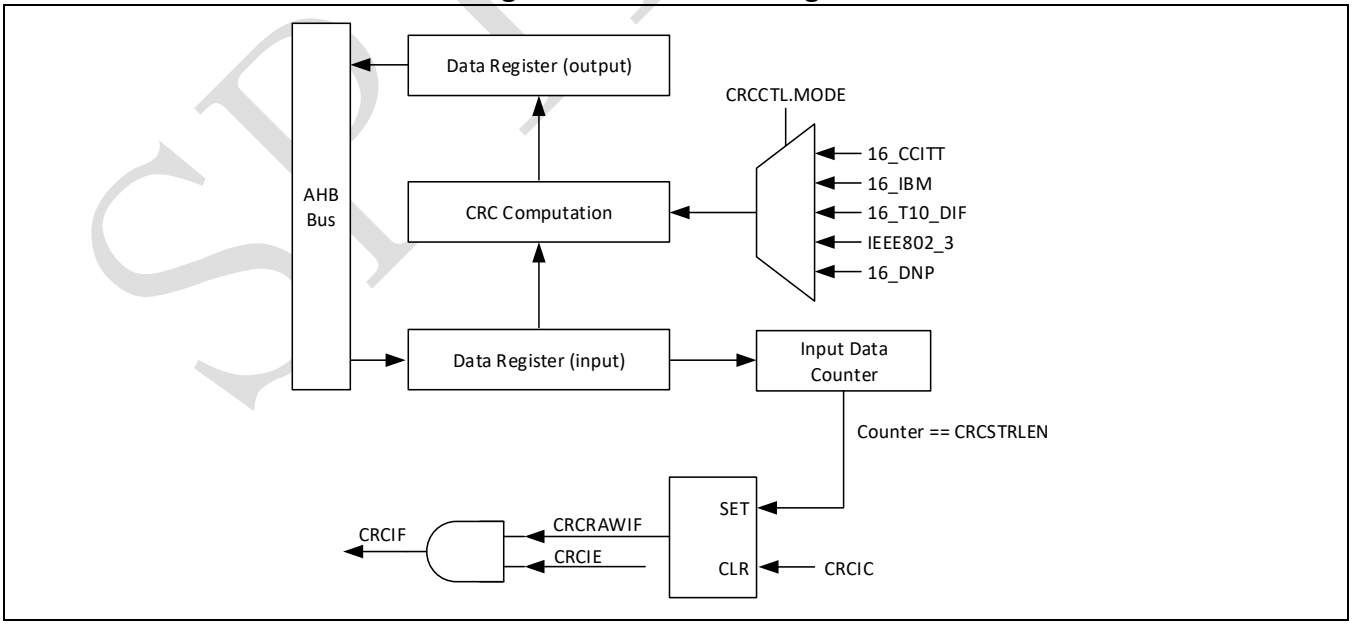
7.2 Main features

A standard AHB slave interface is used to configure the module, receive the bit stream, and output the CRC result. The CRC module supports the following features:

- Supports 32-bit parallel bit stream input, and supports up to 32-bit CRC output
- Supports up to 2^{32}(4294967296) byte length to calculate CRC
- Supports the following CRC standards
- CRC-16-CCITT, the polynomial is $x^{16}+x^{12}+x^5+1$
- CRC-16-IBM, the polynomial is $x^{16}+x^{15}+x^2+1$
- CRC-16-T10-DIF, the polynomial is $x^{16}+x^{15}+x^{11}+x^9+x^8+x^7+x^5+x^4+x^2+1$
  - CRC-32-IEEE 802.3, the polynomial is
- $X^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$
- CRC-16-DNP, the polynomial is $x^{16}+x^{13}+x^{12}+x^{11}+x^{10}+x^8+x^6+x^5+x^2+1$

The block diagram is shown in Figure 7-1.

Figure 7-1: CRC block diagram



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7.3 CRC operation flow

User can operate the CRC module according to the following steps:

Step 1: Disable CRC (Set CRCCTL.EN to 0).

Step 2: Disable the interrupt (Set CRCIE.DONE to 0).

Step 3: Clear all the interrupts (Set CRCIC.DONE to 1).

Step 4: Configure the stream length (Set register CRCSTRLEN).

Step 5: Configure CRC mode (Set bit CRCCTL.MODE).

Step 6: Enable the interrupt (Set CRCIE.DONE to 1).

Step 7: Enable CRC (Set CRCCTL.EN to 1).

Step 8: Write stream in and waiting for interrupt to occur (If interrupt occurred, go to Step 9).

Step 9: Get CRC calculation result (Read register CRCRESULT).

Step 10: CRC operation complete.

Note: The CRC input stream registers accepts a word (32 bit) at a time. If the input data is not 4 bytes aligned, pad zeros at the start of the data stream. For example, if the data stream consists of 5 bytes starting from the lower address: 0xA1, 0xA2, 0xA3, 0xA4, 0xA5, the following two words should be written to the stream input register:

- 0xA1000000
- 0xA5A4A3A2

The CRC result bit order is:

- 16 bit CRC: x_0~x_{15} [MSB->LSB]
- 32 bit CRC: x_0~x_{31} [MSB->LSB]

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7.4 Registers

7.4.1 CRC register map

Table 7-1: CRC Module Base Address

Peripheral Module	Base Address
CRC	0x4000 8000

Table 7-2: CRC Register Map

Register	Offset	Description	Reset Value
CRCIF	0x00	CRC Interrupt Flag Register	0x00000000
CRCRAWIF	0x04	CRC Raw Interrupt Flag Register	0x00000000
CRCIC	0x08	CRC Interrupt Clear Register	0x00000000
CRCIE	0x0C	CRC Interrupt Enable Register	0x00000000
CRCCTL	0x10	CRC Control Register	0x00000000
CRCSTRLEN	0x14	CRC Stream Length Register	0x00000000
CRCSTRIN	0x18	CRC Stream Input Register	0x00000000
CRCRESULT	0x1C	CRC Result Register	0x00000000

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7.4.2 CRC registers

7.4.2.1 CRC Interrupt Flag Register (CRCIF)

Table 7-3: CRC Interrupt Flag Register (CRCIF) Layout

CRCIF (CRC Interrupt Flag Register) Offset: 0x0 Default: 0x00000000 Access: CRC -> CRCIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							DONE

Table 7-4: CRC Interrupt Flag Register (CRCIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	DONE	RO	0x0	CRC calculation done interrupt status after mask 0: Interrupt is not occurred 1: Interrupt is occurred

7.4.2.2 CRC Raw Interrupt Flag Register (CRCRAWIF)

Table 7-5: CRC Raw Interrupt Flag Register (CRCRAWIF) Layout

CRCRAWIF (CRC Raw Interrupt Flag Register) Offset: 0x4 Default: 0x00000000 Access: CRC -> CRCRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							DONE

Table 7-6: CRC RAW Interrupt Flag Register (CRCRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	DONE	RO	0x0	CRC calculation done interrupt raw status regardless of mask 0: Interrupt is not occurred 1: Interrupt is occurred

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7.4.2.3 CRC Interrupt Clear Register (CRCIC)

Table 7-7: CRC Interrupt Clear Register (CRCIC) Layout

CRCIC (CRC Interrupt Clear Register) Offset: 0x8 Default: 0x00000000 Access: CRC -> CRCIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							DONE

Table 7-8: CRC Interrupt Clear Register (CRCIC) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	DONE	W1C	0x0	Clearance of CRCIF and CRCRAWIF 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear CRCIF and CRCRAWIF This bit is self-cleared to 0

7.4.2.4 CRC Interrupt Enable Register (CRCIE)

Table 7-9: CRC Interrupt Enable Register (CRCIE) Layout

CRCIE (CRC Interrupt Enable Register) Offset: 0xC Default: 0x00000000 Access: CRC -> CRCIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							DONE

Table 7-10: CRC Interrupt Enable Register (CRCIE) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	DONE	RW	0x0	Enable interrupt triggered by CRCRAWIF 0: Disable generation of IRQ and corresponding CRCIF 1: Enable generation of IRQ and corresponding CRCIF

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7.4.2.5 CRC Control Register (CRCCTL)

Table 7-11: CRC Control Register (CRCCTL) Layout

CRCCTL (CRC Control Register) Offset: 0x10 Default: 0x00000000 Access: CRC -> CRCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				MODE			EN

Table 7-12: CRC Control Register (CRCCRL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3:1	MODE	RW	0x0	CRC mode select 000: $x^{16}+x^{12}+x^5+1$ (CRC-16-CCITT, CRC-CCITT) 001: $x^{16}+x^{15}+x^2+1$ (CRC-16, CRC-16-IBM, CRC-16-ANSI) 010: $x^{16}+x^{15}+x^{11}+x^9+x^8+x^7+x^5+x^4+x^2+x+1$ (CRC-16-T10-DIF) 011: $x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$ (CRC-32-IEEE802.3) 100: $x^{16}+x^{13}+x^{12}+x^{11}+x^{10}+x^8+x^6+x^5+x^2+1$(CRC-16-DNP) 101: Reserved 110: Reserved 111: Reserved
0	EN	RW	0x0	CRC calculate enable 0: Disable CRC calculation 1: Enable CRC calculation, it is automatically cleared when the CRC calculation is finished

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7.4.2.6 CRC Stream Length Register (CRCSTRLEN)

Table 7-13: CRC Stream Length Register (CRCSTRLEN) Layout

CRCSTRLEN (CRC Stream Length Register) Offset: 0x14 Default: 0x00000000 Access: CRC -> CRCSTRLEN.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 7-14: CRC Stream Length Register (CRCSTRLEN) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Input stream length minus 1(in unit of byte)

7.4.2.7 CRC Stream Input Register (CRCSTRIN)

Table 7-15: CRC Stream Input Register (CRCSTRIN) Layout

CRCSTRIN (CRC Stream Input Register) Offset: 0x18 Default: 0x00000000 Access: CRC -> CRCSTRIN.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 7-16: CRC Stream Input Register (CRCSTRIN) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Stream Input data register

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7.4.2.8 CRC Result Register (CRCRESULT)

Table 7-17: CRC Result Register (CRCRESULT) Layout

CRCRESULT (CRC Result Register) Offset: 0x1C Default: 0x00000000 Access: CRC -> CRCRESULT.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 7-18: CRC Result Register (CRCRESULT) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	CRC calculation result

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8 General-purpose timers

8.1 Timer overview

The SPC2168 includes three 32-bit General Purpose Timers (GPT) with following features:

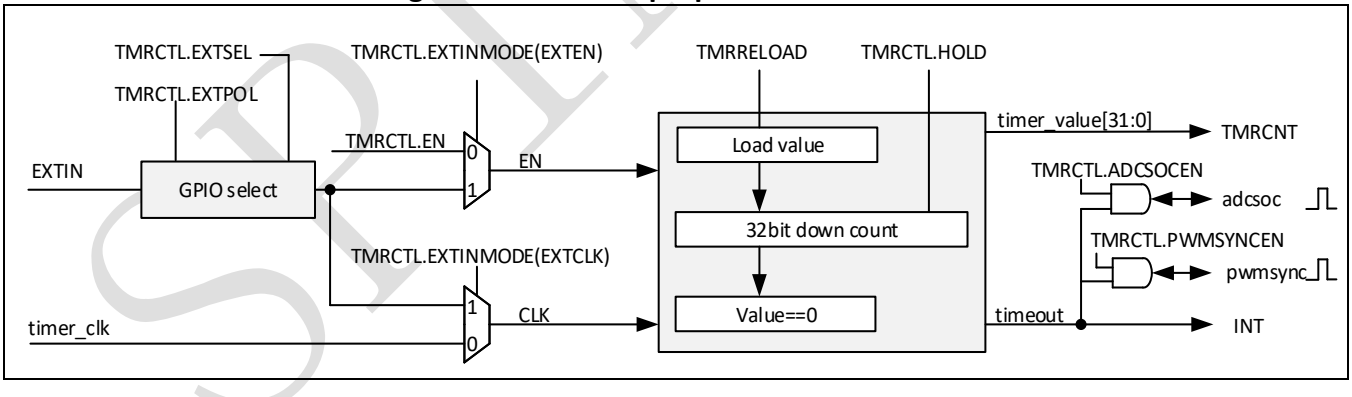
- APB register interface
- Dedicated timer clock, shown in Figure 3-13
- 32-bit down-counter
- Generate interrupt upon counter reaches zero
- Generate ADCSOC event upon counter reaches zero
- Generate PWMSYNCI event upon counter reaches zero
- Capture external input as timer enable
- Capture external input as timer clock

8.2 Functional description

Each GPT operates under periodic timer mode. As shown in Figure 8-1, when the timer is enabled, the counter loads the value from TMRRELOAD register and starts to count down until it reaches 0. Then the counter restarts from the reload value and decrease again. Upon the counter equals 0:

- An interrupt will be generated if it is enabled. The interrupt flag held until it is manually cleared
- An ADCSOC event will be generated if TMRCTL.ADCSOCEN is enabled
- A PWMSYNCI event will be generated if TMRCTL.PWMSYNCEN is enabled

Figure 8-1: General-purpose timer structure



The low to high transition on external input (EXTIN) can be used as timer enable. It can also be used as external clock. The register TMRCTL.EXTSEL is used to select GPIO pin as the external input (EXTIN). Please see Table 8-3 and Table 8-4 for the details.

The timers are disabled by default after system reset.

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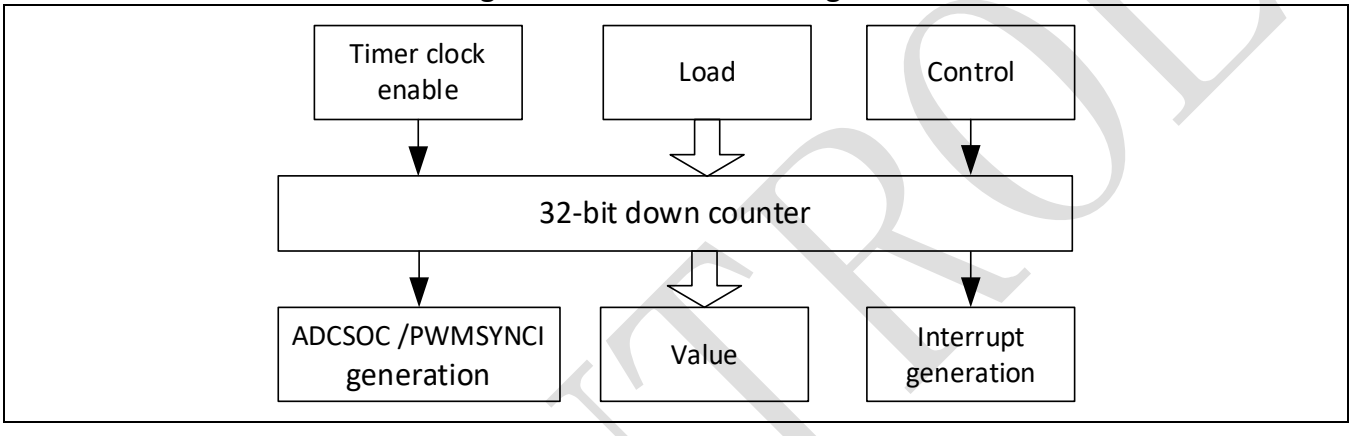
8.3 Initialization sequence

The following sequence of operations should be followed to start the timer.

- Disable the timer and clear timer interrupt
- Configure the timer reload value register (TMRRELOAD)
- Configure the timer control register (TMRCTL)
- Enable the timer to start the timer counter

A block diagram of the timer run mode is shown in Figure 8-2.

Figure 8-2: GPT run flow diagram



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8.4 Registers

8.4.1 TIMER register map

Table 8-1: Timer Module Base Address

Peripheral Module	Base Address
TIMER0	0x4000 7000
TIMER1	0x4000 7020
TIMER2	0x4000 7040

Table 8-2: Timer Register Map

Register	Offset	Description	Reset Value
TMRCTL	0x00	Timer Control Register	0x00000000
TMRCNT	0x04	Timer Counter Value Register	0x00000000
TMRRELOAD	0x08	Timer Reload Value Register	0x00000000
TMRIF	0x0C	Timer Interrupt Flag Register	0x00000000
TMRRAWIF	0x10	Timer Raw Interrupt Flag Register	0x00000000
TMRIE	0x14	Timer Interrupt Enable Register	0x00000000
TMRIFRC	0x18	Timer Interrupt Force Register	0x00000000
TMRIC	0x1C	Timer Interrupt Clear Register	0x00000000

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8.4.2 TIMER registers

8.4.2.1 Timer Control Register (TMRCTL)

Table 8-3: Timer Control Register (TMRCTL) Layout

TMRCTL (Timer Control Register) Offset: 0x0 Default: 0x00000000 Access: TIMER0 -> TMRCTL.all							
31	30	29	28	27	26	25	24
RESERVED_31_13							
23	22	21	20	19	18	17	16
RESERVED_31_13							
15	14	13	12	11	10	9	8
RESERVED_31_13			EXTSEL				
7	6	5	4	3	2	1	0
EXTSEL	EXTPOL	EXTINMODE		PWMSYNCEN	ADCSOCEN	RESERVED_1	EN

Table 8-4: Timer Control Register (TMRCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:13	RESERVED_31_13	RO	0x0	Reserved
12:7	EXTSEL	RW	0x0	External input source select (GPIO number)
6	EXTPOL	RW	0x0	External input polarity 0: Active low 1: Active high
5:4	EXTINMODE	RW	0x0	External input mode 00: Disable external input 01: Invalid 10: Take external input as timer clock 11: Take external input as timer enable
3	PWMSYNCEN	RW	0x0	PWMSYNCI generation enable 0: Do not generate PWMSYNCI 1: Generate PWMSYNCI whenever TMRCNT counts down to 0
2	ADCSOCEN	RW	0x0	ADCSOC generation enable 0: Do not generate ADCSOC 1: Generate ADCSOC whenever TMRCNT counts down to 0
1	RESERVED_1	RW	0x0	Reserved.
0	EN	RW	0x0	Timer enable 0: Disable Timer 1: Enable Timer

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8.4.2.2 Timer Counter Value Register (TMRCNT)

Table 8-5: Timer Counter Value Register (TMRCNT) Layout

TMRCNT (Timer Counter Value Register) Offset: 0x4 Default: 0x00000000 Access: TIMER -> TMRCNT.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 8-6: Timer Counter Value Register (TMRCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Current value of timer counter. When TMRCTL.EN=0, the value will remain unchanged.

8.4.2.3 Timer Reload Value Register (TMRRELOAD)

Table 8-7: Timer Reload Value Register (TMRRELOAD) Layout

TMRRELOAD (Timer Reload Value Register) Offset: 0x8 Default: 0x00000000 Access: TIMER -> TMRRELOAD.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 8-8: Timer Reload Value Register (TMRRELOAD) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reload value. A Write to this register also sets the current TMRCNT value.

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8.4.2.4 Timer Interrupt Flag Register (TMRIF)

Table 8-9: Timer Interrupt Flag Register (TMRIF) Layout

TMRIF (Timer Interrupt Flag Register) Offset: 0xC Default: 0x00000000 Access: TIMER -> TMRIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8-10: Timer Interrupt Flag Register (TMRIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	RO	0x0	Timer interrupt 0: Interrupt not occurred 1: Interrupt occurred and issued to CPU. No further interrupt will be issued until the flag is cleared

8.4.2.5 Timer Raw Interrupt Flag Register (TMRRAWIF)

Table 8-11: Timer Raw Interrupt Flag Register (TMRRAWIF) Layout

TMRRAWIF (Timer Raw Interrupt Flag Register) Offset: 0x10 Default: 0x00000000 Access: TIMER -> TMRRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8-12: Timer Raw Interrupt Flag Register (TMRRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	RO	0x0	Timer raw interrupt status. This bit is set whenever TMRCNT counts down to 0 and cleared only by writing a 1 to TMRIC 0: Interrupt not occurred 1: Interrupt occurred

SPINTROL

8.4.2.6 Timer Interrupt Enable Register (TMRIE)

Table 8-13: Timer Interrupt Enable Register (TMRIE) Layout

TMRIE (Timer Interrupt Enable Register) Offset: 0x14 Default: 0x00000000 Access: TIMER -> TMRIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8-14: Timer Interrupt Enable Register (TMRIE) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	RW	0x0	Timer interrupt enable. This bit does not affect TMRRAWIF and PWMSYNCI/ADCSOC generation 0: Do not issue interrupt to CPU 1: Issue interrupt whenever TMRRAWIF=1

8.4.2.7 Timer Interrupt Force Register (TMRIFRC)

Table 8-15: Timer Interrupt Force Register (TMRIFRC) Layout

TMRIFRC (Timer Interrupt Force Register) Offset: 0x18 Default: 0x00000000 Access: TIMER -> TMRIFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8-16: Timer Interrupt Force Register (TMRIFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	W1S	0x0	Timer interrupt software force 0: Write a 0 has no effect and always reads back 0 1: Write a 1 forces the TMRRAWIF flag. This bit is self-cleared to 0.

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8.4.2.8 Timer Interrupt Clear Register (TMRIC)

Table 8-17: Timer Interrupt Clear Register (TMRIC) Layout

TMRIC (Timer Interrupt Clear Register) Offset: 0x1C Default: 0x00000000 Access: TIMER -> TMRIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 8-18: Timer Interrupt Clear Register (TMRIC) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	W1C	0x0	Timer interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the TMRRAWIF and TMRIF flag. This bit is self-cleared to 0.

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9 Watchdog timers

9.1 Watchdog overview

The watchdog timer (WDT) regains control in case of system failure (due to a software error) to increase application reliability. The WDT can generate a reset or an interrupt when the counter reaches a given timeout value. The SPC2168 includes two 32-bit WDTs. Registers are controlled via AHB bus.

Each WDT has following features:

- APB register interface
- Dedicated WDT clock, shown in Figure 3-12
- 32-bit down-counter
- Configurable reset or interrupt generation with the given timeout value

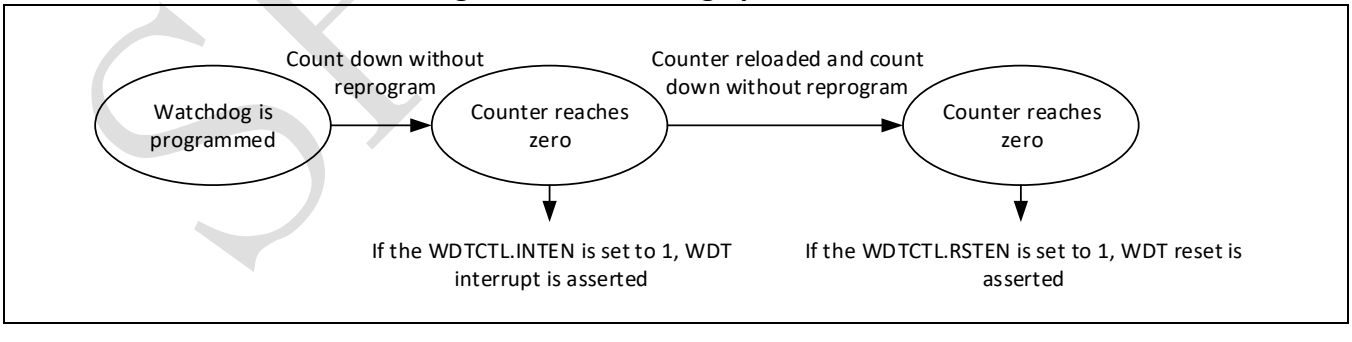
9.2 Functional description

The watchdog counter descends from a preset (timeout) value to zero. The timeout value is obtained by load register WDTLOAD, which should be written after reset and before the WDT is enabled. When the counter reaches zero, either a system reset or an interrupt occurs, depending on the set of the control register WDTCTL.

As a safety feature to prevent rogue software from disabling the watchdog functionality, writing a value of 0x1ACCE551 to WDTREGKEY register enables write access to all other registers, while writing any other value disables the write access. Before configuring the WDT operation, the write access to other registers should be enabled first.

Figure 9-1 shows the flow diagram for the watchdog operation. If the interrupt is enabled, the counter of WDT will be enabled and generate an interrupt when a timeout occurs. Then the counter reloads value from WDTLOAD and continues the count-down sequence. If the interrupt is not cleared by the time a second timeout occurs and the reset is enabled, it generates a system reset request.

Figure 9-1: Watchdog operation flow



When a writing to WDTLOAD occurs, the counter restarts from the new value immediately. When a writing to WDTIC occurs, the interrupt will be cleared and the counter restarts. If the restart occurs at the same time the watchdog counter reaches zero, the interrupt will not be generated. The WDT can be closed by configuring WDTCTL register when CPU in HALTED mode or LOCKUP mode.

Note: The WDT0 interrupt request signal is connected to the NMI interrupt.

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9.3 Initialization sequence

The following sequence of operations must be followed to start the watchdog timer:

- Configure the WDTREGKEY register to enable registers write
- Configure the WDTLOAD register for timeout value
- Configure the WDTCTL.RSTEN bit for reset setup
- Configure interrupt enable bit to start counter and enable interrupt
- Configure the WDTREGKEY Register disable registers write

SPINTROL

9.4 Registers

9.4.1 WDT register map

Table 9-1: WDT Module Base Address

Peripheral Module	Base Address
WDT0	0x4000 1000
WDT1	0x4000 2000

Table 9-2: WDT Register Map

Register	Offset	Description	Reset Value
WDTLOAD*	0x00	Watchdog Timer Load Register	0x003D0900
WDTCNT	0x04	Watchdog Timer Current Value Register	0xFFFFFFFF
WDTCTL*	0x08	Watchdog Timer Control Register	0x0000000F
WDTIC*	0x0C	Watchdog Timer Clear Interrupt Register	0x00000000
WDTRAWIF	0x10	Watchdog Timer Raw Interrupt Status Register	0x00000000
WDTIF	0x14	Watchdog Timer Interrupt Status Register	0x00000000
WDTREGKEY	0x18	Watchdog Timer Lock Register	0x00000000

Note: Registers marked with * are write-allowed only when the WDTREGKEY=0x1ACCE551.
LSB of all register readback will be 1 if WDTREGKEY is not 0x1ACCE551

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9.4.2 WDT registers

9.4.2.1 Watchdog Timer Load Register (WDTLOAD)

Table 9-3: Watchdog Timer Load Register (WDTLOAD) Layout

WDTLOAD (Watchdog Timer Load Register) Offset: 0x0 Default: 0x003D0900 Access: WDT -> WDTLOAD.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 9-4: Watchdog Timer Load Register (WDTLOAD) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x3D0900	Load value The value from which the counter is to decrease. When this register is written to, the count is immediately restarted from the new value. The minimum valid value is 1.

9.4.2.2 Watchdog Timer Current Value Register (WDTCNT)

Table 9-5: Watchdog Timer Current Value Register (WDTCNT) Layout

WDTCNT (Watchdog Timer Current Value Register) Offset: 0x4 Default: 0xFFFFFFFF Access: WDT -> WDTCNT.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 9-6: Watchdog Timer Current Value Register (WDTCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0xFFFFFFFF	Current value of the decrementing counter.

SPINTROL

9.4.2.3 Watchdog Timer Control Register (WDTCTL)

Table 9-7: Watchdog Timer Control Register (WDTCTL) Layout

WDTCTL (Watchdog Timer Control Register) Offset: 0x8 Default: 0x0000000F Access: WDT -> WDTCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				LOCKUPRUN	HALTEDRUN	RSTEN	INTEN

Table 9-8: Watchdog Timer Control Register (WDTCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	LOCKUPRUN	RW	0x1	Allow watchdog to run during core lockup mode 0: Disable watchdog when core is in lockup mode 1: Enable watchdog when core is in lockup mode
2	HALTEDRUN	RW	0x1	Allow watchdog to run during core halted mode 0: Disable watchdog when core is in halted mode 1: Enable watchdog when core is in halted mode
1	RSTEN	RW	0x1	Enable watchdog reset output. 0: Disable the reset request 1: Enable the reset request
0	INTEN	RW	0x1	Enable the interrupt event Reloads the counter from WDTLOAD upon a rising edge of this bit. 0: Disable the counter and the interrupt 1: Enable the counter and the interrupt

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9.4.2.4 Watchdog Timer Clear Interrupt Register (WDTIC)

Table 9-9: Watchdog Timer Clear Interrupt Register (WDTIC) Layout

WDTIC (Watchdog Timer Clear Interrupt Register) Offset: 0xC Default: 0x00000000 Access: WDT -> WDTIC.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 9-10: Watchdog Timer Clear Interrupt Register (WDTIC) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	WO	0x0	Interrupt clear register A write of any value to this register clears the watchdog interrupt, and reloads the counter from WDTLOAD.

9.4.2.5 Watchdog Timer Raw Interrupt Status Register (WDTRAWIF)

Table 9-11: Watchdog Timer Raw Interrupt Status Register (WDTRAWIF) Layout

WDTRAWIF (Watchdog Timer Raw Interrupt Status Register) Offset: 0x10 Default: 0x00000000 Access: WDT -> WDTRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							RAWINT

Table 9-12: Watchdog Timer Raw Interrupt Status Register (WDTRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	RAWINT	RO	0x0	Raw interrupt status from the counter This register indicates the raw interrupt status from the counter. The value is ANDed with WDTCTL.INTEN to create the masked interrupt, which is passed to the interrupt output pin. 0: Interrupt not occurred 1: Interrupt occurred

SPINTROL

9.4.2.6 Watchdog Timer Interrupt Status Register (WDTIF)

Table 9-13: Watchdog Timer Interrupt Status Register (WDTIF) Layout

WDTIF (Watchdog Timer Interrupt Status Register) Offset: 0x14 Default: 0x00000000 Access: WDT -> WDTIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							INT

Table 9-14: Watchdog Timer Interrupt Status Register (WDTIF) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	INT	RO	0x0	Masked interrupt status from the counter This register indicates the masked interrupt status from the counter. This value is the logical AND of WDTRAWIF.RAWINT and WDTCTL.INTEN, and is the same value that is passed to the interrupt output pin. 0: Interrupt not occurred 1: Interrupt occurred

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9.4.2.7 Watchdog Timer Lock Register (WDTREGKEY)

Table 9-15: Watchdog Timer Lock Register (WDTREGKEY) Layout

WDTREGKEY (Watchdog Timer Lock Register) Offset: 0x18 Default: 0x00000000 Access: WDT -> WDTREGKEY.all							
31	30	29	28	27	26	25	24
LCKCTL							
23	22	21	20	19	18	17	16
LCKCTL							
15	14	13	12	11	10	9	8
LCKCTL							
7	6	5	4	3	2	1	0
LCKCTL							LCKSTS

Table 9-16: Watchdog Timer Lock Register (WDTREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:1	LCKCTL	RW	0x0	Enable register writes Enable write access to all other registers by writing 0x1ACCE551 to the whole WDTLOCK register. Disable write access by writing any other value.
0	LCKSTS	RO	0x0	Register write lock status 0: write access to all other registers is enabled (not locked) 1: write access to all other registers is disabled (locked)

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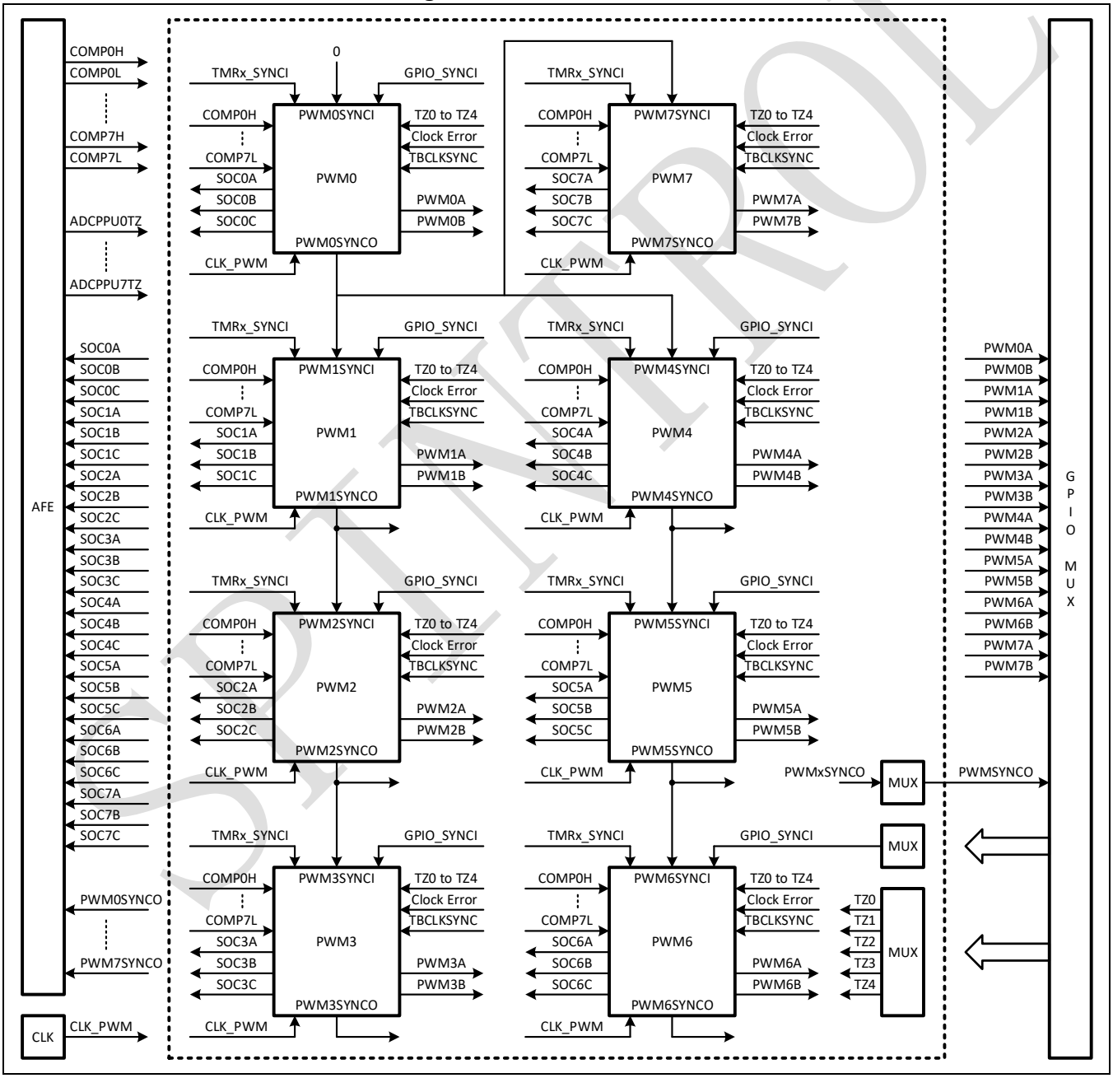
10 PWM

10.1 PWM overview

The PWM plays a key role in power electronic systems such as digital motor control, switch mode power supply control, and uninterruptible power supplies (UPS). The SPC2168 provides 8 PWM modules while each PWM has two outputs: PWMxA and PWMxB. They are chained together via a clock synchronization scheme as shown in Figure 10-1.

Figure 10-1: PWM overview



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Each PWM module supports the following features:

- 16-bit time-based counter with period and frequency control.
- Software override control of PWM signals.
- Independent and programmable phase-control support.
- Synchronized phase relationship on a cycle-by-cycle basis.
- Dead-band generation with independent rising and falling edge delay control.
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions.
- Either high, low, or high-impedance state logic levels can be forced at the PWM outputs on a trip condition.
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions.
- All events can trigger both CPU interrupt and ADC start of conversion (SOC).

Figure 10-2: PWM architecture

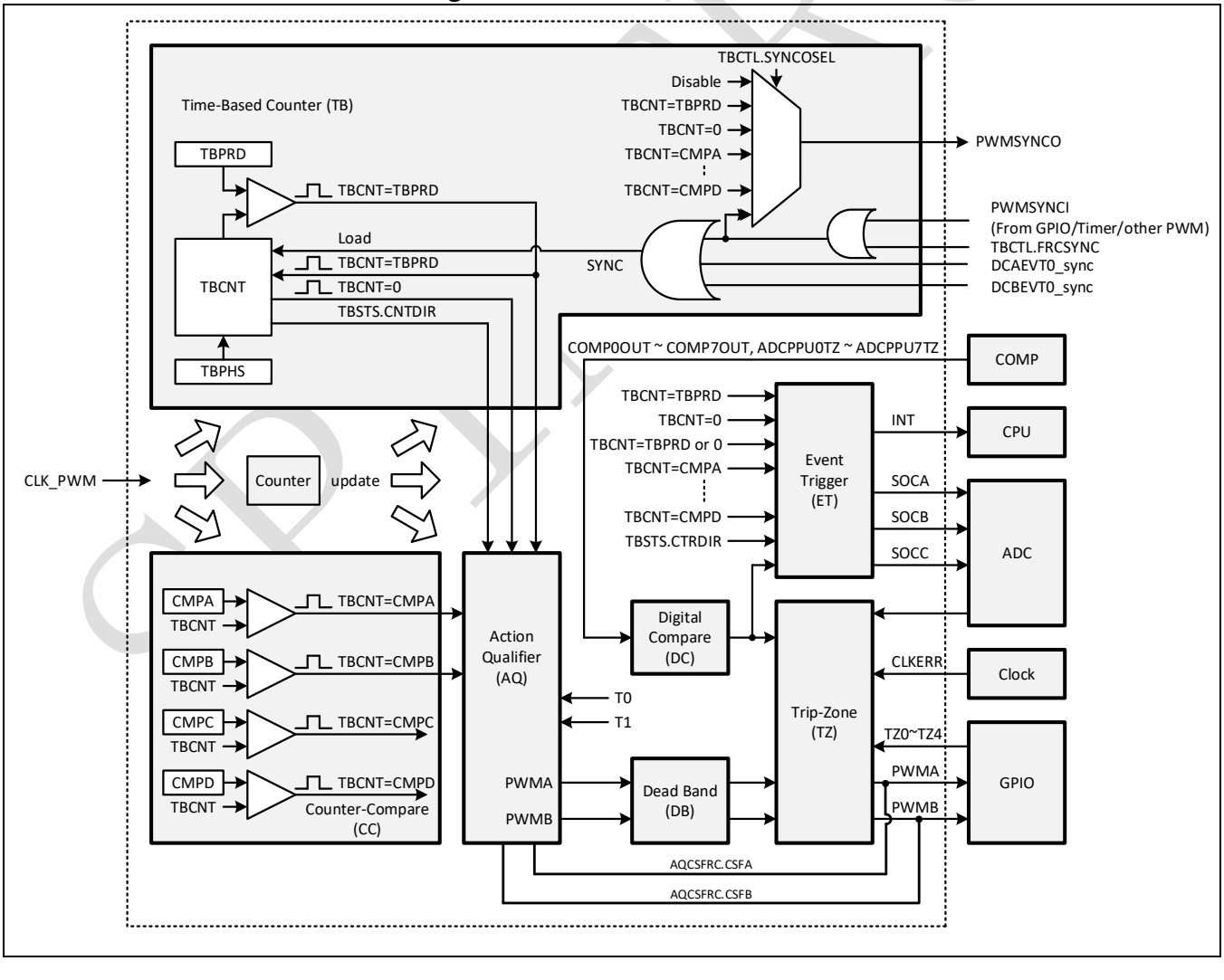

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Figure 10-2 shows more internal details of a single PWM module. The key signals of a PWM module includes:

- Synchronization IO (PWMSYNCI and PWMSYNCO)
  It is used to synchronize the phase relationship of multiple PWMs. In SPC2168, the PWMSYNCI can be from the GPIO, the timer or the PWMSYNCO of the preceding PWM.
- Trip-zone signals
  Each PWM has 5 trip-zone signals (TZ0~TZ4) configured from the GPIOs to alert the external fault conditions. Clock error event from the CLKDET module or the PLL and the halted/lockup event from the CPU can also be configured as trip-zone events for each PWM.

Note: The signal polarity from the GPIO to the trip-zone logic is programmable. By default, the trip-zone event is triggered when the GPIO is high.

- Comparator results
  The results from the 16 external comparators can generate digital compare events.
- ADC start-of-conversion (PWMxSOCA , PWMxSOCB and PWMxSOCC)
  Each PWM has three ADC start of conversion signals. The event to trigger the start of conversion signal is configured in the Event Trigger sub-module.
- PWM output (PWMxA and PWMxB)

  The PWM outputs can be configured to be multiplexed with the GPIO as in Table 4-1.

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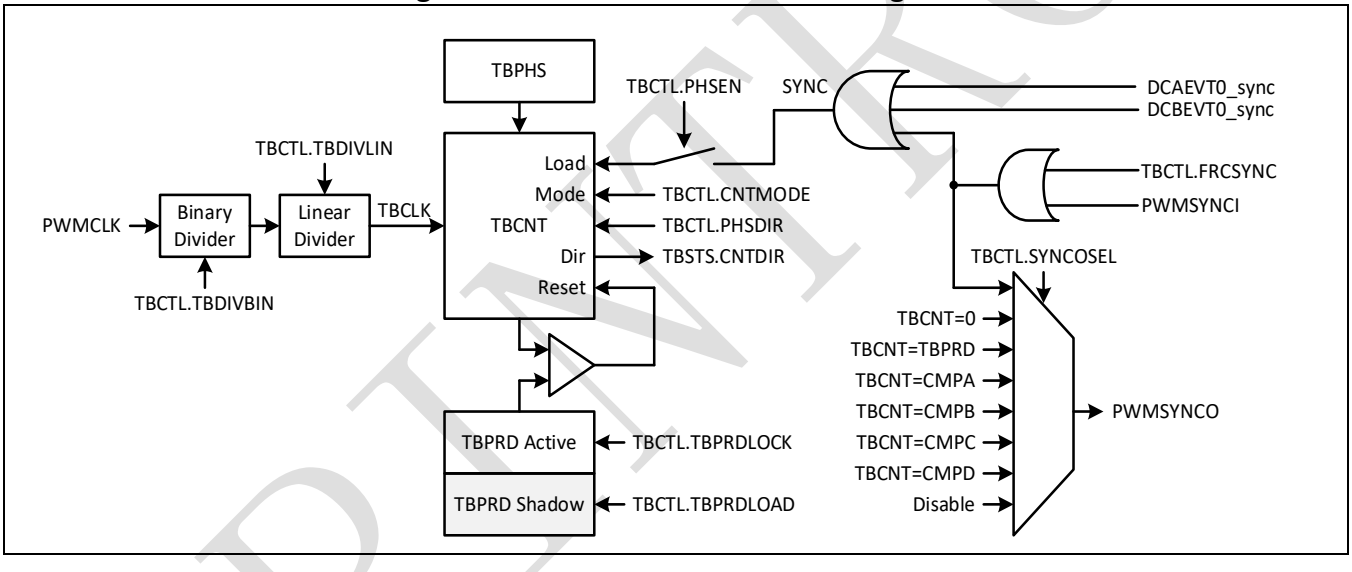
10.2 Time-Base (TB) sub-module

The time-based sub-module handles the timing for the PWM module. The key signals is given in Figure 10-3. It is programmable as below:

- Specify the time-base clock (TBCLK) dividing ratio from the input clock.
- Set the time-base counter (TBCNT) mode:
  - Count-up
  - Count-down
  - Count-up-and-down
- Specify the time-base counter (TBCNT) period.
- Determine the phase relationship with other PWM module.
- Generate the events TBCNT=TBPRD and TBCNT=0.
- Specify the synchronization trigger events input and the action taken on the counter.

Figure 10-3: Time-Base sub-module signals



The frequency of the PWM events is controlled by the counter mode (TBCTL.CNTMODE) and the time-base period (TBPRD) register. Figure 10-4 shows the period and frequency relationships for the up-count, down-count, and up-down-count time-base counter modes.

In up-count mode, the time-base counter starts from zero and increases until it reaches TBPRD. Then the TBCNT is reset to zero and starts to increase again.

In down-count mode, the time-base counter starts from TBPRD and decreases until it reaches zero. Then the TBCNT is reset to TBPRD and starts to decrease again.

In up-down-count mode, the time-base counter increases from zero until it reaches TBPRD and then decrease until it reaches zero. Read back from the CNTDIR bit in the TBSTS register is 1 when the counter increases from zero to (TBPRD-1) and 0 when the counter decreases from TBPRD to 1.

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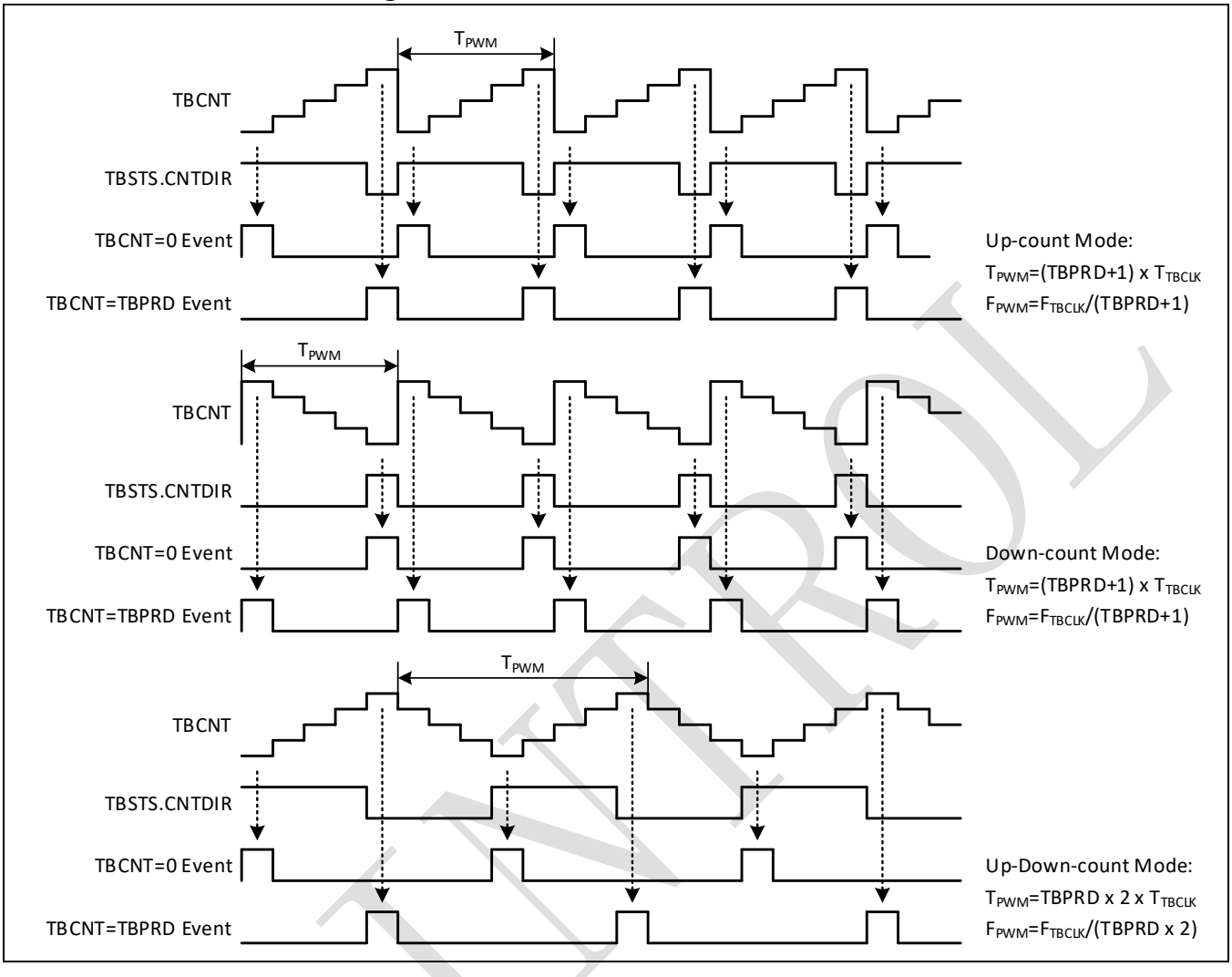
Figure 10-4: Time-base counter waveform



Shadow scheme is provided for TBPRD register in the SPC2168. In this mode, write to the TBPRD register will not immediately change the active value. Instead, the active value of TBPRD is updated from the shadow register when TBCNT=0 or TBCNT=TBPRD as defined by TBCTL.TBPRDLOAD.

While TBCTL.PHSEN=1, phase synchronization is enabled for the TBCNT. In this case, whenever there is a synchronization event, the TBCNT will load the value in time-base phase (TBPHS) register. A timing diagram is given in Figure 10-5. For up-count and down-count mode, the counter keeps the direction after synchronization. For up-down-count mode, the direction is defined by PHSDIR bit in time-base control (TBCTL) register. As shown in Figure 10-3, the synchronization event can be the external input PWMSYNCI signal, the digital compare synchronization A and B, local software forced synchronization, and the global software forced synchronization.

When TBCTL.PHSEN = 0, the PWM ignores the input synchronization event signal, but the input synchronization event signal can still be selected as the PWMSYNCO output to the subsequent PWM module for synchronization purposes.

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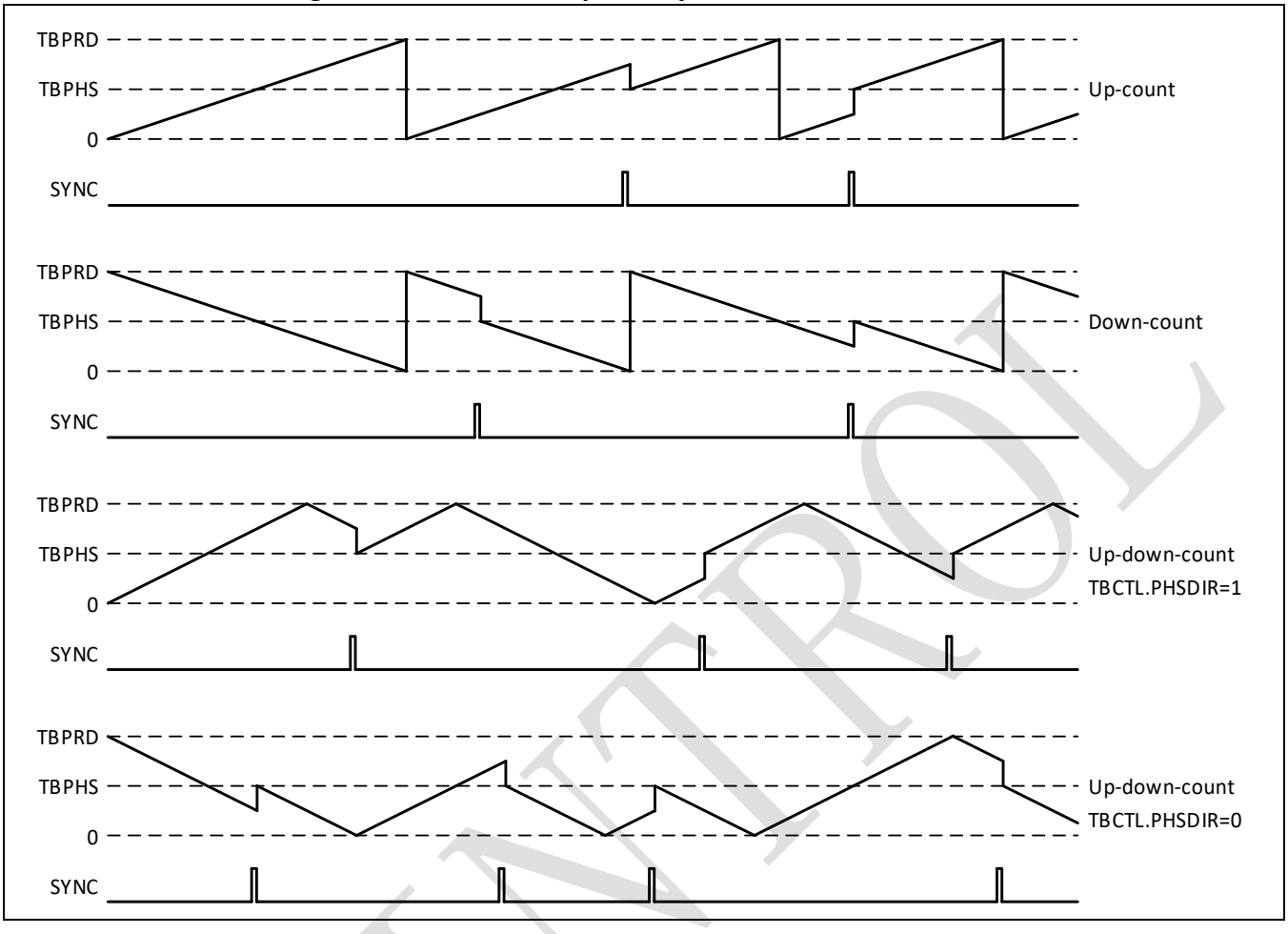
Figure 10-5: Time-base phase synchronization waveform



Note: It takes one PWM clock delay from the synchronization input to the actual synchronization action, results in one time-base cycle delay if TBCTL.TBDIVBIN=0 and TBCTL.TBDIVLIN=0. Please take this into account when setting the TBPHS register.
The register FRCSYNC in PWMCFG module provides a more flexible and convenient synchronization among the PWMs.

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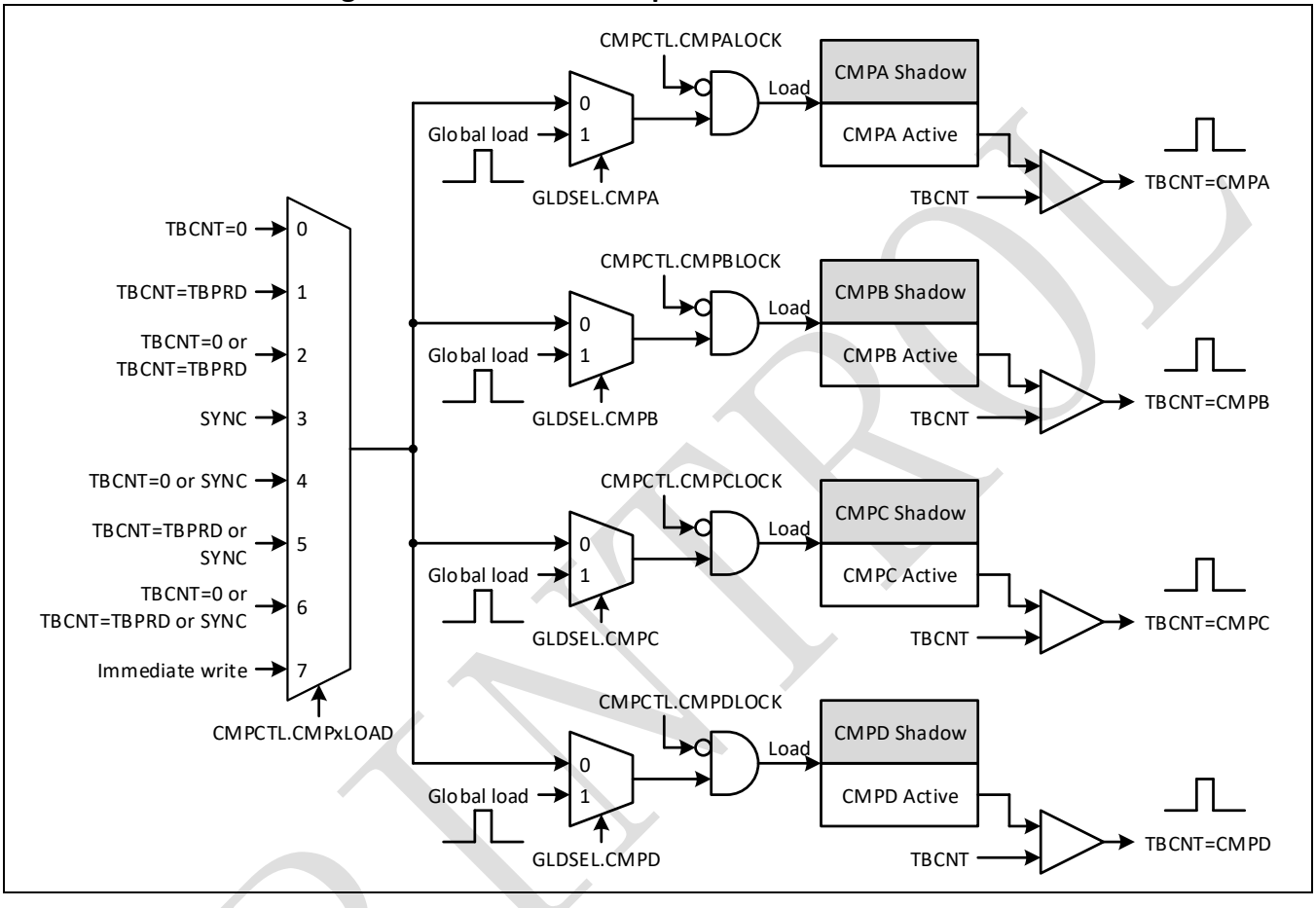
10.3 Counter Compare (CC) sub-module

The counter-compare sub-module continuously compare the TBCNT to the counter-compare A (CMPA), counter-compare B (CMPB), counter-compare C (CMPC), and counter-compare D (CMPD) registers. When TBCNT is equal to the counter-compare register, a corresponding event will be generated.

Figure 10-6: Counter-Compare sub-module structure



The basic structure of counter-compare sub-module is shown in Figure 10-6. The counter-compare registers can be configured in shadow mode that the write to the register affects only the shadow register. The active values of the counter-compare register are updated from the shadow register upon the event defined by CMPxLOAD bit in counter compare control (CMPCTL) register. Global shadow load option can be enabled via CMPx bit in GLDSEL register as described in detail in Table 10-14 and Table 10-15. A sample waveform is shown in Figure 10-7.

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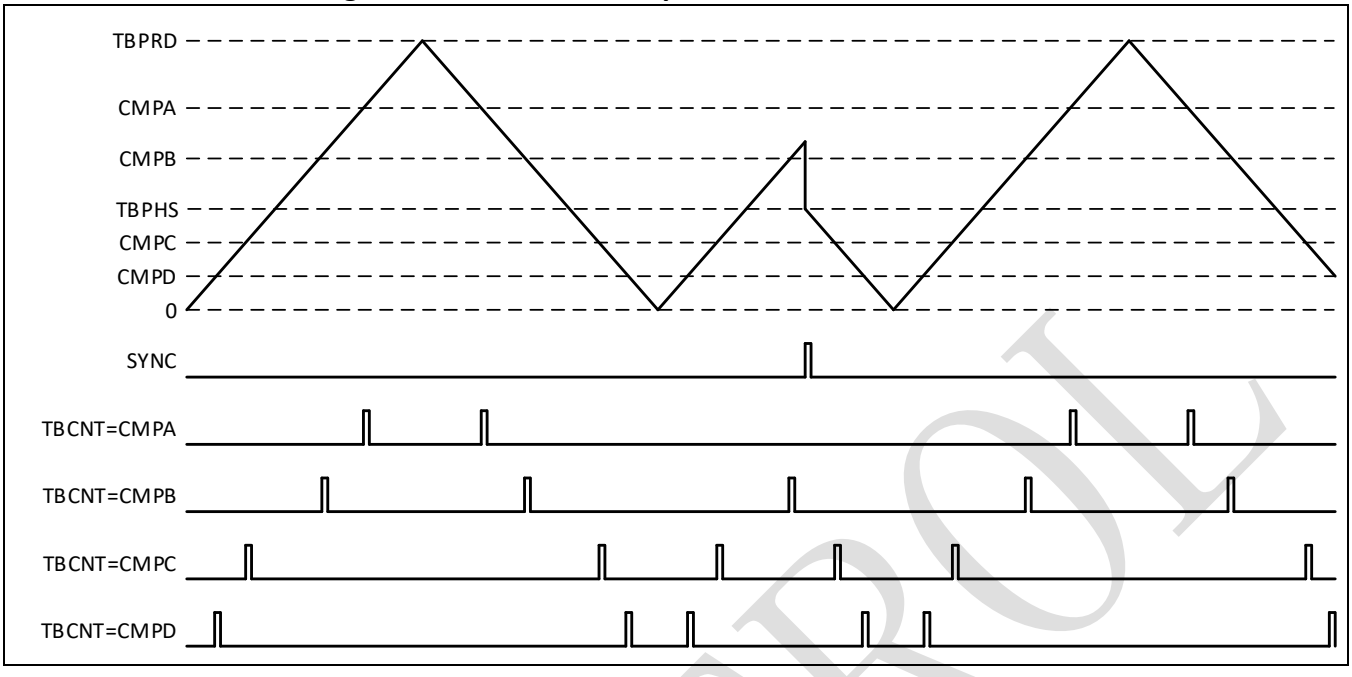
Figure 10-7: Counter-Compare sub-module waveform



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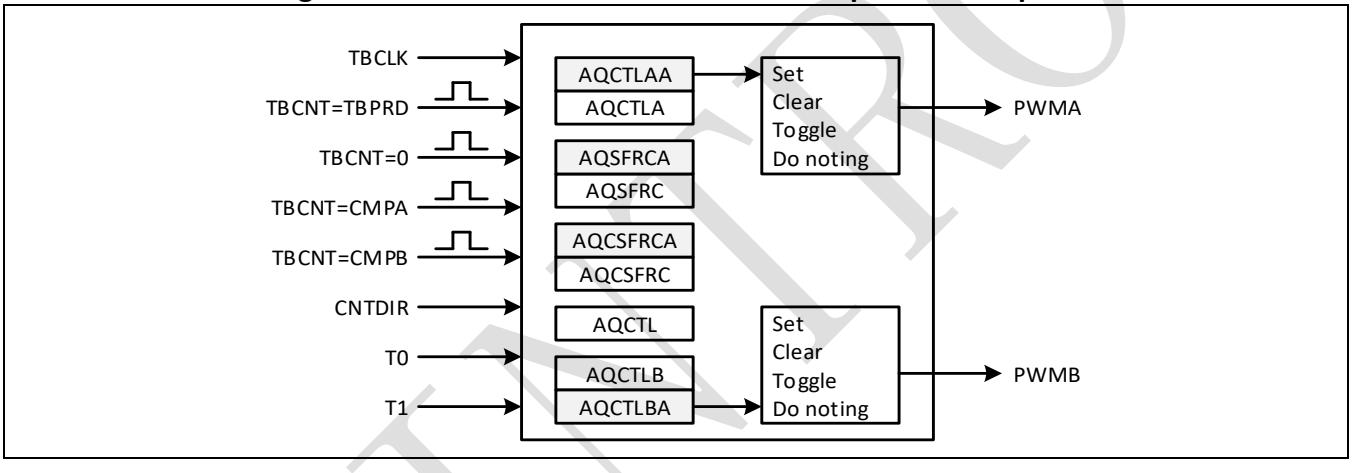
10.4 Action-Qualifier (AQ) sub-module

The action-qualifier sub-module determines which events are converted into various action types and produces the required switched waveforms at PWMA and PWMB outputs.

As shown in Figure 10-8, the events includes:

- TBCNT=TBPRD
- TBCNT=0
- TBCNT=CMPA
- TBCNT=CMPB
- T0/T1 events, which are based on comparator, trip-zone and sync input events
- Software forced event

Figure 10-8: Action-Qualifier sub-module inputs and outputs



Note: The AQCSFRC software forces the A/B output paths of the TZ sub-module.

The action-qualifier handles these events as well as their priority if they occur concurrently. Based on the events, it takes one of following actions as defined by AQCTLA and AQCTLB registers.

- Set output to a high level
- Clear output to a low level
- Toggle the output
- Do nothing

Shadow mode or the immediate write mode can be selected via AQCTL.AQCTLALOAD, AQCTL.AQCTLBLOAD and AQSFRC.CSFLOAD. Global load is also supported by setting GLDSEL.AQCTLA, GLDSEL.AQCTLB and GLDSEL.AQCSFRC. It is similar to the shadow for CMPx registers as shown in Figure 10-6.

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Table 10-1 through Table 10-3 list the priority of action-qualifier in different count modes.

Table 10-1: Action-Qualifier event priority for Up-Count mode

Priority Level	Event
1(Highest)	Software forced event
2	TBCNT=TBPRD (PRD)
3	T0 on up-count (T0U)
4	T1 on up-count (T1U)
5	TBCNT=CMPB on up-count (CBU)
6	TBCNT=CMPA on up-count (CAU)
7 (Lowest)	TBCNT=0 (ZRO)

Table 10-2: Action-Qualifier Event Priority for Down-Count Mode

Priority Level	Event
1(Highest)	Software forced event
2	TBCNT=0 (ZRO)
3	T0 on down-count (T0D)
4	T1 on down-count (T1D)
5	TBCNT=CMPB on down-count (CBD)
6	TBCNT=CMPA on down-count (CAD)
7 (Lowest)	TBCNT=TBPRD (PRD)

Table 10-3: Action-Qualifier Event Priority for Up-Down-Count Mode

Priority Level	Event	
	When increase from 0 to TBPRD-1	When decrease from TBPRD to 1
1(Highest)	Software forced event	Software forced event
2	T0 on up-count (T0U)	T0 on down-count (T0D)
3	T1 on up-count (T1U)	T1 on down-count (T1D)
4	TBCNT=CMPB on up-count (CBU)	TBCNT=CMPB on down-count (CBD)
5	TBCNT=CMPA on up-count (CAU)	TBCNT=CMPA on down-count (CAD)
6 (Lowest)	TBCNT=0 (ZRO)	TBCNT=TBPRD (PRD)

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Figure 10-9 and Figure 10-10 demonstrate timing diagrams for the symmetric and asymmetric scenarios of the action qualifier.

Figure 10-9: Up-Down-Count, dual edge symmetric waveform of Action-Qualifier

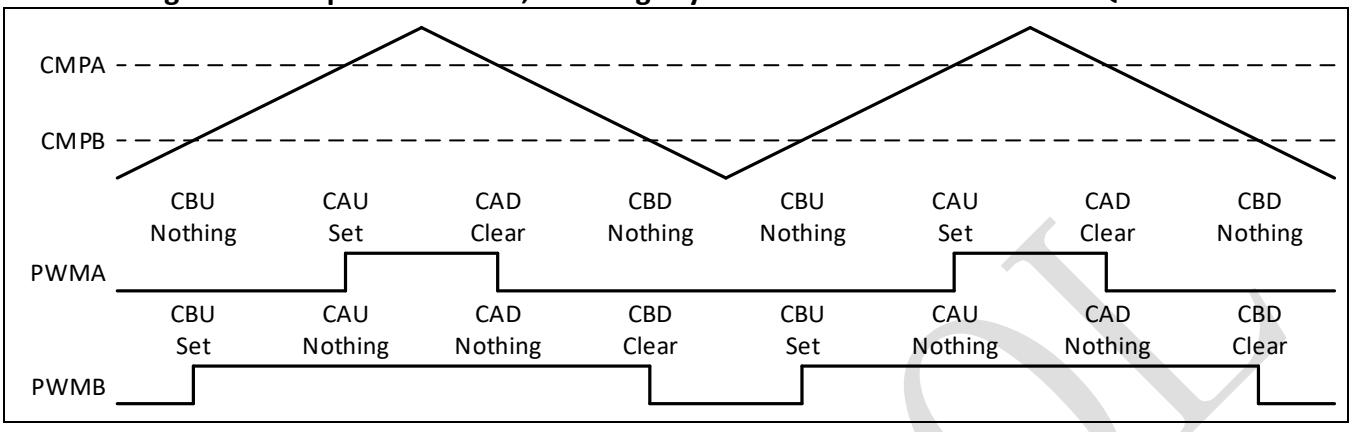
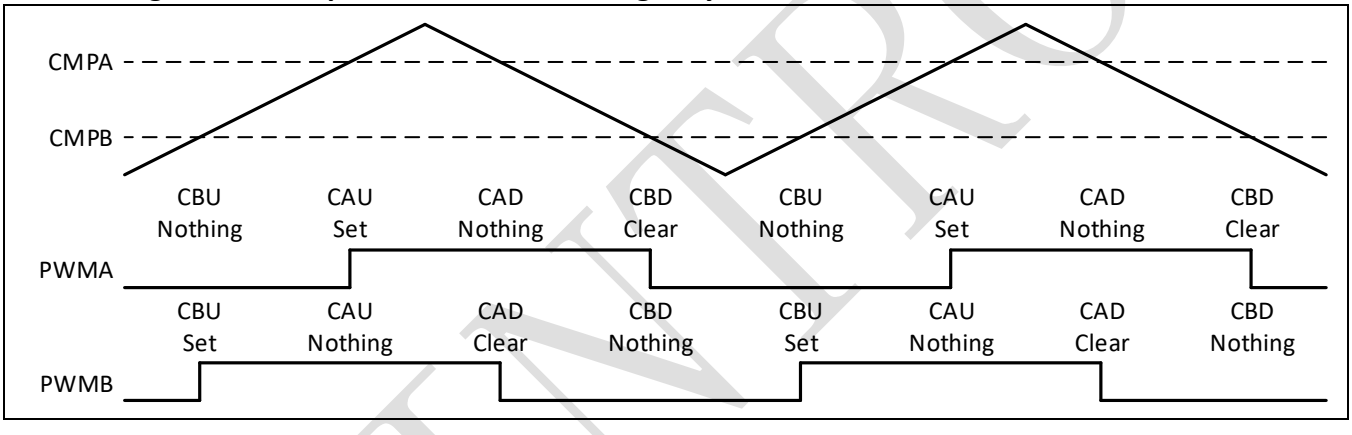


Figure 10-10: Up-Down-Count, dual edge asymmetric waveform of Action-Qualifier



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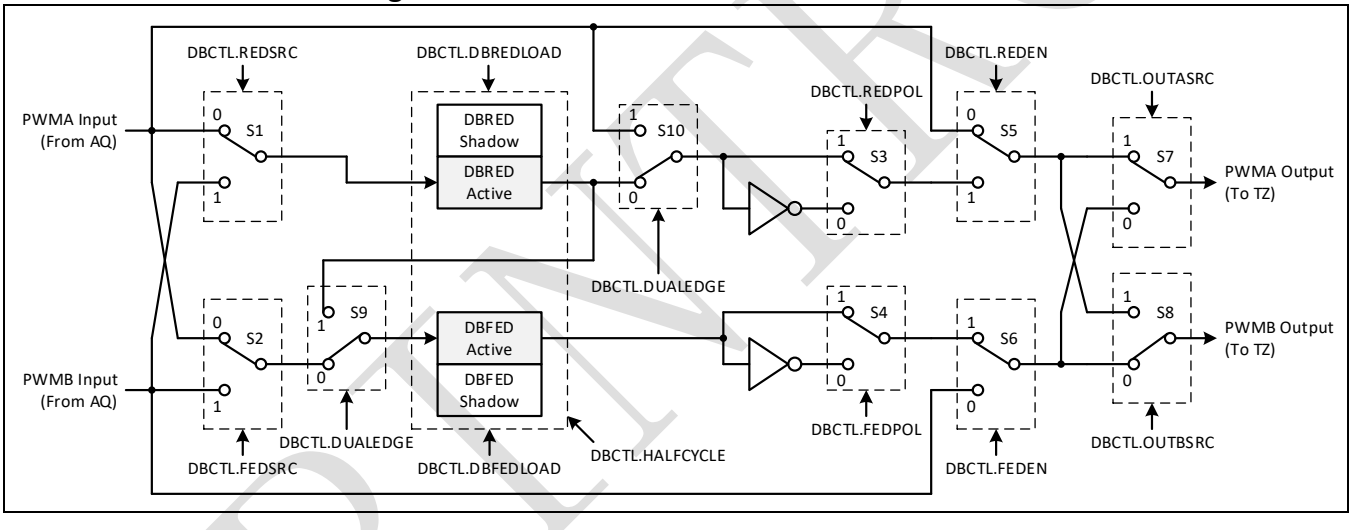
10.5 Dead-Band (DB) sub-module

The dead-band sub-module deals with the signals from the action qualifier to further shaping the waveform with independent and programmable rising-edge and falling-edge delay as well as polarity control.

The key functions of the module includes:

- Generate signal pairs output (PWMA and PWMB) with dead-band relationship from a single PWMA input
- Add programmable delay to rising edge
- Add programmable delay to falling edge
- Support half clock cycle delay
- Adjust the polarity of the output signal
- Bypass the dead-band signal shaping and directly feed through the signals from the action qualifier

Figure 10-11: Dead-Band sub-module structure



Basic structure of the dead-band sub-module is given in Figure 10-11. The REDSRC and FEDSRC bits in dead-band control (DBCTL) register determines the input signal source of the rising edge delay and falling edge delay. All combinations to control the switches from S3 to S10 are supported. Taking DBCTL.REDSRC=0 and DBCTL.FEDSRC=0 for example, when PWMA is configured as the input for both rising-edge and falling-edge delay, the typical operating modes are listed in Table 10-4.

As a special case, dual-edge delay can be achieved by setting the DUALEDGE bit in DBCTL register, when both rising-edge and falling-edge are applied to the same path. This is useful to generate a waveform pair with the same period and duty-cycle but specified phase shift between each other.

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Table 10-4: Typical Dead-Band operating modes

Mode	Mode Description	REDPOL S3	FEDPOL S4	REDEN S5	FEDEN S6
1	Both PWMA and PWMB pass through	X	X	0	0
2	Active high complementary	1	0	1	1
3	Active low complementary	0	1	1	1
4	Active high	0	0	1	1
5	Active low	1	1	1	1
6	PWMA output = PWMA input with no delay PWMB output = PWMA input with falling-edge delay	0 or 1	0 or 1	0	1
7	PWMA output = PWMA input with rising-edge delay PWMB output = PWMA input with no delay	0 or 1	0 or 1	1	0

Figure 10-12 illustrates the waveform of typical dead-band sub-module.

Figure 10-12: Typical Dead-Band waveform

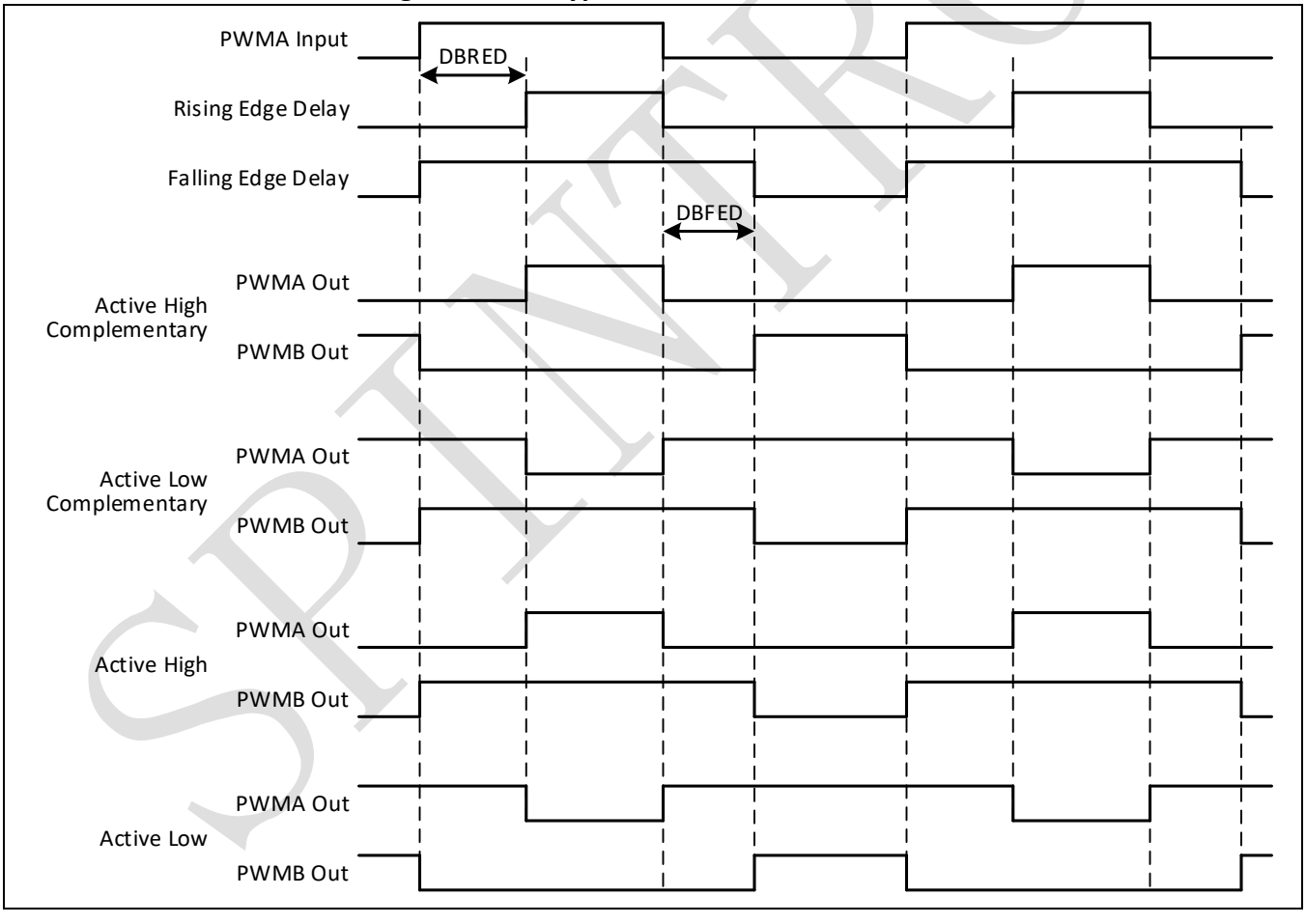

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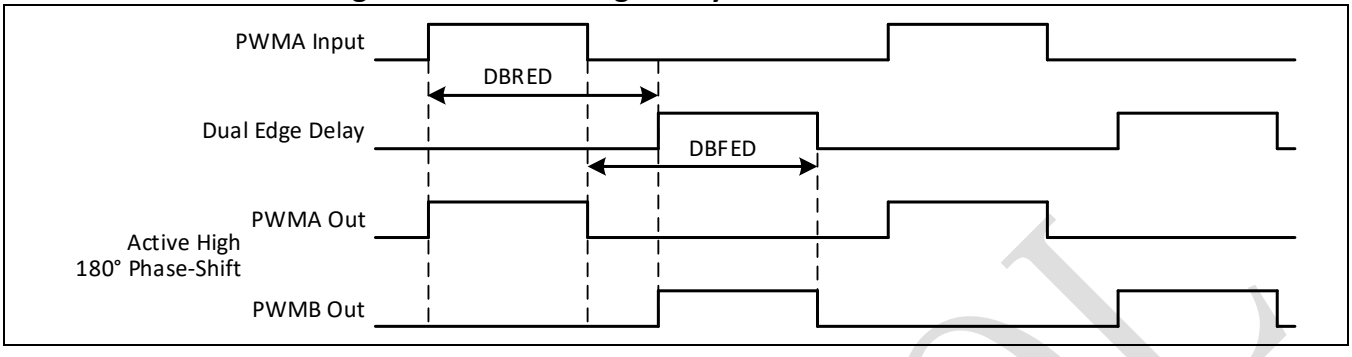
Figure 10-13 illustrates the case to generate waveform with 180° phase shift by enable dual-edge delay and setting both DBRED and DBFED to half the waveform period.

Figure 10-13: Dual-edge delay Dead-Band waveform



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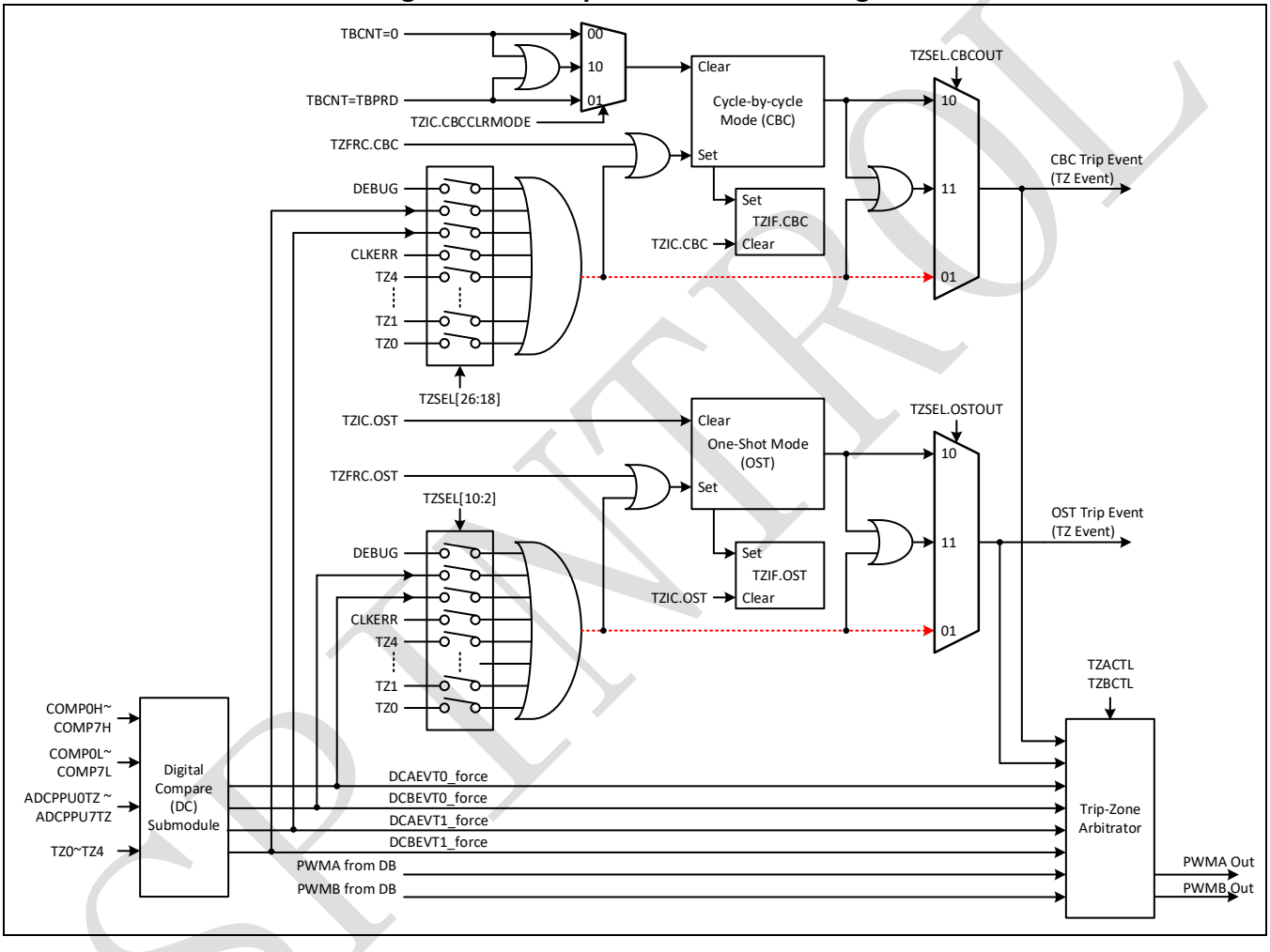
10.6 Trip-Zone (TZ) sub-module

The trip-zone sub-module determines the PWM outputs when external fault or trip condition occurs. As shown in Figure 10-14, the input can be from the TZ signal, the clock error event from the PLL unlock detection or the CLKDET module, the debug signal from the core, or the digital compare (DC) output. The five TZ signals (TZ0~TZ4) are sourced from the GPIO multiplexer with programmable signal polarity according to the TZ#SRCCTL registers in PWMCFG module. Software-forced tripping is also supported and interrupt can be generated on any trip-zone input.

Figure 10-14: Trip-Zone sub-module logic



Upon a fault condition, the PWMA and PMWB outputs can be forced to one of the following:

- High
- Low
- High-impedance
- No action

The event actions on PWMA output is controlled by register TZACTL, and the priority of these event actions is TZU > TZD > DCAEVT0U > DCAEVT0D > DCAEVT1U > DCAEVT1D. It means that when both high priority event and low priority event happen, the output is determined by the configuration of the high

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priority event. For example, when both TZU and DCAEVT1U events happen, TZU register field determines the PWM output while DCAEVT1U field is ignored.

Both one-shot trip (OST) and cycle-by-cycle (CBC) trip are supported. The one-shot trip is typically used for major over-current or short circuits condition while the cycle-by-cycle trip is usually used for current limiting operation.

When a one-shot trip event occurs, the action specified in the TZACTL and TZBCTL registers is immediately taken on the PWMA and PWMB outputs. Meanwhile, the one-shot trip event flag (TZIF.OST) is set and a PWM_TZINT interrupt is generated if it is enabled in trip-zone enable interrupt (TZIE) register. The TZIF.OST flag must be manually cleared by writing 1 to the TZIC.OST bit.

When a cycle-by-cycle trip event occurs, the action specified in the TZACTL and TZBCTL registers is immediately taken on the PWMA and PWMB outputs. Meanwhile, the cycle-by-cycle trip event flag (TZIF.CBC) is set and a PWM_TZINT interrupt is generated if it is enabled in the TZIE register. The specified condition is automatically cleared if the trip event is no longer present when the TBCNT reaches zero or TBPRD as specified by TZIC.CBCCLRPUL. However, the TZIF.CBC flag bit remains set until it is manually cleared by writing 1 to the TZIC.CBC bit. If the cycle-by-cycle trip event is still present when the TZIF.CBC flag is cleared, it will be set again immediately.

Note: The asynchronous logic path shown as dashed line in Figure 10-14 is used to observe the original trip-zone event signal when TZSEL.OSTOUT or TZSEL.CBCOUT is set to 1. In real application, the latched path should be enabled to implement the one-shot or cycle-by-cycle trip function as described above. i.e. TZSEL.OSTOUT and TZSEL.CBCOUT should be 2 or 3.

The digital compare DCAEVT0/1 or DCBEVT0/1 event is generated based on the DCAH/DCAL and DCBH/DCBL bits of trip-zone digital compare selection (TZDCSEL) register. When a digital compare event occurs, the action specified in the TZACTL and TZBCTL registers is immediately taken on the PWMA and PWMB outputs. Meanwhile, the DC trip event flag (TZIF.DCAEVT0/1 and TZIF.DCBEVT0/1) is set and a PWM_TZINT interrupt is generated if it is enabled in the TZIE register. The specified condition is automatically cleared when the DC trip event is no longer present. However, the flag bits in the TZIF register remains set until it is manually cleared by writing 1 to the corresponding bits in the TZIC register. If the DC trip event is still present when the TZIF bit is cleared, it will be set again immediately.
Figure 10-15 illustrates the trip-zone interrupt logic.

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Figure 10-15: Trip-Zone interrupt generation

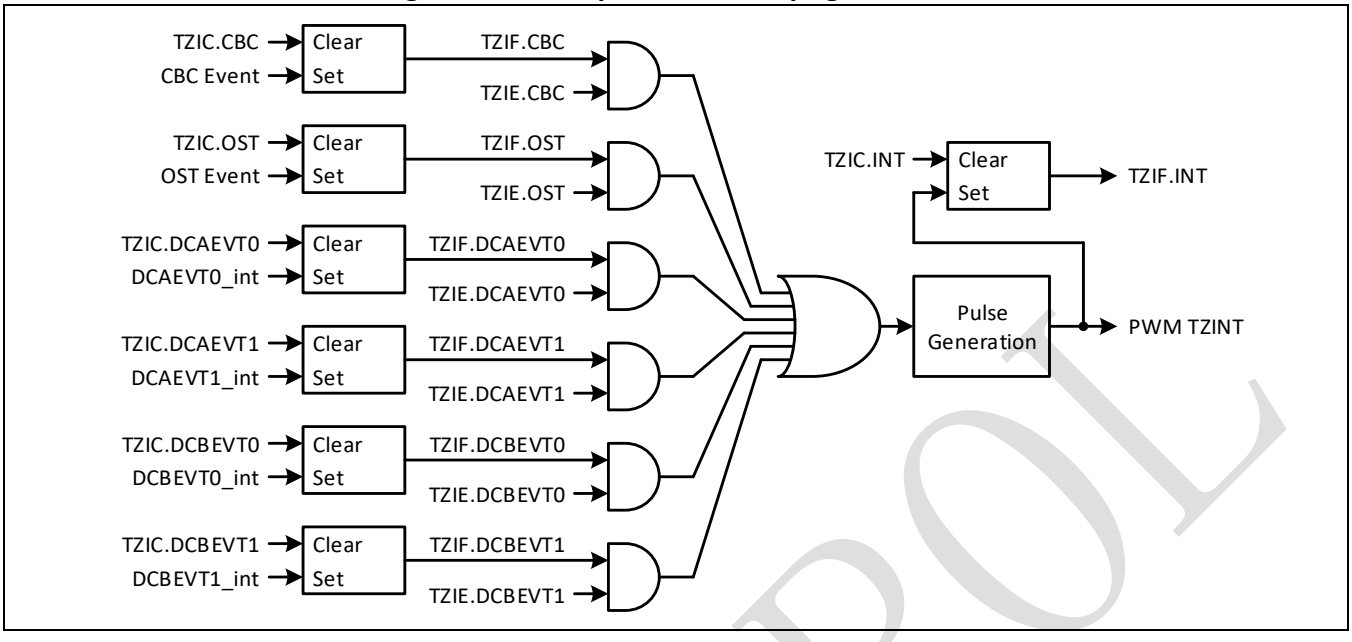

Table 10-5 lists the priority of events that effect the final PWM outputs.

Table 10-5: Priority of events that effect the final PWM outputs

Priority Level	Event
1(Highest)	Trip event
2	Continuous software force via AQCSFRC register
3	Dead-Band control logic
4	One-time software force via AQSFRC register
5 (Lowest)	Action-Qualifier control logic

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10.7 Digital Compare (DC) sub-module

The digital compare sub-module takes the analog comparator (COMP) module outputs, the ADC post-processing unit (ADCPPU) module trip-zone outputs, and TZ0, TZ1, TZ2, TZ3 and TZ4 inputs to generate digital compare A high/low (DCAH, DCAL) and digital compare B high/low (DCBH, DCBL) signals. As shown in Figure 10-16,these signals generates DCAEVT0/1 and DCBEVT0/1 events, which can be either filtered or directly fed to the event processing logic, so as to generate signals for time-base, trip-zone and event-trigger sub-modules.

The raw DCAEVT0/1 and DCBEVT0/1 events can be filtered to remove noise by inserting a blank window to gate the event for a certain time as shown in Figure 10-17. Upon the TBCNT=TBPRD or TBCNT=0 pulse, the offset counter loads the value from the DCFOFFSET register and starts to count down. When the counter expires, the blank window starts and the duration is certain TBCLK clocks determined by DCFWINDOW register. During the blank window, all events are ignored. Before the window starts and after the window ends, events can generate SOC, SYNC, interrupt and force signals as before. To take into account the cross-talk from/to other blocks in real application, the generated blank windows from PWM modules can be enabled to filter local raw DC events. The polarity of the blank window can be inverted by set BLANKINV bit of DCFCTL register. As shown in the timing diagram in Figure 10-18, the new blank window will immediately start even if the old one does not expire.

Figure 10-16: Digital Compare sub-module structure

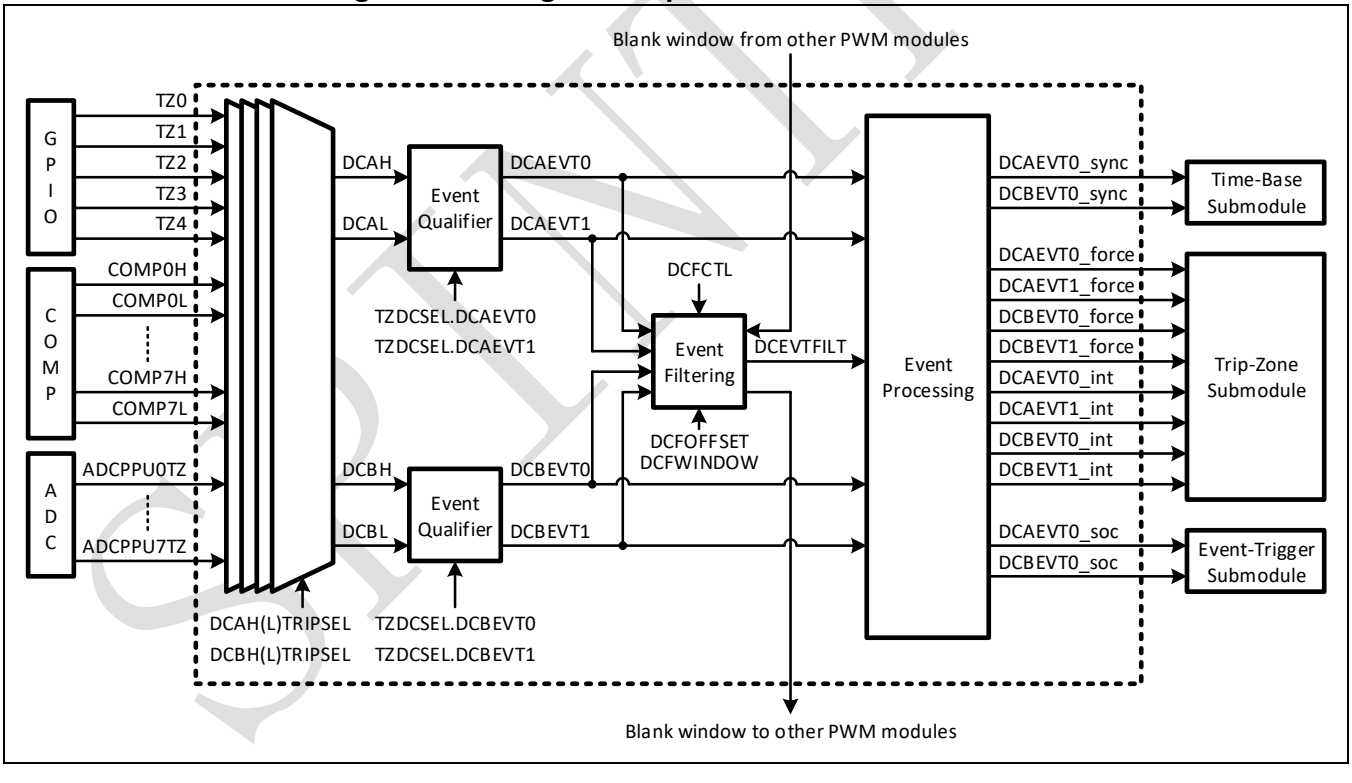

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Figure 10-17: Event filtering logic

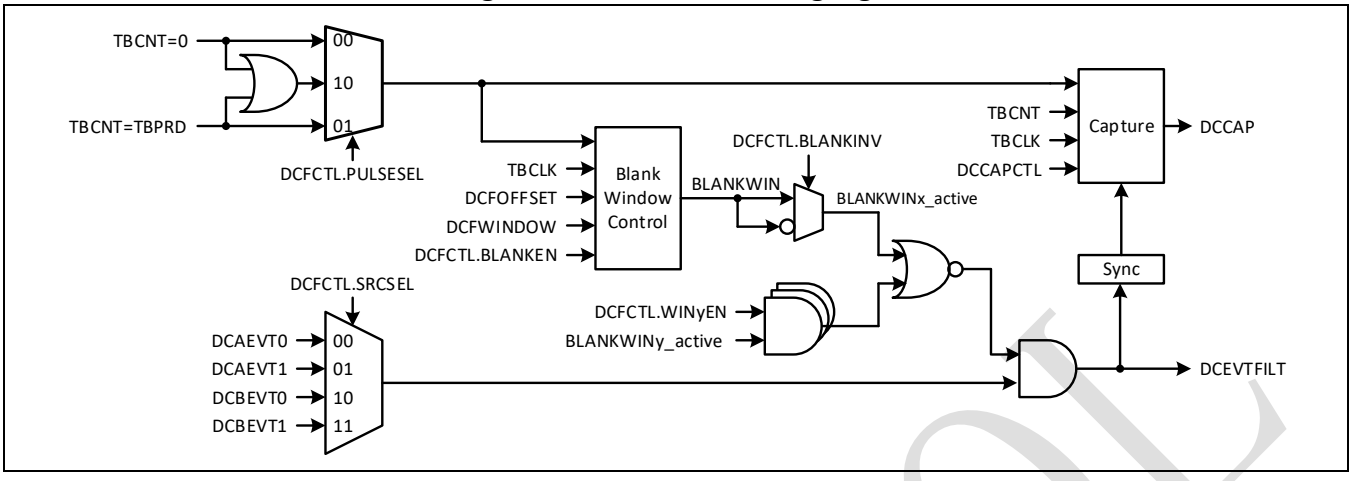
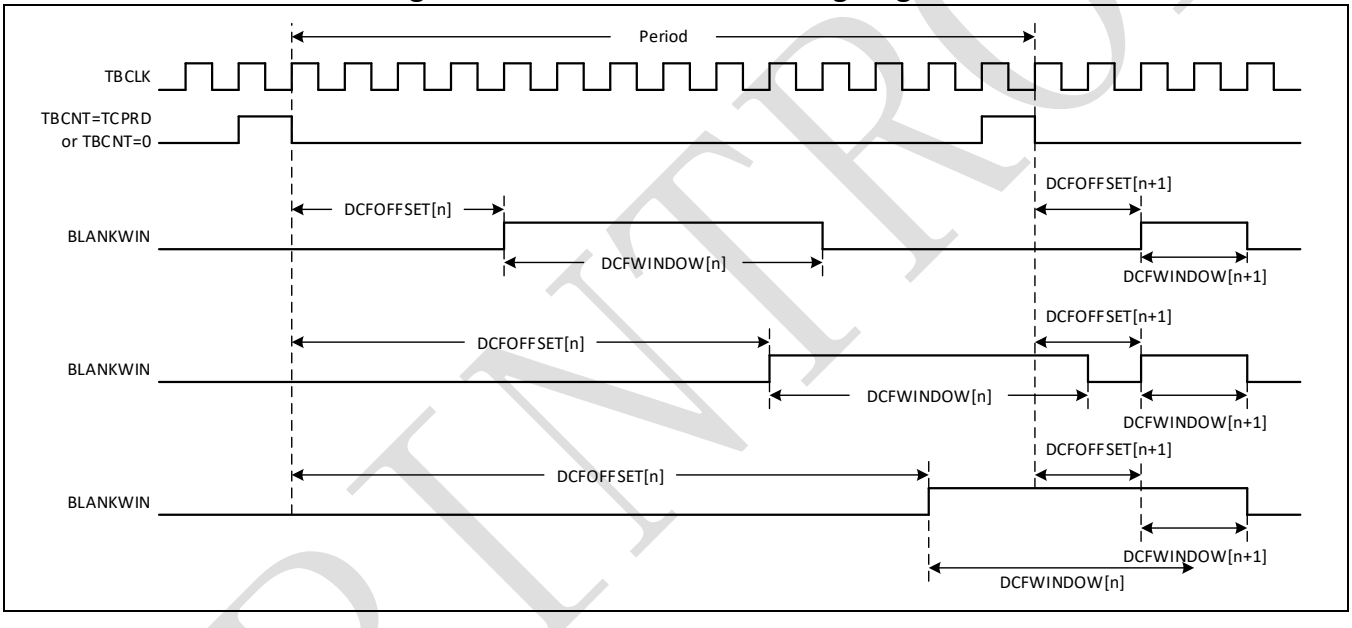


Figure 10-18: Blank window timing diagram



As shown in Figure 10-19, the raw DCAEVT0, DCAEVT1, DCBEVT0, DCBEVT1 and the filtered DCEVTFILT pass through the event processing block and generate the final DCAEVT0, DCAEVT1, DCBEVT0 and DCBEVT1 events according to EVT0SRCSEL and EVT1SRCSEL fields in DCACTL and DCBCTL registers. Based on these events, further signals can be generated as below:

- Force signals for trip-zone sub-module
  DCAEVT0_force, DCAEVT1_force, DCBEVT0_force, DCBEVT1_force
- Synchronous signal for time-base sub-module
  DCAEVT0_sync, DCBEVT0_sync
- ADC start of conversion
  DCAEVT0_soc, DCBEVT0_soc
- Interrupt
  DCAEVT0_int, DCAEVT1_int, DCBEVT0_int, DCBEVT1_int

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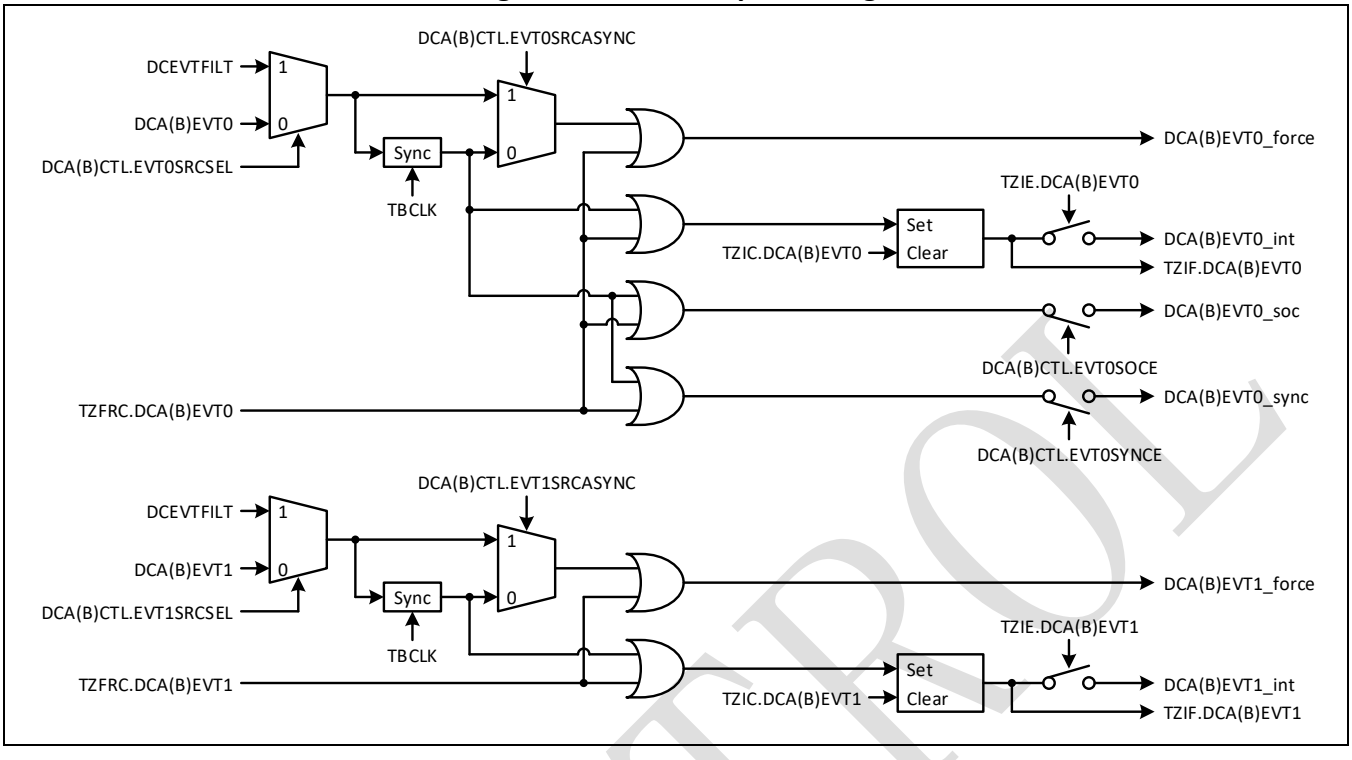
Figure 10-19: Event processing



Below is an example in the scenario that COMP0~COMP2 are used for shut-current monitoring and generate filtered DC trip-zone events to control both PWMxA and PWMxB outputs.

- DCAH is set as the logic OR of COMP0H, COMP0L, COMP1H, COMP1L, COMP2H, and COMP2L via DCAHTRIPSEL register.
- Use DCAH=high to generate the raw DCAEVT0 signal via setting TZDCSEL.DCAEVT0=4.
- Use the raw DCAEVT0 as the DC filter input via setting DCFCTL.SRCSEL=0.
- Use the filtered signal DCEVTFILT as the final DCAEVT0 event via setting DCACTL.EVT0SRCSEL=1.
- Use the filtered signal DCEVTFILT as the final DCBEVT0 event via setting DCBCTL.EVT0SRCSEL=1.
- Configure the PWMxA output action upon final DCAEVT0 trip-zone event via DCAEVT0U and DCAEVT0D fields in TZACTL register.
- Configure the PWMxB output action upon final DCBEVT0 trip-zone event via DCBEVT0U and DCBEVT0D fields in TZBCTL register.

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10.8 Event-Trigger (ET) sub-module

The event-trigger sub-module manages the events generated by the time-base sub-module, the counter-compare sub-module, and the digital-compare sub-module to generate an interrupt to the CPU and/or a start-of-conversion (SOC) pulse to the ADC when a selected event occurs.

Figure 10-20: Event-Trigger sub-module structure

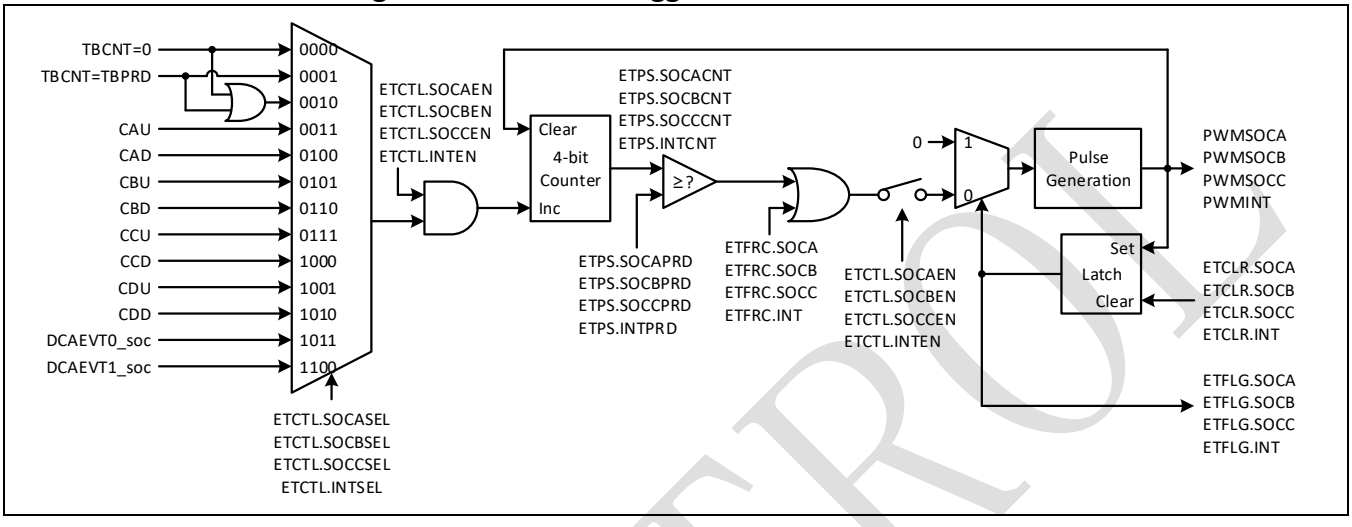

Figure 10-20 illustrates the basic structure of the event-trigger sub-module. Software forced SOCA, SOCB, SOCC and INT pulses are supported in the SPC2168. By using a 4-bit counter, the pulse can be generated in following scenario:

- Never generate
- Generate a pulse on every event
- Generate a pulse on every second event
- ……
- Generate a pulse up to every fifteenth event

10.9 Global reload

The content transfer from the shadow register to the active register can be done upon the global load strobe as shown in Figure 10-21. This feature is enabled by setting the GLDEN bit of GLDCTL0 register to 1. And the bits in GLDSEL register decide whether the corresponding active register is updated upon the global load strobe or the local load strobe.
When GLDCTL0.OSTMODE=0, the pre-scaler is applied so that the global load strobe is generated every GLDCTL0.GLDPRD occurrences of the global reload events.

When GLDCTL0.OSTMODE=1, one-shot reload mode is enabled so that only the first global reload event will generate the global load strobe after GLDCTL1.OSTLD is setting to 1. Once the global load strobe is generated, the GLDCTL1.OSTLD is cleared to 0 until it is manually set to 1 again. Global reload events during GLDCTL1.OSTLD=0 do not generate any global load strobe.

Software forced global reload can be enabled via writing 1 to GLDCTL1.FRCLD.

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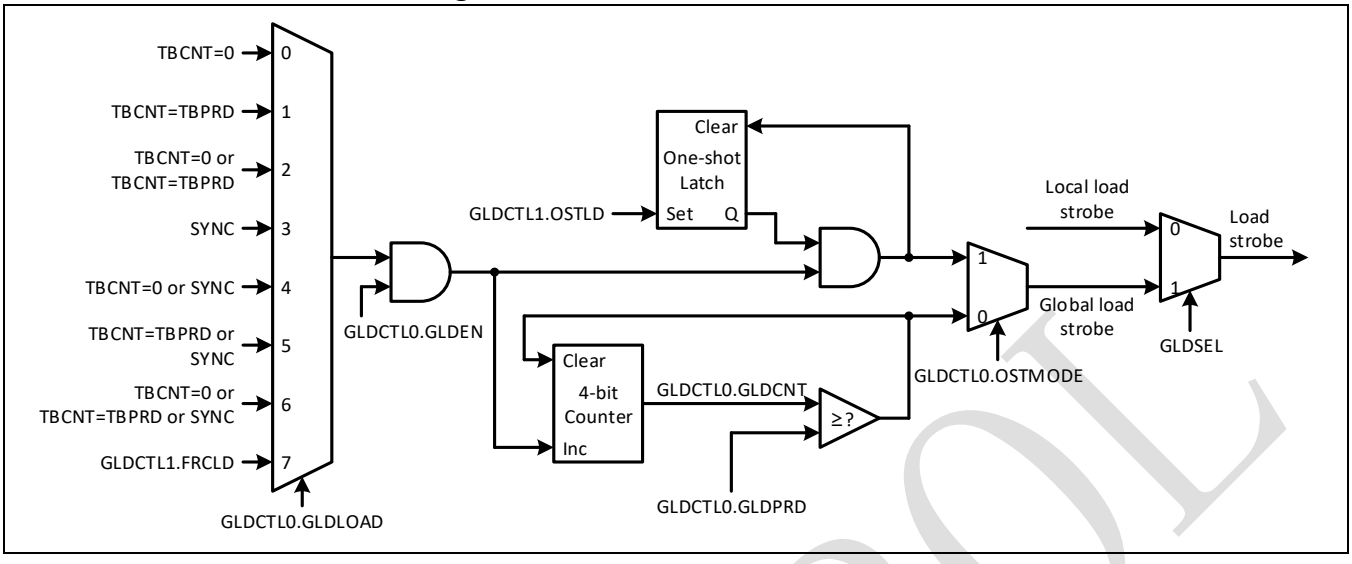
Figure 10-21: Global reload structure



10.10 Simultaneous write

In some applications, there is a need of simultaneous writes to the registers of same name in different PWMs. SPC2168 provides a PWM link feature by PWMLINK register, so that write to the register of another PWM module can also update the value of the same register in current PWM module. The registers supporting this feature are TBPRD, CMPA, CMPB, CMPC, CMPD, DBRED, DBFED and GLDCTL1.

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10.11 Registers

10.11.1 PWM register map

Table 10-6: PWM Module Base Address

Peripheral Module	Base Address
PWM0	0x4000 9000
PWM1	0x4000 9100
PWM2	0x4000 9200
PWM3	0x4000 9300
PWM4	0x4000 9400
PWM5	0x4000 9500
PWM6	0x4000 9600
PWM7	0x4000 9700

Table 10-7: PWM Register Map

Register	Offset	Description	Reset Value
SHADOWSTS	0x00	Shadow Status Register	0x00000000
GLDCTL0*	0x04	Global Shadow to Active Load Control Register 0	0x00000000
GLDCTL1	0x08	Global Shadow to Active Load Control Register 1	0x00000000
GLDSEL*	0x0C	Global Shadow to Active Load Select Register	0x00000000
PWMLINK*	0x10	PWM Link Control Register	0xFFFFFFFF
TBCTL*	0x14	Time-Base Control Register	0x00000006
TBPRD	0x18	Time-Base Period Register	0x00000000
TBPRDA	0x1C	Time-Base Period Active Register	0x00000000
TBPHS	0x20	Time-Base Phase Register	0x00000000
TBCNT	0x24	Time-Base Counter Register	0x00000000
TBSTS	0x28	Time-Base Status Register	0x00000100
TBSTSCLR	0x2C	Time-Base Status Clear Register	0x00000000
CMPCTL*	0x30	Counter-Compare Control Register	0x00000000
CMPA	0x34	Counter-Compare A Threshold Register	0x00000000
CMPAA	0x38	Counter-Compare A Threshold Active Register	0x00000000
CMPB	0x3C	Counter-Compare B Threshold Register	0x00000000
CMPBA	0x40	Counter-Compare B Threshold Active Register	0x00000000
CMPC	0x44	Counter-Compare C Threshold Register	0x00000000
CMPCA	0x48	Counter-Compare C Threshold Active Register	0x00000000
CMPD	0x4C	Counter-Compare D Threshold Register	0x00000000
CMPDA	0x50	Counter-Compare D Threshold Active Register	0x00000000
AQCTL*	0x54	Action-Qualifier Control Register	0x00000000
AQCTLA	0x58	Action-Qualifier Output A Control Register	0x00000000
AQCTLAA	0x5C	Action-Qualifier Output A Control Active Register	0x00000000
AQCTLB	0x60	Action-Qualifier Output B Control Register	0x00000000
AQCTLBA	0x64	Action-Qualifier Output B Control Active Register	0x00000000
AQSFRC	0x68	Action-Qualifier Software Force Register	0x00000000
AQCSFRC	0x6C	Action-Qualifier Continuous Software Force Register	0x00000000
AQCSFRCA	0x70	Action-Qualifier Continuous Software Force Active Register	0x00000000

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Register	Offset	Description	Reset Value
DBCTL*	0x74	Dead-Band Generator Control Register	0x00000070
DBCTLA	0x78	Dead-Band Generator Control Active Register	0x00000070
DBRED	0x7C	Dead-Band Generator Rising Edge Delay Register	0x00000000
DBREDA	0x80	Dead-Band Generator Rising Edge Delay Active Register	0x00000000
DBFED	0x84	Dead-Band Generator Falling Edge Delay Register	0x00000000
DBFEDA	0x88	Dead-Band Generator Falling Edge Delay Active Register	0x00000000
TZSEL*	0x8C	Trip-Zone Event Select Register	0x00030003
TZSTS	0x90	Trip-Zone Status Register	0x00000000
TZSTSCLR	0x94	Trip-Zone Status Clear Register	0x00000000
TZDCSEL*	0x98	Trip-Zone Digital Compare Event Select Register	0x00000000
TZACTL	0x9C	Trip-Zone Output A Control Register	0x00000000
TZBCTL	0xA0	Trip-Zone Output B Control Register	0x00000000
TZIF	0xA4	Trip-Zone Interrupt Flag Register	0x00000000
TZIC	0xA8	Trip-Zone Interrupt Clear Register	0x00000000
TZIE*	0xAC	Trip-Zone Interrupt Enable Register	0x00000000
TZFRC	0xB0	Trip-Zone Force Register	0x00000000
DCALTRIPSEL*	0xB4	Digital Compare AL Trip Select Register	0x00000000
DCAHTRIPSEL*	0xB8	Digital Compare AH Trip Select Register	0x00000000
DCBLTRIPSEL*	0xBC	Digital Compare BL Trip Select Register	0x00000000
DCBHTRIPSEL*	0xC0	Digital Compare BH Trip Select Register	0x00000000
DCACTL*	0xC4	Digital Compare A Control Register	0x00000000
DCBCTL*	0xC8	Digital Compare B Control Register	0x00000000
DCFCTL*	0xCC	Digital Compare Filter Register	0x00000010
DCFOFFSET	0xD0	Digital Compare Filter Offset Register	0x00000000
DCFOFFSETCNT	0xD4	Digital Compare Filter Offset Counter Register	0x00000000
DCFWINDOW	0xD8	Digital Compare Filter Window Register	0x00000000
DCFWINDOWCNT	0xDC	Digital Compare Filter Window Counter Register	0x00000000
DCCAPCTL	0xE0	Digital Compare Capture Control Register	0x00000000
DCCAP	0xE4	Digital Compare Counter Capture Register	0x00000000
ETCTL*	0xE8	Event-Trigger Control Register	0x0007B16F
ETPS	0xEC	Event-Trigger Prescale Register	0x00000000
ETFLG	0xF0	Event-Trigger Flag Register	0x00000000
ETCLR	0xF4	Event-Trigger Clear Register	0x00000000
ETFRC	0xF8	Event-Trigger Force Register	0x00000000
PWMREGKEY	0xFC	PWM Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the PWMREGKEY=0x1ACCE551.

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10.11.2 PWM registers

10.11.2.1 Shadow Status Register (SHADOWSTS)

Table 10-8: Shadow Status Register (SHADOWSTS) Layout

SHADOWSTS (Shadow Status Register) Offset: 0x0 Default: 0x00000000 Access: PWM -> SHADOWSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					DBFED	DBRED	DBCTL
7	6	5	4	3	2	1	0
AQCSFRC	AQCTLB	AQCTLA	CMPD	CMPC	CMPB	CMPA	TBPRD

Table 10-9: Shadow Status Register (SHADOWSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	DBFED	RO	0x0	DBFED shadow status 0: A load from DBFED to DBFEDA clears this bit 1: Write to DBFED set this bit and overwrite current value in DBFED
9	DBRED	RO	0x0	DBRED shadow status 0: A load from DBRED to DBREDA clears this bit 1: Write to DBRED set this bit and overwrite current value in DBRED
8	DBCTL	RO	0x0	DBCTL shadow status 0: A load from DBCTL to DBCTLA clears this bit 1: Write to DBCTL set this bit and overwrite current value in DBCTL
7	AQCSFRC	RO	0x0	AQCSFRC shadow status 0: A load from AQCSFRC to AQCSFRCA clears this bit 1: Write to AQCSFRC set this bit and overwrite current value in AQCSFRC
6	AQCTLB	RO	0x0	AQCTLB shadow status 0: A load from AQCTLB to AQCTLBA clears this bit 1: Write to AQCTLB set this bit and overwrite current value in AQCTLB

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Bits	Field Name	Type	Reset	Description
5	AQCTLA	RO	0x0	AQCTLA shadow status 0: A load from AQCTLA to AQCTLAA clears this bit 1: Write to AQCTLA set this bit and overwrite current value in AQCTLA
4	CMPD	RO	0x0	CMPD shadow status 0: A load from CMPD to CMPDA clears this bit 1: Write to CMPD set this bit and overwrite current value in CMPD
3	CMPC	RO	0x0	CMPC shadow status 0: A load from CMPC to CMPCA clears this bit 1: Write to CMPC set this bit and overwrite current value in CMPC
2	CMPB	RO	0x0	CMPB shadow status 0: A load from CMPB to CMPBA clears this bit 1: Write to CMPB set this bit and overwrite current value in CMPB
1	CMPA	RO	0x0	CMPA shadow status 0: A load from CMPA to CMPAA clears this bit 1: Write to CMPA set this bit and overwrite current value in CMPA
0	TBPRD	RO	0x0	TBPRD shadow status 0: A load from TBPRD to TBPRDA clears this bit 1: Write to TBPRD set this bit and overwrite current value in TBPRD

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10.11.2.2 Global Shadow to Active Load Control Register 0 (GLDCTL0)

Table 10-10: Global Shadow to Active Load Control Register 0 (GLDCTL0) Layout

GLDCTL0 (Global Shadow to Active Load Control Register 0) Offset: 0x4 Default: 0x00000000 Access: PWM -> GLDCTL0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED			OSTMODE	GLDCNT			
7	6	5	4	3	2	1	0
GLDPRD				GLDLOAD			GLDEN

Table 10-11: Global Shadow to Active Load Control Register 0 (GLDCTL0) Field Description

Bits	Field Name	Type	Reset	Description
31:13	RESERVED_31_13	RO	0x0	Reserved
12	OSTMODE	RW	0x0	One-shot global load mode 0: Global strobe is continuously controlled by GLDPRD and GLDCNT 1: Global strobe is blocked until GLDCTL1.OSTLOAD is written with 1
11:8	GLDCNT	RO	0x0	Global shadow to active load strobe counter It indicates how many selected global load events have occurred
7:4	GLDPRD	RW	0x0	Global shadow to active load strobe period No global load pulse will be generated if GLDPRD=0.Otherwise, the global load pulse is generated uponGLDCNT = GLDPRD. It has no effect if OSTMODE=1
3:1	GLDLOAD	RW	0x0	Global shadow to active load mode 000: Load from shadow to active on TBCNT=0 001: Load from shadow to active on TBCNT=TBPRD 010: Load from shadow to active on TBCNT=0 or TBCNT=TBPRD 011: Load from shadow to active on SYNC event 100: Load from shadow to active on SYNC event or TBCNT=0 101: Load from shadow to active on SYNC event or TBCNT=TBPRD 110: Load from shadow to active on SYNC event, TBCNT=0 or TBCNT=TBPRD 111: Load from shadow to active on software by writing 1 to GLDCTL1.FRCLOAD

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Bits	Field Name	Type	Reset	Description
0	GLDEN	RW	0x0	Global shadow to active load enable 0: Shadow to active load is defined per register regardless of GLDSEL. i.e. CMPA load is always controlled by CMPCTL.CMPALOAD 1: Shadow to active load is globally controlled

10.11.2.3 Global Shadow to Active Load Control Register 1 (GLDCTL1)

Table 10-12: Global Shadow to Active Load Control Register 1 (GLDCTL1) Layout

GLDCTL1 (Global Shadow to Active Load Control Register 1) Offset: 0x8 Default: 0x00000000 Access: PWM -> GLDCTL1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED						FRCLOAD	OSTLOAD

Table 10-13: Global Shadow to Active Load Control Register 1 (GLDCTL1) Field Description

Bits	Field Name	Type	Reset	Description
31:2	RESERVED_31_2	RO	0x0	Reserved
1	FRCLOAD	W1S	0x0	Global force shadow to active load 0: Write a 0 has no effect. Always reads back a 0. 1: Write a 1 generates global load event to the event counter. This bit is self-cleared to 0.
0	OSTLOAD	W1S	0x0	Start the one-shot load pending 0: Write a 0 has no effect. Read a 0 indicates there is no pending one-shot load 1: Write a 1 initialize a one-shot load pending. Upon event defined by GLDCTL0.GLDLOAD, the global load happens and this bit is self-cleared to 0.

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10.11.2.4 Global Shadow to Active Load Select Register (GLDSEL)

Table 10-14: Global Shadow to Active Load Select Register (GLDSEL) Layout

GLDSEL (Global Shadow to Active Load Select Register) Offset: 0xC Default: 0x00000000 Access: PWM -> GLDSEL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					DBFED	DBRED	DBCTL
7	6	5	4	3	2	1	0
AQCSFRC	AQCTLB	AQCTLA	CMPD	CMPC	CMPB	CMPA	TBPRD

Table 10-15: Global Shadow to Active Load Select Register (GLDSEL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	DBFED	RW	0x0	DBFED global shadow to active load select 0: Shadow to active load is controlled by DBCTL.DBFEDLOAD 1: Shadow to active load is controlled by GLDCTL
9	DBRED	RW	0x0	DBRED global shadow to active load select 0: Shadow to active load is controlled by DBCTL.DBREDLOAD 1: Shadow to active load is controlled by GLDCTL
8	DBCTL	RW	0x0	DBCTL global shadow to active load select 0: Shadow to active load is controlled by DBCTL.DBCTLLOAD 1: Shadow to active load is controlled by GLDCTL
7	AQCSFRC	RW	0x0	AQCSFRC global shadow to active load select 0: Shadow to active load is controlled by AQSFRC.CSFLOAD 1: Shadow to active load is controlled by GLDCTL
6	AQCTLB	RW	0x0	AQCTLB global shadow to active load select 0: Shadow to active load is controlled by AQCTL.AQCTLBLOAD 1: Shadow to active load is controlled by GLDCTL
5	AQCTLA	RW	0x0	AQCTLA global shadow to active load select 0: Shadow to active load is controlled by AQCTL.AQCTLALOAD 1: Shadow to active load is controlled by GLDCTL
4	CMPD	RW	0x0	CMPD global shadow to active load select

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Bits	Field Name	Type	Reset	Description
				0: Shadow to active load is controlled by CMPCTL.CMPDLOAD 1: Shadow to active load is controlled by GLDCTL
3	CMPC	RW	0x0	CMPC global shadow to active load select 0: Shadow to active load is controlled by CMPCTL.CMPCLOAD 1: Shadow to active load is controlled by GLDCTL
2	CMPB	RW	0x0	CMPB global shadow to active load select 0: Shadow to active load is controlled by CMPCTL.CMPBLOAD 1: Shadow to active load is controlled by GLDCTL
1	CMPA	RW	0x0	CMPA global shadow to active load select 0: Shadow to active load is controlled by CMPCTL.CMPALOAD 1: Shadow to active load is controlled by GLDCTL
0	TBPRD	RW	0x0	TBPRD global shadow to active load select 0: Shadow to active load is controlled by TBCTL.TBPRDLOAD 1: Shadow to active load is controlled by GLDCTL

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10.11.2.5 PWM Link Control Register (PWMLINK)

Table 10-16: PWM Link Control Register (PWMLINK) Layout

PWMLINK (PWM Link Control Register) Offset: 0x10 Default: 0xFFFFFFFF
Access: PWM -> PWMLINK.all

31	30	29	28	27	26	25	24
GLDCTL1				DBFED			
23	22	21	20	19	18	17	16
DBRED				CMPD			
15	14	13	12	11	10	9	8
CMPC				CMPB			
7	6	5	4	3	2	1	0
CMPA				TBPRD			

Table 10-17: PWM Link Control Register (PWMLINK) Field Description

Bits	Field Name	Type	Reset	Description
31:28	GLDCTL1	RW	0xF	Write to the GLDCTL1 of PWM selected by PWMLINK.GLDCTL1 results in simultaneous write to GLDCTL1 of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2 0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected
27:24	DBFED	RW	0xF	Write to the DBFED of PWM selected by PWMLINK.DBFED results in simultaneous write to DBFED of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2 0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected
23:20	DBRED	RW	0xF	Write to the DBRED of PWM selected by PWMLINK.DBRED results in simultaneous write to DBRED of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2

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Bits	Field Name	Type	Reset	Description
				0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected
19:16	CMPD	RW	0xF	Write to the CMPD of PWM selected by PWMLINK.CMPD results in simultaneous write to CMPD of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2 0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected
15:12	CMPC	RW	0xF	Write to the CMPC of PWM selected by PWMLINK.CMPC results in simultaneous write to CMPC of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2 0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected
11:8	CMPB	RW	0xF	Write to the CMPB of PWM selected by PWMLINK.CMPB results in simultaneous write to CMPB of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2 0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected

SPINTROL

Bits	Field Name	Type	Reset	Description
7:4	CMPA	RW	0xF	Write to the CMPA of PWM selected by PWMLINK.CMPA results in simultaneous write to CMPA of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2 0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected
3:0	TBPRD	RW	0xF	Write to the TBPRD of PWM selected by PWMLINK.TBPRD results in simultaneous write to TBPRD of current PWM module 0000: Select PWM0 0001: Select PWM1 0010: Select PWM2 0011: Select PWM3 0100: Select PWM4 0101: Select PWM5 0110: Select PWM6 0111: Select PWM7 Others: No PWM selected

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10.11.2.6 Time-Base Control Register (TBCTL)

Table 10-18: Time-Base Control Register (TBCTL) Layout

TBCTL (Time-Base Control Register) Offset: 0x14 Default: 0x00000006 Access: PWM -> TBCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED				DBGRUN		TBDIVBIN	
15	14	13	12	11	10	9	8
TBDIVBIN	TBDIVLIN			FRCSYNC	SYNCOSEL		
7	6	5	4	3	2	1	0
TBPRDLOCK	TBPRDLOAD		PHSDIR	PHSEN	CNTMODE		CNTRUN

Table 10-19: Time-Base Control Register (TBCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19:18	DBGRUN	RW	0x0	PWM counter 233rotocol when CPU is halted Note: Debug operation and CPU fault exceptions both can cause CPU halted. 00: Stop after the next time-base counter increment or decrement 01: Stop when TBCNT completes a whole cycle (TBCNT=TBPRD for up-count mode and TBCNT=0 for other modes) 1x: Counter keep running when CPU is halted
17:15	TBDIVBIN	RW	0x0	Binary part of TBCLK dividing ratio from PWM clock input. Overall dividing ratio is $2^{TBDIVBIN}$ x (TBDIVLIN+1) 0: Divide by 1 (default on reset) 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32 6: Divide by 64 7: Divide by 128
14:12	TBDIVLIN	RW	0x0	Lineary part of TBCLK dividing ratio from PWM clock input. Overall dividing ratio is $2^{TBDIVBIN}$ x (TBDIVLIN+1) 0: Divide by 1 (default on reset) 1: Divide by 2 2: Divide by 3

SPINTROL

Bits	Field Name	Type	Reset	Description
				3: Divide by 4 4: Divide by 5 5: Divide by 6 6: Divide by 7 7: Divide by 8
11	FRCSYNC	W1S	0x0	Software forced synchronization 0: Write a 0 has no effect and always readback 0 1: Write a 1 forces a one-time synchronization pulse. This bit is self-cleared to 0 and not affected by PWMREGKEY protection
10:8	SYNCOSEL	RW	0x0	Synchronization output select 000: SYNCI and the software forced sync 001: TBCNT=0 event 010: TBCNT=TBPRD event 011: TBCNT=CMPA event 100: TBCNT=CMPB event 101: TBCNT=CMPC event 110: TBCNT=CMPD event 111: Disable SYNCO
7	TBPRDLOCK	RW	0x0	TBPRD active value lock 0: Active value in TBPRDA is updated according to TBCTL.TBPRDLOAD 1: Active value in TBPRDA will not change
6:5	TBPRDLOAD	RW	0x0	TBPRD active value load mode It has no effect when TBCTL.TBPRDLOCK=1 00: Load TBPRD into TBPRDA on TBCNT=0 01: Load TBPRD into TBPRDA on SYNC event 10: Load TBPRD into TBPRDA on SYNC event or TBCNT=0 11: Write TBPRD will immediately change the active value in TBPRDA
4	PHSDIR	RW	0x0	Phase direction It is valid only when TBCNT is in up-down-count mode (CNTMODE=0x2) 0: Count down after synchronization event 1: Count up after synchronization event
3	PHSEN	RW	0x0	Phase register enable 0: Do not load time-base counter (TBCNT) from time-base phase register (TBPHS)

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Bits	Field Name	Type	Reset	Description
				1: Load TBCNT from TBPHS when synchronization event occurs (SYNCI input, software synchronization or digital compare sync event)
2:1	CNTMODE	RW	0x3	Counter mode 00: Down-count 01: Up-count 10: Up-down-count 11: Stop and freeze (default on reset)
0	CNTRUN	RW	0x0	Counter run/stop control 0: Counter stop 1: Counter free-running

10.11.2.7 Time-Base Period Register (TBPRD)

Table 10-20: Time-Base Period Register (TBPRD) Layout

TBPRD (Time-Base Period Register) Offset: 0x18 Default: 0x00000000 Access: PWM -> TBPRD.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-21: Time-Base Period Register (TBPRD) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Time-base counter period

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10.11.2.8 Time-Base Period Active Register (TBPRDA)

Table 10-22: Time-Base Period Active Register (TBPRDA) Layout

TBPRDA (Time-Base Period Active Register) Offset: 0x1C Default: 0x00000000 Access: PWM -> TBPRDA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-23: Time-Base Period Active Register (TBPRDA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Time-base counter active period When TBCTL.PRDLOAD=0x3, write to TBPRD directly affects this register. Otherwise, the value is loaded from TBPRD upon the events defined in TBCTL.PRDLOAD.

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10.11.2.9 Time-Base Phase Register (TBPHS)

Table 10-24: Time-Base Phase Register (TBPHS) Layout

TBPHS (Time-Base Phase Register) Offset: 0x20 Default: 0x00000000 Access: PWM -> TBPHS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-25: Time-Base Phase Register (TBPHS) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Time-base counter phase when synchronization event occurs TBCTL.PHSEN=0: The synchronization event is ignored and TBCNT keeps its value. TBCTL.PHSEN=1: Time-base counter (TBCNT) will be loaded with TBPHS when synchronization event occurs.

10.11.2.10 Time-Base Counter Register (TBCNT)

Table 10-26: Time-Base Counter Register (TBCNT) Layout

TBCNT (Time-Base Counter Register) Offset: 0x24 Default: 0x00000000 Access: PWM -> TBCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-27: Time-Base Counter Register (TBCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Current value of the time-base counter

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10.11.2.11 Time-Base Status Register (TBSTS)

Table 10-28: Time-Base Status Register (TBSTS) Layout

TBSTS (Time-Base Status Register) Offset: 0x28 Default: 0x00000100 Access: PWM -> TBSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							CNTDIR
7	6	5	4	3	2	1	0
CNTCMPD	CNTCMPC	CNTCMPB	CNTCMPA	CNTPRD	CNTZRO	CNTMAX	SYNCI

Table 10-29: Time-Base Status Register (TBSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	CNTDIR	RO	0x1	Time-base counter direction status 0: Time-base counter is currently counting down 1: Time-base counter is currently counting up
7	CNTCMPD	RO	0x0	Time-base counter reaching CMPD latched status 0: TBCNT never reaches CMPD 1: TBCNT reached CMPD
6	CNTCMPC	RO	0x0	Time-base counter reaching CMPC latched status 0: TBCNT never reaches CMPC 1: TBCNT reached CMPC
5	CNTCMPB	RO	0x0	Time-base counter reaching CMPB latched status 0: TBCNT never reaches CMPB 1: TBCNT reached CMPB
4	CNTCMPA	RO	0x0	Time-base counter reaching CMPA latched status 0: TBCNTnever reaches CMPA 1: TBCNT reached CMPA
3	CNTPRD	RO	0x0	Time-base counter reaching period latched status 0: TBCNT never reaches TBPRD 1: TBCNT reached TBPRD
2	CNTZRO	RO	0x0	Time-base counter reaching zero latched status 0: TBCNT never reaches 0x0000 1: TBCNT reached 0xFFFF
1	CNTMAX	RO	0x0	Time-base counter reaching max latched status 0: TBCNT never reaches 0xFFFF 1: TBCNT reached 0xFFFF
0	SYNCI	RO	0x0	Input synchronization latched status 0: No input synchronization event has occurred 1: An input synchronization event has occurred

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10.11.2.12 Time-Base Status Clear Register (TBSTSCLR)

Table 10-30: Time-Base Status Clear Register (TBSTSCLR) Layout

TBSTSCLR (Time-Base Status Clear Register) Offset: 0x2C Default: 0x00000000 Access: PWM -> TBSTSCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7 CNTCMPD	6 CNTCMPC	5 CNTCMPB	4 CNTCMPA	3 CNTPRD	2 CNTZRO	1 CNTMAX	0 SYNCI

Table 10-31: Time-Base Status Clear Register (TBSTSCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	CNTCMPD	W1C	0x0	Time-base counter reaching CMPD status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.
6	CNTCMPC	W1C	0x0	Time-base counter reaching CMPC status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.
5	CNTCMPB	W1C	0x0	Time-base counter reaching CMPB status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.
4	CNTCMPA	W1C	0x0	Time-base counter reaching CMPA status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.
3	CNTPRD	W1C	0x0	Time-base counter reaching period status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.
2	CNTZRO	W1C	0x0	Time-base counter reaching zero status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.

SPINTROL

Bits	Field Name	Type	Reset	Description
1	CNTMAX	W1C	0x0	Time-base counter reaching max status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.
0	SYNCI	W1C	0x0	Input synchronization status clear 0: Writing a 0 has no effect. Always readback 0. 1: Writing a 1 clears the latched status. This bit is self-cleared to 0.

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10.11.2.13 Counter-Compare Control Register (CMPCTL)

Table 10-32: Counter-Compare Control Register (CMPCTL) Layout

CMPCTL (Counter-Compare Control Register) Offset: 0x30 Default: 0x00000000 Access: PWM -> CMPCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
CMPDLOCK	CMPDLOAD			CMPCLOCK	CMPCLOAD		
7	6	5	4	3	2	1	0
CMPBLOCK	CMPBLOAD			CMPALOCK	CMPALOAD		

Table 10-33: Counter-Compare Control Register (CMPCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	CMPDLOCK	RW	0x0	CMPD active value lock 0: Active value in CMPDA is updated according to CMPCTL.CMPDLOAD 1: Active value in CMPDA will not change
14:12	CMPDLOAD	RW	0x0	CMPD active value load mode It has no effect when CMPCTL.CMPDLOCK=1 000: Load CMPD into CMPDA on TBCNT=0 001: Load CMPD into CMPDA on TBCNT=TBPRD 010: Load CMPD into CMPDA on TBCNT=0 or TBCNT=TBPRD 011: Load CMPD into CMPDA on SYNC event 100: Load CMPD into CMPDA on SYNC event or TBCNT=0 101: Load CMPD into CMPDA on SYNC event or TBCNT=TBPRD 110: Load CMPD into CMPDA on SYNC event, TBCNT=0 or TBCNT=TBPRD 111: Write CMPD will immediately change the active value in CMPDA
11	CMPCLOCK	RW	0x0	CMPC active value lock 0: Active value in CMPCA is updated according to CMPCTL.CMPCLOAD 1: Active value in CMPCA will not change
10:8	CMPCLOAD	RW	0x0	CMPC active value load mode It has no effect when CMPCTL.CMPCLOCK=1

SPINTROL

Bits	Field Name	Type	Reset	Description
				000: Load CMPC into CMPCA on TBCNT=0 001: Load CMPC into CMPCA on TBCNT=TBPRD 010: Load CMPC into CMPCA on TBCNT=0 or TBCNT=TBPRD 011: Load CMPC into CMPCA on SYNC event 100: Load CMPC into CMPCA on SYNC event or TBCNT=0 101: Load CMPC into CMPCA on SYNC event or TBCNT=TBPRD 110: Load CMPC into CMPCA on SYNC event, TBCNT=0 or TBCNT=TBPRD 111: Write CMPC will immediately change the active value in CMPCA
7	CMPBLOCK	RW	0x0	CMPB active value lock 0: Active value in CMPBA is updated according to CMPBTL.CMPBLOAD 1: Active value in CMPBA will not change
6:4	CMPBLOAD	RW	0x0	CMPB active value load mode It has no effect when CMPBTL.CMPBLOCK=1 000: Load CMPB into CMPBA on TBCNT=0 001: Load CMPB into CMPBA on TBCNT=TBPRD 010: Load CMPB into CMPBA on TBCNT=0 or TBCNT=TBPRD 011: Load CMPB into CMPBA on SYNC event 100: Load CMPB into CMPBA on SYNC event or TBCNT=0 101: Load CMPB into CMPBA on SYNC event or TBCNT=TBPRD 110: Load CMPB into CMPBA on SYNC event, TBCNT=0 or TBCNT=TBPRD 111: Write CMPB will immediately change the active value in CMPBA
3	CMPALOCK	RW	0x0	CMPA active value lock 0: Active value in CMPAA is updated according to CMPATL.CMPALOAD 1: Active value in CMPAA will not change
2:0	CMPALOAD	RW	0x0	CMPA active value load mode It has no effect when CMPATL.CMPALOCK=1 000: Load CMPA into CMPAA on TBCNT=0

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Bits	Field Name	Type	Reset	Description
				001: Load CMPA into CMPAA on TBCNT=TBPRD 010: Load CMPA into CMPAA on TBCNT=0 or TBCNT=TBPRD 011: Load CMPA into CMPAA on SYNC event 100: Load CMPA into CMPAA on SYNC event or TBCNT=0 101: Load CMPA into CMPAA on SYNC event or TBCNT=TBPRD 110: Load CMPA into CMPAA on SYNC event, TBCNT=0 or TBCNT=TBPRD 111: Write CMPA will immediately change the active value in CMPAA

10.11.2.14 Counter-Compare A Threshold Register (CMPA)

Table 10-34: Counter-Compare A Threshold Register (CMPA) Layout

CMPA (Counter-Compare A Threshold Register) Offset: 0x34 Default: 0x00000000 Access: PWM -> CMPA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-35: Counter-Compare A Threshold Register (CMPA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Comparator A threshold

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10.11.2.15 Counter-Compare A Threshold Active Register (CMPAA)

Table 10-36: Counter-Compare A Threshold Active Register (CMPAA) Layout

CMPAA (Counter-Compare A Threshold Active Register) Offset: 0x38 Default: 0x00000000 Access: PWM -> CMPAA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-37: Counter-Compare A Threshold Active Register (CMPAA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Comparator A threshold active value A TBCNT=CMPA event will be generated while TBCNT is equal to the threshold value

10.11.2.16 Counter-Compare B Threshold Register (CMPB)

Table 10-38: Counter-Compare B Threshold Register (CMPB) Layout

CMPB (Counter-Compare B Threshold Register) Offset: 0x3C Default: 0x00000000 Access: PWM -> CMPB.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-39: Counter-Compare B Threshold Register (CMPB) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Comparator B threshold

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10.11.2.17 Counter-Compare B Threshold Active Register (CMPBA)

Table 10-40: Counter-Compare B Threshold Active Register (CMPBA) Layout

CMPBA (Counter-Compare B Threshold Active Register) Offset: 0x40 Default: 0x00000000 Access: PWM -> CMPBA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-41: Counter-Compare B Threshold Active Register (CMPBA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Comparator B threshold active value A TBCNT=CMPB event will be generated while TBCNT is equal to the threshold value

10.11.2.18 Counter-Compare C Threshold Register (CMPC)

Table 10-42: Counter-Compare C Threshold Register (CMPC) Layout

CMPC (Counter-Compare C Threshold Register) Offset: 0x44 Default: 0x00000000 Access: PWM -> CMPC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-43: Counter-Compare C Threshold Register (CMPC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Comparator C threshold

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10.11.2.19 Counter-Compare C Threshold Active Register (CMPCA)

Table 10-44: Counter-Compare C Threshold Active Register (CMPCA) Layout

CMPCA (Counter-Compare C Threshold Active Register) Offset: 0x48 Default: 0x00000000 Access: PWM -> CMPCA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-45: Counter-Compare C Threshold Active Register (CMPCA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Comparator C threshold active value A TBCNT=CMPC event will be generated while TBCNT is equal to the threshold value

10.11.2.20 Counter-Compare D Threshold Register (CMPD)

Table 10-46: Counter-Compare D Threshold Register (CMPD) Layout

CMPD (Counter-Compare D Threshold Register) Offset: 0x4C Default: 0x00000000 Access: PWM -> CMPD.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-47: Counter-Compare D Threshold Register (CMPD) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Comparator D threshold

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10.11.2.21 Counter-Compare D Threshold Active Register (CMPDA)

Table 10-48: Counter-Compare D Threshold Active Register (CMPDA) Layout

CMPDA (Counter-Compare D Threshold Active Register) Offset: 0x50 Default: 0x00000000 Access: PWM -> CMPDA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-49: Counter-Compare D Threshold Active Register (CMPDA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Comparator D threshold active value A TBCNT=CMPD event will be generated while TBCNT is equal to the threshold value

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10.11.2.22 Action-Qualifier Control Register (AQCTL)

Table 10-50: Action-Qualifier Control Register (AQCTL) Layout

AQCTL (Action-Qualifier Control Register) Offset: 0x54 Default: 0x00000000
Access: PWM -> AQCTL.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
T1SEL				T0SEL			
7	6	5	4	3	2	1	0
AQCTLBLOCK	AQCTLBLOAD			AQCTLALOCK	AQCTLALOAD		

Table 10-51: Action-Qualifier Control Register (AQCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:12	T1SEL	RW	0x0	T1 event source select 0000: DCAEVT0 0001: DCAEVT1 0010: DCBEVT0 0011: DCBEVT1 0100: TZ0 0101: TZ1 0110: TZ2 0111: TZ3 1000: TZ4 1001: SYNCI Others: T1 event is disabled
11:8	T0SEL	RW	0x0	T0 event source select 0000: DCAEVT0 0001: DCAEVT1 0010: DCBEVT0 0011: DCBEVT1 0100: TZ0 0101: TZ1 0110: TZ2 0111: TZ3 1000: TZ4 1001: SYNCI Others: T0 event is disabled
7	AQCTLBLOCK	RW	0x0	AQCTLB active value lock 0: Active value in AQCTLBA is updated according to AQCTL.AQCTLBLOAD 1: Active value in AQCTLBA will not change

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Bits	Field Name	Type	Reset	Description
6:4	AQCTLBLOAD	RW	0x0	AQCTLB active value load mode It has no effect when AQCTL.AQCTLBLOCK=1 000: Load AQCTLB into AQCTLBA on TBCNT=0 001: Load AQCTLB into AQCTLBA on TBCNT=TBPRD 010: Load AQCTLB into AQCTLBA on TBCNT=0 or TBCNT=TBPRD 011: Load AQCTLB into AQCTLBA on SYNC event 100: Load AQCTLB into AQCTLBA on SYNC event or TBCNT=0 101: Load AQCTLB into AQCTLBA on SYNC event or TBCNT=TBPRD 110: Load AQCTLB into AQCTLBA on SYNC event, TBCNT=0 or TBCNT=TBPRD 111: Write AQCTLB immediately change the active value in AQCTLBA
3	AQCTLALOCK	RW	0x0	AQCTLA active value lock 0: Active value in AQCTLAA is updated according to AQCTL.AQCTLALOAD 1: Active value in AQCTLAA will not change
2:0	AQCTLALOAD	RW	0x0	AQCTLA active value load mode It has no effect when AQCTL.AQCTLALOCK=1 000: Load AQCTLA into AQCTLAA on TBCNT=0 001: Load AQCTLA into AQCTLAA on TBCNT=TBPRD 010: Load AQCTLA into AQCTLAA on TBCNT=0 or TBCNT=TBPRD 011: Load AQCTLA into AQCTLAA on SYNC event 100: Load AQCTLA into AQCTLAA on SYNC event or TBCNT=0 101: Load AQCTLA into AQCTLAA on SYNC event or TBCNT=TBPRD 110: Load AQCTLA into AQCTLAA on SYNC event, TBCNT=0 or TBCNT=TBPRD 111: Write AQCTLA immediately change the active value in AQCTLAA

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10.11.2.23 Action-Qualifier Output A Control Register (AQCTLA)

Table 10-52: Action-Qualifier Output A Control Register (AQCTLA) Layout

AQCTLA (Action-Qualifier Output A Control Register) Offset: 0x58 Default: 0x00000000
Access: PWM -> AQCTLA.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED				T1D		T1U	
15	14	13	12	11	10	9	8
T0D		T0U		CBD		CBU	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	

Table 10-53: Action-Qualifier Output A Control Register (AQCTLA) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19:18	T1D	RW	0x0	Action on output A when T1 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
17:16	T1U	RW	0x0	Action on output A when T1 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
15:14	T0D	RW	0x0	Action on output A when T0 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
13:12	T0U	RW	0x0	Action on output A when T0 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
11:10	CBD	RW	0x0	Action on output A when TBCNT=CMPB and TBCNT is counting down

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Bits	Field Name	Type	Reset	Description
				00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
9:8	CBU	RW	0x0	Action on output A when TBCNT=CMPB and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
7:6	CAD	RW	0x0	Action on output A when TBCNT=CMPA and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
5:4	CAU	RW	0x0	Action on output A when TBCNT=CMPA and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
3:2	PRD	RW	0x0	Action on output A when TBCNT=TBPRD 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
1:0	ZRO	RW	0x0	Action on output A when TBCNT=Zero 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)

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10.11.2.24 Action-Qualifier Output A Control Active Register (AQCTLAA)

Table 10-54: Action-Qualifier Output A Control Active Register (AQCTLAA) Layout

AQCTLAA (Action-Qualifier Output A Control Active Register) Offset: 0x5C Default: 0x00000000
Access: PWM -> AQCTLAA.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED				T1D		T1U	
15	14	13	12	11	10	9	8
T0D		T0U		CBD		CBU	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	

Table 10-55: Action-Qualifier Output A Control Active Register (AQCTLAA) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19:18	T1D	RO	0x0	Action on output A when T1 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
17:16	T1U	RO	0x0	Action on output A when T1 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
15:14	T0D	RO	0x0	Action on output A when T0 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
13:12	T0U	RO	0x0	Action on output A when T0 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
11:10	CBD	RO	0x0	Action on output A when TBCNT=CMPB and TBCNT is counting down

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Bits	Field Name	Type	Reset	Description
				00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
9:8	CBU	RO	0x0	Action on output A when TBCNT=CMPB and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
7:6	CAD	RO	0x0	Action on output A when TBCNT=CMPA and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
5:4	CAU	RO	0x0	Action on output A when TBCNT=CMPA and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
3:2	PRD	RO	0x0	Action on output A when TBCNT=TBPRD 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)
1:0	ZRO	RO	0x0	Action on output A when TBCNT=Zero 00: Do nothing (action disabled) 01: Clear (force PWM output A to low) 10: Set (force PWM output A to high) 11: Toggle (invert current PWM output A status)

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10.11.2.25 Action-Qualifier Output B Control Register (AQCTLB)

Table 10-56: Action-Qualifier Output B Control Register (AQCTLB) Layout

AQCTLB (Action-Qualifier Output B Control Register) Offset: 0x60 Default: 0x00000000
Access: PWM -> AQCTLB.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED				T1D		T1U	
15	14	13	12	11	10	9	8
T0D		T0U		CBD		CBU	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	

Table 10-57: Action-Qualifier Output B Control Register (AQCTLB) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19:18	T1D	RW	0x0	Action on output B when T1 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
17:16	T1U	RW	0x0	Action on output B when T1 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
15:14	T0D	RW	0x0	Action on output B when T0 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
13:12	T0U	RW	0x0	Action on output B when T0 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
11:10	CBD	RW	0x0	Action on output B when TBCNT=CMPA and TBCNT is counting down

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Bits	Field Name	Type	Reset	Description
				00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
9:8	CBU	RW	0x0	Action on output B when TBCNT=CMPB and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
7:6	CAD	RW	0x0	Action on output B when TBCNT=CMPA and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
5:4	CAU	RW	0x0	Action on output B when TBCNT=CMPA and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
3:2	PRD	RW	0x0	Action on output B when TBCNT=TBPRD 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
1:0	ZRO	RW	0x0	Action on output B when TBCNT=Zero 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)

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10.11.2.26 Action-Qualifier Output B Control Active Register (AQCTLBA)

Table 10-58: Action-Qualifier Output B Control Active Register (AQCTLBA) Layout

AQCTLBA (Action-Qualifier Output B Control Active Register) Offset: 0x64 Default: 0x00000000
Access: PWM -> AQCTLBA.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED				T1D		T1U	
15	14	13	12	11	10	9	8
T0D		T0U		CBD		CBU	
7	6	5	4	3	2	1	0
CAD		CAU		PRD		ZRO	

Table 10-59: Action-Qualifier Output B Control Active Register (AQCTLBA) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19:18	T1D	RO	0x0	Action on output B when T1 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
17:16	T1U	RO	0x0	Action on output B when T1 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
15:14	T0D	RO	0x0	Action on output B when T0 event and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
13:12	T0U	RO	0x0	Action on output B when T0 event and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
11:10	CBD	RO	0x0	Action on output B when TBCNT=CMPA and TBCNT is counting down

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Bits	Field Name	Type	Reset	Description
				00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
9:8	CBU	RO	0x0	Action on output B when TBCNT=CMPB and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
7:6	CAD	RO	0x0	Action on output B when TBCNT=CMPA and TBCNT is counting down 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
5:4	CAU	RO	0x0	Action on output B when TBCNT=CMPA and TBCNT is counting up 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
3:2	PRD	RO	0x0	Action on output B when TBCNT=TBPRD 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)
1:0	ZRO	RO	0x0	Action on output B when TBCNT=Zero 00: Do nothing (action disabled) 01: Clear (force PWM output B to low) 10: Set (force PWM output B to high) 11: Toggle (invert current PWM output B status)

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10.11.2.27 Action-Qualifier Software Force Register (AQSFRC)

Table 10-60: Action-Qualifier Software Force Register (AQSFRC) Layout

AQSFRC (Action-Qualifier Software Force Register) Offset: 0x68 Default: 0x00000000 Access: PWM -> AQSFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
CSFLOAD		OTSFB	ACTSFB		OTSFA	ACTSFA	

Table 10-61: Action-Qualifier Software Force Register (AQSFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:6	CSFLOAD	RW	0x0	Options to load continuous software force register (AQCSFRC) active value from shadow register 00: Load from AQCSFRC into AQCSFRCA on TBCNT=0 01: Load from AQCSFRC into AQCSFRCA on TBCNT=TBPRD 10: Load from AQCSFRC into AQCSFRCA on TBCNT=Zero or TBCNT=TBPRD 11: Write AQCSFRC immediately change the active value in AQCSFRCA
5	OTSFB	W1S	0x0	One-time software forced event on output B 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 initialize a one-cycle force pulse. This bit is self-cleared to 0
4:3	ACTSFB	RW	0x0	Action when one-time software force B is invoked 00: Do nothing (action disabled) 01: Clear (force PWM output B to low 10: Set (force PWM output B to high 11: Toggle (invert current PWM AQ output B state)
2	OTSFA	W1S	0x0	One-time software forced event on output A 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 initialize a one-cycle force pulse. This bit is self-cleared to 0
1:0	ACTSFA	RW	0x0	Action when one-time software force A is invoked 00: Do nothing (action disabled) 01: Clear (force PWM output A to low 10: Set (force PWM output A to high 11: Toggle (invert current PWM AQ output A state)

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10.11.2.28 Action-Qualifier Continuous Software Force Register (AQCSFRC)

Table 10-62: Action-Qualifier Continuous Software Force Register (AQCSFRC) Layout

AQCSFRC (Action-Qualifier Continuous Software Force Register) Offset: 0x6C Default: 0x00000000 Access: PWM -> AQCSFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				CSFB		CSFA	

Table 10-63: Action-Qualifier Continuous Software Force Register (AQCSFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3:2	CSFB	RW	0x0	Continuous software force on output B 00: Forcing disabled 01: Force a continuous low on output B 10: Force a continuous high on output B 11: Invalid option
1:0	CSFA	RW	0x0	Continuous software force on output A 00: Forcing disabled 01: Force a continuous low on output A 10: Force a continuous high on output A 11: Invalid option

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10.11.2.29 Action-Qualifier Continuous Software Force Active Register (AQCSFRCA)

Table 10-64: Action-Qualifier Continuous Software Force Active Register (AQCSFRCA) Layout

AQCSFRCA (Action-Qualifier Continuous Software Force Active Register) Offset: 0x70 Default: 0x00000000 Access: PWM -> AQCSFRCA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				CSFB		CSFA	

Table 10-65: Action-Qualifier Continuous Software Force Active Register (AQCSFRCA) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3:2	CSFB	RO	0x0	Continuous software force on output B 00: Forcing disabled 01: Force a continuous low on output B 10: Force a continuous high on output B 11: Invalid option
1:0	CSFA	RO	0x0	Continuous software force on output A 00: Forcing disabled 01: Force a continuous low on output A 10: Force a continuous high on output A 11: Invalid option

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10.11.2.30 Dead-Band Generator Control Register (DBCTL)

Table 10-66: Dead-Band Generator Control Register (DBCTL) Layout

DBCTL (Dead-Band Generator Control Register) Offset: 0x74 Default: 0x00000070
Access: PWM -> DBCTL.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					DBFEDLOCK	DBFEDLOAD	
15	14	13	12	11	10	9	8
DBREDLOCK	DBREDLOAD		DBCTLLOCK	DBCTLLOAD		HALFCYCLE	DUALEDGE
7	6	5	4	3	2	1	0
OUTBSRC	OUTASRC	FEDPOL	REDPOL	FEDSRC	REDSRC	FEDEN	REDEN

Table 10-67: Dead-Band Generator Control Register (DBCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:19	RESERVED_31_19	RO	0x0	Reserved
18	DBFEDLOCK	RW	0x0	DBFED active value lock 0: Active value in DBFEDA is updated according to DBCTL.DBFEDLOAD 1: Active value in DBFEDA will not change
17:16	DBFEDLOAD	RW	0x0	DBFED active value load mode It has no effect when DBCTL.DBFEDLOCK=1 00: Load DBFED into DBFEDA on TBCNT=0 01: Load DBFED into DBFEDA on TBCNT=TBPRD 10: Load DBFED into DBFEDA on TBCNT=0 or TBCNT=TBPRD 11: Write DBFED immediately change the active value in DBFEDA
15	DBREDLOCK	RW	0x0	DBRED active value lock 0: Active value in DBREDA is updated according to DBCTL.DBREDLOAD 1: Active value in DBREDA will not change
14:13	DBREDLOAD	RW	0x0	DBRED active value load mode It has no effect when DBCTL.DBFEDLOCK=1 00: Load DBRED into DBREDA on TBCNT=0 01: Load DBRED into DBREDA on TBCNT=TBPRD 10: Load DBRED into DBREDA on TBCNT=0 or TBCNT=TBPRD 11: Write DBRED will immediately change the active value in DBREDA

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Bits	Field Name	Type	Reset	Description
12	DBCTLLOCK	RW	0x0	DBCTL[9:0] active value lock 0: Active value in DBCTLA is updated according to DBCTL.DBCTLLOAD 1: Active value in DBCTLA will not change
11:10	DBCTLLOAD	RW	0x0	DBCTL[9:0] active value load mode It has no effect when DBCTL.DBCTLLOCK=1 00: Load DBCTL[9:0] into DBCTLA on TBCNT=0 01: Load DBCTL[9:0] into DBCTLA on TBCNT=TBPRD 10: Load DBCTL[9:0] into DBCTLA on TBCNT=0 or TBCNT=TBPRD 11: Write DBCTL[9:0] will immediately change the active value in DBCTLA
9	HALFCYCLE	RW	0x0	Half cycle clocking enable 0: Full cycle clocking enabled. The dead-band counter is clocked at TBCLK. 1: Half cycle clocking enabled. The dead-band counter is clocked at 2x TBCLK.
8	DUALEDGE	RW	0x0	Dual-edge delay mode 0: Rising-edge delay and falling-edge delay are two separate paths 1: Rising-edge delay path output serves as input for Falling-edge delay path
7	OUTBSRC	RW	0x0	Output B source 0: Falling-edge delay path is selected as output B 1: Rising-edge delay path is selected as output B
6	OUTASRC	RW	0x1	Output A source 0: Falling-edge delay path is selected as output A 1: Rising-edge delay path is selected as output A
5	FEDPOL	RW	0x1	Falling-edge delay output polarity 0: Falling-edge delay output is inverted to have active-low polarity 1: Falling-edge delay output keeps the original active-high polarity
4	REDPOL	RW	0x1	Rising-edge delay output polarity 0: Rising-edge delay output is inverted to have active-low polarity 1: Rising-edge delay output keeps the original active-high polarity

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Bits	Field Name	Type	Reset	Description
3	FEDSRC	RW	0x0	Falling-edge delay source 0: Input A is the source for falling-edge delay 1: Input B is the source for falling-edge delay
2	REDSRC	RW	0x0	Rising-edge delay source 0: Input A is the source for rising-edge delay 1: Input B is the source for rising-edge delay
1	FEDEN	RW	0x0	Falling-edge delay enable 0: Falling-edge delay is bypassed and the input from action-qualifier goes to the submodule directly 1: Falling-edge delay is enabled and applied at output B
0	REDEN	RW	0x0	Rising-edge delay enable 0: Rising-edge delay is bypassed and the input from action-qualifier goes to the submodule directly 1: Rising-edge delay is enabled and applied at output A

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10.11.2.31 Dead-Band Generator Control Active Register (DBCTLA)

Table 10-68: Dead-Band Generator Control Active Register (DBCTLA) Layout

DBCTLA (Dead-Band Generator Control Active Register) Offset: 0x78 Default: 0x00000070 Access: PWM -> DBCTLA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						HALFCYCLE	DUALEDGE
7	6	5	4	3	2	1	0
OUTBSRC	OUTASRC	FEDPOL	REDPOL	FEDSRC	REDSRC	FEDEN	REDEN

Table 10-69: Dead-Band Generator Control Active Register (DBCTLA) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9	HALFCYCLE	RO	0x0	Half cycle clocking enable 0: Full cycle clocking enabled. The dead-band counter is clocked at TBCLK. 1: Half cycle clocking enabled. The dead-band counter is clocked at 2x TBCLK.
8	DUALEDGE	RO	0x0	Dual-edge delay mode 0: Rising-edge delay and falling-edge delay are two separate paths 1: Rising-edge delay path output serves as input for Falling-edge delay path
7	OUTBSRC	RO	0x0	Output B source 0: Falling-edge delay path is selected as output B 1: Rising-edge delay path is selected as output B
6	OUTASRC	RO	0x1	Output A source 0: Falling-edge delay path is selected as output A 1: Rising-edge delay path is selected as output A
5	FEDPOL	RO	0x1	Falling-edge delay output polarity 0: Falling-edge delay output is inverted to have active-low polarity 1: Falling-edge delay output keeps the original active-high polarity
4	REDPOL	RO	0x1	Rising-edge delay output polarity 0: Rising-edge delay output is inverted to have active-low polarity

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Bits	Field Name	Type	Reset	Description
				1: Rising-edge delay output keeps the original active-high polarity
3	FEDSRC	RO	0x0	Falling-edge delay source 0: Input A is the source for falling-edge delay 1: Input B is the source for falling-edge delay
2	REDSRC	RO	0x0	Rising-edge delay source 0: Input A is the source for rising-edge delay 1: Input B is the source for rising-edge delay
1	FEDEN	RO	0x0	Falling-edge delay enable 0: Falling-edge delay is bypassed and the input from action-qualifier goes to the submodule directly 1: Falling-edge delay is enabled and applied at output B
0	REDEN	RO	0x0	Rising-edge delay enable 0: Rising-edge delay is bypassed and the input from action-qualifier goes to the submodule directly 1: Rising-edge delay is enabled and applied at output A

10.11.2.32 Dead-Band Generator Rising Edge Delay Register (DBRED)

Table 10-70: Dead-Band Generator Rising Edge Delay Register (DBRED) Layout

DBRED (Dead-Band Generator Rising Edge Delay Register) Offset: 0x7C Default: 0x00000000
Access: PWM -> DBRED.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-71: Dead-Band Generator Rising Edge Delay Register (DBRED) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Rising-edge delay

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10.11.2.33 Dead-Band Generator Rising Edge Delay Active Register (DBREDA)

Table 10-72: Dead-Band Generator Rising Edge Delay Active Register (DBREDA) Layout

DBREDA (Dead-Band Generator Rising Edge Delay Active Register) Offset: 0x80 Default: 0x00000000 Access: PWM -> DBREDA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-73: Dead-Band Generator Rising Edge Delay Active Register (DBREDA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Rising-edge delay

10.11.2.34 Dead-Band Generator Falling Edge Delay Register (DBFED)

Table 10-74: Dead-Band Generator Falling Edge Delay Register (DBFED) Layout

DBFED (Dead-Band Generator Falling Edge Delay Register) Offset: 0x84 Default: 0x00000000 Access: PWM -> DBFED.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-75: Dead-Band Generator Falling Edge Delay Register (DBFED) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Falling-edge delay

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10.11.2.35 Dead-Band Generator Falling Edge Delay Active Register (DBFEDA)

Table 10-76: Dead-Band Generator Falling Edge Delay Active Register (DBFEDA) Layout

DBFEDA (Dead-Band Generator Falling Edge Delay Active Register) Offset: 0x88 Default: 0x00000000 Access: PWM -> DBFEDA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-77: Dead-Band Generator Falling Edge Delay Active Register (DBFEDA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Falling-edge delay

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10.11.2.36 Trip-Zone Event Select Register (TZSEL)

Table 10-78: Trip-Zone Event Select Register (TZSEL) Layout

TZSEL (Trip-Zone Event Select Register) Offset: 0x8C Default: 0x00030003
Access: PWM -> TZSEL.all

31	30	29	28	27	26	25	24
RESERVED					DBGCBC	DCBEVT1	DCAEVT1
23	22	21	20	19	18	17	16
CLKERRCBC	TZ4CBC	TZ3CBC	TZ2CBC	TZ1CBC	TZ0CBC	CBCOUT	
15	14	13	12	11	10	9	8
RESERVED					DBGOST	DCBEVT0	DCAEVT0
7	6	5	4	3	2	1	0
CLKERROST	TZ4OST	TZ3OST	TZ2OST	TZ1OST	TZ0OST	OSTOUT	

Table 10-79: Trip-Zone Event Select Register (TZSEL) Field Description

Bits	Field Name	Type	Reset	Description
31:27	RESERVED_31_27	RO	0x0	Reserved
26	DBGCBC	RW	0x0	Debug (or other reason) caused core lockup or halted event as cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
25	DCBEVT1	RW	0x0	Digital compare B event 1 as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
24	DCAEVT1	RW	0x0	Digital compare A event 1 as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
23	CLKERRCBC	RW	0x0	Clock error as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
22	TZ4CBC	RW	0x0	TZ4 as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
21	TZ3CBC	RW	0x0	TZ3 as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
20	TZ2CBC	RW	0x0	TZ2 as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
19	TZ1CBC	RW	0x0	TZ1 as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable
18	TZ0CBC	RW	0x0	TZ0 as a cycle-by-cycle trip source (Ored) 0: Disable 1: Enable

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Bits	Field Name	Type	Reset	Description
17:16	CBCOUT	RW	0x3	Cycle-by-cycle trip-zone output select 00: Disable cycle-by-cycle trip-zone 01: Select only the asynchronous path. i.e. The original event OR gate output 10: Select only the latched path 11: Select both the asynchronous path and the latched path (Ored)
15:11	RESERVED_15_11	RO	0x0	Reserved
10	DBGOST	RW	0x0	Debug (or other reason) caused core lockup or halted event as a one-shot trip source (Ored) 0: Disable 1: Enable
9	DCBEVT0	RW	0x0	Digital compare B event 0 as a one-shot trip source (Ored) 0: Disable 1: Enable
8	DCAEVT0	RW	0x0	Digital compare A event 0 as a one-shot trip source (Ored) 0: Disable 1: Enable
7	CLKERROST	RW	0x0	Clock error as a one-shot trip source (Ored) 0: Disable 1: Enable
6	TZ4OST	RW	0x0	TZ4 as a one-shot trip source (Ored) 0: Disable 1: Enable
5	TZ3OST	RW	0x0	TZ3 as a one-shot trip source (Ored) 0: Disable 1: Enable
4	TZ2OST	RW	0x0	TZ2 as a one-shot trip source (Ored) 0: Disable 1: Enable
3	TZ1OST	RW	0x0	TZ1 as a one-shot trip source (Ored) 0: Disable 1: Enable
2	TZ0OST	RW	0x0	TZ0 as a one-shot trip source (Ored) 0: Disable 1: Enable
1:0	OSTOUT	RW	0x3	One-shot trip-zone output select 00: Disable one-shot trip-zone 01: Select only the asynchronous path. i.e. The original event OR gate output 10: Select only the latched path 11: Select both the asynchronous path and the latched path (Ored)

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10.11.2.37 Trip-Zone Status Register (TZSTS)

Table 10-80: Trip-Zone Status Register (TZSTS) Layout

TZSTS (Trip-Zone Status Register) Offset: 0x90 Default: 0x00000000 Access: PWM -> TZSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED						DBGCBC	DCBEVT1
15	14	13	12	11	10	9	8
DCAEVT1	CLKERRCBC	TZ4CBC	TZ3CBC	TZ2CBC	TZ1CBC	TZ0CBC	DBGOST
7	6	5	4	3	2	1	0
DCBEVT0	DCAEVT0	CLKERROST	TZ4OST	TZ3OST	TZ2OST	TZ1OST	TZ0OST

Table 10-81: Trip-Zone Status Register (TZSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	DBGCBC	RO	0x0	Latched debug (or other reason) caused core lockup or halted cycle-by-cycle trip event status 0: No event has occurred 1: Event occurred
16	DCBEVT1	RO	0x0	Latched digital compare B event 1 cycle-by-cycle trip status 0: No event has occurred 1: Event occurred
15	DCAEVT1	RO	0x0	Latched digital compare A event 1 cycle-by-cycle trip status 0: No event has occurred 1: Event occurred
14	CLKERRCBC	RO	0x0	Latched clock error cycle-by-cycle trip event status 0: No event has occurred 1: Event occurred
13	TZ4CBC	RO	0x0	Latched TZ4 cycle-by-cycle trip event status 0: No event has occurred 1: Event occurred
12	TZ3CBC	RO	0x0	Latched TZ3 cycle-by-cycle trip event status 0: No event has occurred 1: Event occurred
11	TZ2CBC	RO	0x0	Latched TZ2 cycle-by-cycle trip event status 0: No event has occurred 1: Event occurred
10	TZ1CBC	RO	0x0	Latched TZ1 cycle-by-cycle trip event status

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Bits	Field Name	Type	Reset	Description
				0: No event has occurred 1: Event occurred
9	TZ0CBC	RO	0x0	Latched TZ0 cycle-by-cycle trip event status 0: No event has occurred 1: Event occurred
8	DBGOST	RO	0x0	Latched debug (or other reason) caused core lockup or halted one-shot trip event status 0: No event has occurred 1: Event occurred
7	DCBEVT0	RO	0x0	Latched digital compare B event 0 one-shot trip status 0: No event has occurred 1: Event occurred
6	DCAEVT0	RO	0x0	Latched digital compare A event 0 one-shot trip status 0: No event has occurred 1: Event occurred
5	CLKERROST	RO	0x0	Latched clock error one-shot trip event status 0: No event has occurred 1: Event occurred
4	TZ4OST	RO	0x0	Latched TZ4 one-shot trip event status 0: No event has occurred 1: Event occurred
3	TZ3OST	RO	0x0	Latched TZ3 one-shot trip event status 0: No event has occurred 1: Event occurred
2	TZ2OST	RO	0x0	Latched TZ2 one-shot trip event status 0: No event has occurred 1: Event occurred
1	TZ1OST	RO	0x0	Latched TZ1 one-shot trip event status 0: No event has occurred 1: Event occurred
0	TZ0OST	RO	0x0	Latched TZ0 one-shot trip event status 0: No event has occurred 1: Event occurred

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10.11.2.38 Trip-Zone Status Clear Register (TZSTSCLR)

Table 10-82: Trip-Zone Status Clear Register (TZSTSCLR) Layout

TZSTSCLR (Trip-Zone Status Clear Register) Offset: 0x94 Default: 0x00000000 Access: PWM -> TZSTSCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED						DBGCBC	DCBEVT1
15	14	13	12	11	10	9	8
DCAEVT1	CLKERRCBC	TZ4CBC	TZ3CBC	TZ2CBC	TZ1CBC	TZ0CBC	DBGOST
7	6	5	4	3	2	1	0
DCBEVT0	DCAEVT0	CLKERROST	TZ4OST	TZ3OST	TZ2OST	TZ1OST	TZ0OST

Table 10-83: Trip-Zone Status Clear Register (TZSTSCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	DBGCBC	W1C	0x0	Latched debug (or other reason) caused core lockup or halted cycle-by-cycle trip status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
16	DCBEVT1	W1C	0x0	Latched digital compare B event 1 cycle-by-cycle trip status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
15	DCAEVT1	W1C	0x0	Latched digital compare A event 1 cycle-by-cycle trip status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
14	CLKERRCBC	W1C	0x0	Latched clock error cycle-by-cycle trip status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
13	TZ4CBC	W1C	0x0	Latched TZ4 cycle-by-cycle trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
12	TZ3CBC	W1C	0x0	Latched TZ3 cycle-by-cycle trip event status clear

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Bits	Field Name	Type	Reset	Description
				0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
11	TZ2CBC	W1C	0x0	Latched TZ2 cycle-by-cycle trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
10	TZ1CBC	W1C	0x0	Latched TZ1 cycle-by-cycle trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
9	TZ0CBC	W1C	0x0	Latched TZ0 cycle-by-cycle trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
8	DBGOST	W1C	0x0	Latched debug (or other reason) caused core lockup or halted one-shot trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
7	DCBEVT0	W1C	0x0	Latched digital output B event 0 one-shot trip status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
6	DCAEVT0	W1C	0x0	Latched digital output A event 0 one-shot trip status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
5	CLKERROST	W1C	0x0	Latched clock error one-shot trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
4	TZ4OST	W1C	0x0	Latched TZ4 one-shot trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
3	TZ3OST	W1C	0x0	Latched TZ3 one-shot trip event status clear

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
2	TZ2OST	W1C	0x0	Latched TZ2 one-shot trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
1	TZ1OST	W1C	0x0	Latched TZ1 one-shot trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
0	TZ0OST	W1C	0x0	Latched TZ0 one-shot trip event status clear 0: Write a 0 has no effect. Always reads back a 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0

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10.11.2.39 Trip-Zone Digital Compare Event Select Register (TZDCSEL)

Table 10-84: Trip-Zone Digital Compare Event Select Register (TZDCSEL) Layout

TZDCSEL (Trip-Zone Digital Compare Event Select Register) Offset: 0x98 Default: 0x00000000 Access: PWM -> TZDCSEL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				DCBEVT1			DCBEVT0
7	6	5	4	3	2	1	0
DCBEVT0		DCAEVT1			DCAEVT0		

Table 10-85: Trip-Zone Digital Compare Event Select Register (TZDCSEL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	DCBEVT1	RW	0x0	Digital compare B event 1 option 000: Event disabled 001: DCBL=low, DCBH=don't care 010: DCBL=high, DCBH=don't care 011: DCBL=don't care, DCBH=low 100: DCBL=don't care, DCBH=high 101: DCBL=low, DCBH=high 110: DCBL=high, DCBH=low 111: DCBL=high, DCBH=high
8:6	DCBEVT0	RW	0x0	Digital compare B event 0 option 000: Event disabled 001: DCBL=low, DCBH=don't care 010: DCBL=high, DCBH=don't care 011: DCBL=don't care, DCBH=low 100: DCBL=don't care, DCBH=high 101: DCBL=low, DCBH=high 110: DCBL=high, DCBH=low 111: DCBL=high, DCBH=high
5:3	DCAEVT1	RW	0x0	Digital compare A event 1 option 000: Event disabled 001: DCAL=low, DCAH=don't care 010: DCAL=high, DCAH=don't care 011: DCAL=don't care, DCAH=low 100: DCAL=don't care, DCAH=high 101: DCAL=low, DCAH=high 110: DCAL=high, DCAH=low 111: DCAL=high, DCAH=high

SPINTROL

Bits	Field Name	Type	Reset	Description
2:0	DCAEVT0	RW	0x0	Digital compare A event 0 option 000: Event disabled 001: DCAL=low, DCAH=don't care 010: DCAL=high, DCAH=don't care 011: DCAL=don't care, DCAH=low 100: DCAL=don't care, DCAH=high 101: DCAL=low, DCAH=high 110: DCAL=high, DCAH=low 111: DCAL=high, DCAH=high

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10.11.2.40 Trip-Zone Output A Control Register (TZACTL)

Table 10-86: Trip-Zone Output A Control Register (TZACTL) Layout

TZACTL (Trip-Zone Output A Control Register) Offset: 0x9C Default: 0x00000000
Access: PWM -> TZACTL.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED						DCAEVT1D	
15	14	13	12	11	10	9	8
DCAEVT1D	DCAEVT1U			DCAEVT0D			DCAEVT0U
7	6	5	4	3	2	1	0
DCAEVT0U		TZAD			TZAU		

Table 10-87: Trip-Zone Output A Control Register (TZACTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17:15	DCAEVT1D	RW	0x0	Action on output A when a digital compare A event 1 occurs and TBCNT is counting down 000: Set output A to high-impedance 001: Force output A to low state 010: Force output A to high state 011: Force output A to invert current state (high->low, low->high) 1xx: Do nothing for output A
14:12	DCAEVT1U	RW	0x0	Action on output A when a digital compare A event 1 occurs and TBCNT is counting up 000: Set output A to high-impedance 001: Force output A to low state 010: Force output A to high state 011: Force output A to invert current state (high->low, low->high) 1xx: Do nothing for output A
11:9	DCAEVT0D	RW	0x0	Action on output A when a digital compare A event 0 occurs and TBCNT is counting down 000: Set output A to high-impedance 001: Force output A to low state 010: Force output A to high state 011: Force output A to invert current state (high->low, low->high) 1xx: Do nothing for output A

SPINTROL

Bits	Field Name	Type	Reset	Description
8:6	DCAEVT0U	RW	0x0	Action on output A when a digital compare A event 0 occurs and TBCNT is counting up 000: Set output A to high-impedance 001: Force output A to low state 010: Force output A to high state 011: Force output A to invert current state (high->low, low->high) 1xx: Do nothing for output A
5:3	TZAD	RW	0x0	Action on output A when a trip event occurs and TBCNT is counting down 000: Set output A to high-impedance 001: Force output A to low state 010: Force output A to high state 011: Force output A to invert current state (high->low, low->high) 1xx: Do nothing for output A
2:0	TZAU	RW	0x0	Action on output A when a trip event occurs and TBCNT is counting up 000: Set output A to high-impedance 001: Force output A to low state 010: Force output A to high state 011: Force output A to invert current state (high->low, low->high) 1xx: Do nothing for output A

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10.11.2.41 Trip-Zone Output B Control Register (TZBCTL)

Table 10-88: Trip-Zone Output B Control Register (TZBCTL) Layout

TZBCTL (Trip-Zone Ouput B Control Register) Offset: 0xA0 Default: 0x00000000
Access: PWM -> TZBCTL.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED						DCBEVT1D	
15	14	13	12	11	10	9	8
DCBEVT1D	DCBEVT1U			DCBEVT0D			DCBEVT0U
7	6	5	4	3	2	1	0
DCBEVT0U		TZBD			TZBU		

Table 10-89: Trip-Zone Output B Control Register (TZBCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17:15	DCBEVT1D	RW	0x0	Action on Output B when a digital compare B event 1 occurs and TBCNT is counting down 000: Set Output B to high-impedance 001: Force Output B to low state 010: Force Output B to high state 011: Force Output B to invert current state (high->low, low->high) 1xx: Do nothing for Output B
14:12	DCBEVT1U	RW	0x0	Action on Output B when a digital compare B event 1 occurs and TBCNT is counting up 000: Set Output B to high-impedance 001: Force Output B to low state 010: Force Output B to high state 011: Force Output B to invert current state (high->low, low->high) 1xx: Do nothing for Output B
11:9	DCBEVT0D	RW	0x0	Action on Output B when a digital compare B event 0 occurs and TBCNT is counting down 000: Set Output B to high-impedance 001: Force Output B to low state 010: Force Output B to high state 011: Force Output B to invert current state (high->low, low->high) 1xx: Do nothing for Output B

SPINTROL

Bits	Field Name	Type	Reset	Description
8:6	DCBEVT0U	RW	0x0	Action on Output B when a digital compare B event 0 occurs and TBCNT is counting up 000: Set Output B to high-impedance 001: Force Output B to low state 010: Force Output B to high state 011: Force Output B to invert current state (high->low, low->high) 1xx: Do nothing for Output B
5:3	TZBD	RW	0x0	Action on Output B when a trip event occurs and TBCNT is counting down 000: Set Output B to high-impedance 001: Force Output B to low state 010: Force Output B to high state 011: Force Output B to invert current state (high->low, low->high) 1xx: Do nothing for Output B
2:0	TZBU	RW	0x0	Action on Output B when a trip event occurs and TBCNT is counting up 000: Set Output B to high-impedance 001: Force Output B to low state 010: Force Output B to high state 011: Force Output B to invert current state (high->low, low->high) 1xx: Do nothing for Output B

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10.11.2.42 Trip-Zone Flag Register (TZIF)

Table 10-90: Trip-Zone Flag Register (TZIF) Layout

TZIF (Trip-Zone Flag Register) Offset: 0xA4 Default: 0x00000000 Access: PWM -> TZIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	INT	DCBEVT1	DCBEVT0	DCAEVT1	DCAEVT0	CBC	OST

Table 10-91: Trip-Zone Flag Register (TZIF) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	INT	RO	0x0	Latched trip interrupt status flag 0: Trip-zone interrupt does not occur. 1: Trip-zone interrupt occurred. Further trip-zone interrupt will not be generated until this flag is cleared
5	DCBEVT1	RO	0x0	Latched digital compare B event 1 status flag 0: DCBEVT1 does not occur. 1: DCBEVT1 occurred.
4	DCBEVT0	RO	0x0	Latched digital compare B event 0 status flag 0: DCBEVT0 does not occur 1: DCBEVT0 occurred.
3	DCAEVT1	RO	0x0	Latched digital compare A event 1 status flag 0: DCAEVT1 did not occur 1: DCAEVT1 occurred.
2	DCAEVT0	RO	0x0	Latched digital compare A event 0 status flag 0: DCAEVT0 did not occur 1: DCAEVT0 occurred.
1	CBC	RO	0x0	Latched cycle-by-cycle trip event status flag 0: No cycle-by-cycle trip event has occurred. 1: A cycle-by-cycle trip event occurred.
0	OST	RO	0x0	Latched one-shot trip event status flag 0: No one-shot trip event has occurred. 1: A one-shot trip event occurred.

SPINTROL

10.11.2.43 Trip-Zone Clear Register (TZIC)

Table 10-92: Trip-Zone Clear Register (TZIC) Layout

TZIC (Trip-Zone Clear Register) Offset: 0xA8 Default: 0x00000000 Access: PWM -> TZIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							CBCCLRMODE
7	6	5	4	3	2	1	0
CBCCLRMODE	INT	DCBEVT1	DCBEVT0	DCAEVT1	DCAEVT0	CBC	OST

Table 10-93: Trip-Zone Clear Register (TZIC) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8:7	CBCCLRMODE	RW	0x0	Latched CBC trip status clear mode 00: Clear CBC trip on TBCNT=0 01: Clear CBC trip on TBCNT=TBPRD 10: Clear CBC trip on TBCNT=0 or TBCNT=TBPRD 11: Clear disabled. i.e. Never clear the CBC trip
6	INT	W1C	0x0	Clear global interrupt status flag 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 clears TZIF.INT and TZ interrupt. This bit is self-cleared to 0.
5	DCBEVT1	W1C	0x0	Clear digital compare B event 1 status flag 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 clears TZIF.DCBEVT1. This bit is self-cleared to 0.
4	DCBEVT0	W1C	0x0	Clear digital compare B event 0 status flag 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 clears TZIF.DCBEVT0. This bit is self-cleared to 0.
3	DCAEVT1	W1C	0x0	Clear digital compare A event 1 status flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears TZIF.DCAEVT1. This bit is self-cleared to 0.
2	DCAEVT0	W1C	0x0	Clear digital compare A event 0 status flag 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 clears TZIF.DCAEVT0. This bit is self-cleared to 0.

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Bits	Field Name	Type	Reset	Description
1	CBC	W1C	0x0	Clear cycle-by-cycle trip status flag 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 clears TZIF.CBC. This bit is self-cleared to 0.
0	OST	W1C	0x0	Clear one-shot trip status flag 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 clears TZIF.OST. This bit is self-cleared to 0.

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10.11.2.44 Trip-Zone Interrupt Enable Register (TZIE)

Table 10-94: Trip-Zone Interrupt Enable Register (TZIE) Layout

TZIE (Trip-Zone Interrupt Enable Register) Offset: 0xAC Default: 0x00000000 Access: PWM -> TZIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		DCBEVT1	DCBEVT0	DCAEVT1	DCAEVT0	CBC	OST

Table 10-95: Trip-Zone Interrupt Enable Register (TZIE) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	DCBEVT1	RW	0x0	Digital compare B event 1 interrupt enable 0: Disable 1: Enable
4	DCBEVT0	RW	0x0	Digital compare B event 0 interrupt enable 0: Disable 1: Enable
3	DCAEVT1	RW	0x0	Digital compare A event 1 interrupt enable 0: Disable 1: Enable
2	DCAEVT0	RW	0x0	Digital compare A event 0 interrupt enable 0: Disable 1: Enable
1	CBC	RW	0x0	Cycle-by-cycle trip-zone interrupt enable 0: Disable 1: Enable
0	OST	RW	0x0	One-shot trip-zone interrupt enable 0: Disable 1: Enable

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10.11.2.45 Trip-Zone Force Register (TZFRC)

Table 10-96: Trip-Zone Force Register (TZFRC) Layout

TZFRC (Trip-Zone Force Register) Offset: 0xB0 Default: 0x00000000 Access: PWM -> TZFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		DCBEVT1	DCBEVT0	DCAEVT1	DCAEVT0	CBC	OST

Table 10-97: Trip-Zone Force Register (TZFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	DCBEVT1	W1S	0x0	Software force a digital compare B event 1 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 forces a digital compare B event 1 and sets TZIF.DCBEVT1.This bit is self-cleared to 0.
4	DCBEVT0	W1S	0x0	Software force a digital compare B event 0 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 forces a digital compare B event 0 and sets TZIF.DCBEVT0.This bit is self-cleared to 0.
3	DCAEVT1	W1S	0x0	Software force a digital compare A event 1 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 forces a digital compare A event 1 and sets TZIF.DCAEVT1.This bit is self-cleared to 0.
2	DCAEVT0	W1S	0x0	Software force a digital compare A event 0 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 forces a digital compare A event 0 and sets TZIF.DCAEVT0.This bit is self-cleared to 0.
1	CBC	W1S	0x0	Software force a cycle-by-cycle trip event 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 forces a cycle-by-cycle trip event and sets TZIF.CBC.This bit is self-cleared to 0.
0	OST	W1S	0x0	Software force a one-shot trip event 0: Write a 0 has no effect. Always reads back 0. 1: Write a 1 forces a one-shot trip event and sets TZIF.OST.This bit is self-cleared to 0.

SPINTROL

10.11.2.46 Digital Compare AL Trip Select Register (DCALTRIPSEL)

Table 10-98: Digital Compare AL Trip Select Register (DCALTRIPSEL) Layout

DCALTRIPSEL (Digital Compare AL Trip Select Register) Offset: 0xB4 Default: 0x00000000 Access: PWM -> DCALTRIPSEL.all							
31	30	29	28	27	26	25	24
COMP7H	COMP7L	COMP6H	COMP6L	COMP5H	COMP5L	COMP4H	COMP4L
23	22	21	20	19	18	17	16
COMP3H	COMP3L	COMP2H	COMP2L	COMP1H	COMP1L	COMP0H	COMP0L
15	14	13	12	11	10	9	8
ADCPPU7TZ	ADCPPU6TZ	ADCPPU5TZ	ADCPPU4TZ	ADCPPU3TZ	ADCPPU2TZ	ADCPPU1TZ	ADCPPU0TZ
7	6	5	4	3	2	1	0
RESERVED			TZ4	TZ3	TZ2	TZ1	TZ0

Table 10-99: Digital Compare AL Trip Select Register (DCALTRIPSEL) Field Description

Bits	Field Name	Type	Reset	Description
31	COMP7H	RW	0x0	Enable COMP7H as DCAL trip event (Ored) 0: Disable 1: Enable
30	COMP7L	RW	0x0	Enable COMP7L as DCAL trip event (Ored) 0: Disable 1: Enable
29	COMP6H	RW	0x0	Enable COMP6H as DCAL trip event (Ored) 0: Disable 1: Enable
28	COMP6L	RW	0x0	Enable COMP6L as DCAL trip event (Ored) 0: Disable 1: Enable
27	COMP5H	RW	0x0	Enable COMP5H as DCAL trip event (Ored) 0: Disable 1: Enable
26	COMP5L	RW	0x0	Enable COMP5L as DCAL trip event (Ored) 0: Disable 1: Enable
25	COMP4H	RW	0x0	Enable COMP4H as DCAL trip event (Ored) 0: Disable 1: Enable
24	COMP4L	RW	0x0	Enable COMP4L as DCAL trip event (Ored) 0: Disable 1: Enable

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Bits	Field Name	Type	Reset	Description
23	COMP3H	RW	0x0	Enable COMP3H as DCAL trip event (Ored) 0: Disable 1: Enable
22	COMP3L	RW	0x0	Enable COMP3L as DCAL trip event (Ored) 0: Disable 1: Enable
21	COMP2H	RW	0x0	Enable COMP2H as DCAL trip event (Ored) 0: Disable 1: Enable
20	COMP2L	RW	0x0	Enable COMP2L as DCAL trip event (Ored) 0: Disable 1: Enable
19	COMP1H	RW	0x0	Enable COMP1H as DCAL trip event (Ored) 0: Disable 1: Enable
18	COMP1L	RW	0x0	Enable COMP1L as DCAL trip event (Ored) 0: Disable 1: Enable
17	COMP0H	RW	0x0	Enable COMP0H as DCAL trip event (Ored) 0: Disable 1: Enable
16	COMP0L	RW	0x0	Enable COMP0L as DCAL trip event (Ored) 0: Disable 1: Enable
15	ADCPPU7TZ	RW	0x0	Enable ADCPPU7TZ as DCAL trip event (Ored) 0: Disable 1: Enable
14	ADCPPU6TZ	RW	0x0	Enable ADCPPU6TZ as DCAL trip event (Ored) 0: Disable 1: Enable
13	ADCPPU5TZ	RW	0x0	Enable ADCPPU5TZ as DCAL trip event (Ored) 0: Disable 1: Enable
12	ADCPPU4TZ	RW	0x0	Enable ADCPPU4TZ as DCAL trip event (Ored) 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
11	ADCPPU3TZ	RW	0x0	Enable ADCPPU3TZ as DCAL trip event (Ored) 0: Disable 1: Enable
10	ADCPPU2TZ	RW	0x0	Enable ADCPPU2TZ as DCAL trip event (Ored) 0: Disable 1: Enable
9	ADCPPU1TZ	RW	0x0	Enable ADCPPU1TZ as DCAL trip event (Ored) 0: Disable 1: Enable
8	ADCPPU0TZ	RW	0x0	Enable ADCPPU0TZ as DCAL trip event (Ored) 0: Disable 1: Enable
7:5	RESERVED_7_5	RO	0x0	Reserved
4	TZ4	RW	0x0	Enable TZ4 as DCAL trip event (Ored) 0: Disable 1: Enable
3	TZ3	RW	0x0	Enable TZ3 as DCAL trip event (Ored) 0: Disable 1: Enable
2	TZ2	RW	0x0	Enable TZ2 as DCAL trip event (Ored) 0: Disable 1: Enable
1	TZ1	RW	0x0	Enable TZ1 as DCAL trip event (Ored) 0: Disable 1: Enable
0	TZ0	RW	0x0	Enable TZ0 as DCAL trip event (Ored) 0: Disable 1: Enable

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10.11.2.47 Digital Compare AH Trip Select Register (DCAHTRIPSEL)

Table 10-100: Digital Compare AH Trip Select Register (DCAHTRIPSEL) Layout

DCAHTRIPSEL (Digital Compare AH Trip Select Register) Offset: 0xB8 Default: 0x00000000 Access: PWM -> DCAHTRIPSEL.all							
31	30	29	28	27	26	25	24
COMP7H	COMP7L	COMP6H	COMP6L	COMP5H	COMP5L	COMP4H	COMP4L
23	22	21	20	19	18	17	16
COMP3H	COMP3L	COMP2H	COMP2L	COMP1H	COMP1L	COMP0H	COMP0L
15	14	13	12	11	10	9	8
ADCPPU7TZ	ADCPPU6TZ	ADCPPU5TZ	ADCPPU4TZ	ADCPPU3TZ	ADCPPU2TZ	ADCPPU1TZ	ADCPPU0TZ
7	6	5	4	3	2	1	0
RESERVED			TZ4	TZ3	TZ2	TZ1	TZ0

Table 10-101: Digital Compare AH Trip Select Register (DCAHTRIPSEL) Field Description

Bits	Field Name	Type	Reset	Description
31	COMP7H	RW	0x0	Enable COMP7H as DCAH trip event (Ored) 0: Disable 1: Enable
30	COMP7L	RW	0x0	Enable COMP7L as DCAH trip event (Ored) 0: Disable 1: Enable
29	COMP6H	RW	0x0	Enable COMP6H as DCAH trip event (Ored) 0: Disable 1: Enable
28	COMP6L	RW	0x0	Enable COMP6L as DCAH trip event (Ored) 0: Disable 1: Enable
27	COMP5H	RW	0x0	Enable COMP5H as DCAH trip event (Ored) 0: Disable 1: Enable
26	COMP5L	RW	0x0	Enable COMP5L as DCAH trip event (Ored) 0: Disable 1: Enable
25	COMP4H	RW	0x0	Enable COMP4H as DCAH trip event (Ored) 0: Disable 1: Enable
24	COMP4L	RW	0x0	Enable COMP4L as DCAH trip event (Ored) 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
23	COMP3H	RW	0x0	Enable COMP3H as DCAH trip event (Ored) 0: Disable 1: Enable
22	COMP3L	RW	0x0	Enable COMP3L as DCAH trip event (Ored) 0: Disable 1: Enable
21	COMP2H	RW	0x0	Enable COMP2H as DCAH trip event (Ored) 0: Disable 1: Enable
20	COMP2L	RW	0x0	Enable COMP2L as DCAH trip event (Ored) 0: Disable 1: Enable
19	COMP1H	RW	0x0	Enable COMP1H as DCAH trip event (Ored) 0: Disable 1: Enable
18	COMP1L	RW	0x0	Enable COMP1L as DCAH trip event (Ored) 0: Disable 1: Enable
17	COMP0H	RW	0x0	Enable COMP0H as DCAH trip event (Ored) 0: Disable 1: Enable
16	COMP0L	RW	0x0	Enable COMP0L as DCAH trip event (Ored) 0: Disable 1: Enable
15	ADCPPU7TZ	RW	0x0	Enable ADCPPU7TZ as DCAH trip event (Ored) 0: Disable 1: Enable
14	ADCPPU6TZ	RW	0x0	Enable ADCPPU6TZ as DCAH trip event (Ored) 0: Disable 1: Enable
13	ADCPPU5TZ	RW	0x0	Enable ADCPPU5TZ as DCAH trip event (Ored) 0: Disable 1: Enable
12	ADCPPU4TZ	RW	0x0	Enable ADCPPU4TZ as DCAH trip event (Ored) 0: Disable 1: Enable

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Bits	Field Name	Type	Reset	Description
11	ADCPPU3TZ	RW	0x0	Enable ADCPPU3TZ as DCAH trip event (Ored) 0: Disable 1: Enable
10	ADCPPU2TZ	RW	0x0	Enable ADCPPU2TZ as DCAH trip event (Ored) 0: Disable 1: Enable
9	ADCPPU1TZ	RW	0x0	Enable ADCPPU1TZ as DCAH trip event (Ored) 0: Disable 1: Enable
8	ADCPPU0TZ	RW	0x0	Enable ADCPPU0TZ as DCAH trip event (Ored) 0: Disable 1: Enable
7:5	RESERVED_7_5	RO	0x0	Reserved
4	TZ4	RW	0x0	Enable TZ4 as DCAH trip event (Ored) 0: Disable 1: Enable
3	TZ3	RW	0x0	Enable TZ3 as DCAH trip event (Ored) 0: Disable 1: Enable
2	TZ2	RW	0x0	Enable TZ2 as DCAH trip event (Ored) 0: Disable 1: Enable
1	TZ1	RW	0x0	Enable TZ1 as DCAH trip event (Ored) 0: Disable 1: Enable
0	TZ0	RW	0x0	Enable TZ0 as DCAH trip event (Ored) 0: Disable 1: Enable

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10.11.2.48 Digital Compare BL Trip Select Register (DCBLTRIPSEL)

Table 10-102: Digital Compare BL Trip Select Register (DCBLTRIPSEL) Layout

DCBLTRIPSEL (Digital Compare BL Trip Select Register) Offset: 0xBC Default: 0x00000000 Access: PWM -> DCBLTRIPSEL.all							
31	30	29	28	27	26	25	24
COMP7H	COMP7L	COMP6H	COMP6L	COMP5H	COMP5L	COMP4H	COMP4L
23	22	21	20	19	18	17	16
COMP3H	COMP3L	COMP2H	COMP2L	COMP1H	COMP1L	COMP0H	COMP0L
15	14	13	12	11	10	9	8
ADCPPU7TZ	ADCPPU6TZ	ADCPPU5TZ	ADCPPU4TZ	ADCPPU3TZ	ADCPPU2TZ	ADCPPU1TZ	ADCPPU0TZ
7	6	5	4	3	2	1	0
RESERVED			TZ4	TZ3	TZ2	TZ1	TZ0

Table 10-103: Digital Compare BL Trip Select Register (DCBLTRIPSEL) Field Description

Bits	Field Name	Type	Reset	Description
31	COMP7H	RW	0x0	Enable COMP7H as DCBL trip event (Ored) 0: Disable 1: Enable
30	COMP7L	RW	0x0	Enable COMP7L as DCBL trip event (Ored) 0: Disable 1: Enable
29	COMP6H	RW	0x0	Enable COMP6H as DCBL trip event (Ored) 0: Disable 1: Enable
28	COMP6L	RW	0x0	Enable COMP6L as DCBL trip event (Ored) 0: Disable 1: Enable
27	COMP5H	RW	0x0	Enable COMP5H as DCBL trip event (Ored) 0: Disable 1: Enable
26	COMP5L	RW	0x0	Enable COMP5L as DCBL trip event (Ored) 0: Disable 1: Enable
25	COMP4H	RW	0x0	Enable COMP4H as DCBL trip event (Ored) 0: Disable 1: Enable
24	COMP4L	RW	0x0	Enable COMP4L as DCBL trip event (Ored) 0: Disable 1: Enable
23	COMP3H	RW	0x0	Enable COMP3H as DCBL trip event (Ored)

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Bits	Field Name	Type	Reset	Description
				0: Disable 1: Enable
22	COMP3L	RW	0x0	Enable COMP3L as DCBL trip event (Ored) 0: Disable 1: Enable
21	COMP2H	RW	0x0	Enable COMP2H as DCBL trip event (Ored) 0: Disable 1: Enable
20	COMP2L	RW	0x0	Enable COMP2L as DCBL trip event (Ored) 0: Disable 1: Enable
19	COMP1H	RW	0x0	Enable COMP1H as DCBL trip event (Ored) 0: Disable 1: Enable
18	COMP1L	RW	0x0	Enable COMP1L as DCBL trip event (Ored) 0: Disable 1: Enable
17	COMP0H	RW	0x0	Enable COMP0H as DCBL trip event (Ored) 0: Disable 1: Enable
16	COMP0L	RW	0x0	Enable COMP0L as DCBL trip event (Ored) 0: Disable 1: Enable
15	ADCPPU7TZ	RW	0x0	Enable ADCPPU7TZ as DCBL trip event (Ored) 0: Disable 1: Enable
14	ADCPPU6TZ	RW	0x0	Enable ADCPPU6TZ as DCBL trip event (Ored) 0: Disable 1: Enable
13	ADCPPU5TZ	RW	0x0	Enable ADCPPU5TZ as DCBL trip event (Ored) 0: Disable 1: Enable
12	ADCPPU4TZ	RW	0x0	Enable ADCPPU4TZ as DCBL trip event (Ored) 0: Disable 1: Enable
11	ADCPPU3TZ	RW	0x0	Enable ADCPPU3TZ as DCBL trip event (Ored) 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
10	ADCPPU2TZ	RW	0x0	Enable ADCPPU2TZ as DCBL trip event (Ored) 0: Disable 1: Enable
9	ADCPPU1TZ	RW	0x0	Enable ADCPPU1TZ as DCBL trip event (Ored) 0: Disable 1: Enable
8	ADCPPU0TZ	RW	0x0	Enable ADCPPU0TZ as DCBL trip event (Ored) 0: Disable 1: Enable
7:5	RESERVED_7_5	RO	0x0	Reserved
4	TZ4	RW	0x0	Enable TZ4 as DCBL trip event (Ored) 0: Disable 1: Enable
3	TZ3	RW	0x0	Enable TZ3 as DCBL trip event (Ored) 0: Disable 1: Enable
2	TZ2	RW	0x0	Enable TZ2 as DCBL trip event (Ored) 0: Disable 1: Enable
1	TZ1	RW	0x0	Enable TZ1 as DCBL trip event (Ored) 0: Disable 1: Enable
0	TZ0	RW	0x0	Enable TZ0 as DCBL trip event (Ored) 0: Disable 1: Enable

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10.11.2.49 Digital Compare BH Trip Select Register (DCBHTRIPSEL)

Table 10-104: Digital Compare BH Trip Select Register (DCBHTRIPSEL) Layout

DCBHTRIPSEL (Digital Compare BH Trip Select Register) Offset: 0xC0 Default: 0x00000000 Access: PWM -> DCBHTRIPSEL.all							
31	30	29	28	27	26	25	24
COMP7H	COMP7L	COMP6H	COMP6L	COMP5H	COMP5L	COMP4H	COMP4L
23	22	21	20	19	18	17	16
COMP3H	COMP3L	COMP2H	COMP2L	COMP1H	COMP1L	COMP0H	COMP0L
15	14	13	12	11	10	9	8
ADCPPU7TZ	ADCPPU6TZ	ADCPPU5TZ	ADCPPU4TZ	ADCPPU3TZ	ADCPPU2TZ	ADCPPU1TZ	ADCPPU0TZ
7	6	5	4	3	2	1	0
RESERVED			TZ4	TZ3	TZ2	TZ1	TZ0

Table 10-105: Digital Compare BH Trip Select Register (DCBHTRIPSEL) Field Description

Bits	Field Name	Type	Reset	Description
31	COMP7H	RW	0x0	Enable COMP7H as DCBH trip event (Ored) 0: Disable 1: Enable
30	COMP7L	RW	0x0	Enable COMP7L as DCBH trip event (Ored) 0: Disable 1: Enable
29	COMP6H	RW	0x0	Enable COMP6H as DCBH trip event (Ored) 0: Disable 1: Enable
28	COMP6L	RW	0x0	Enable COMP6L as DCBH trip event (Ored) 0: Disable 1: Enable
27	COMP5H	RW	0x0	Enable COMP5H as DCBH trip event (Ored) 0: Disable 1: Enable
26	COMP5L	RW	0x0	Enable COMP5L as DCBH trip event (Ored) 0: Disable 1: Enable
25	COMP4H	RW	0x0	Enable COMP4H as DCBH trip event (Ored) 0: Disable 1: Enable
24	COMP4L	RW	0x0	Enable COMP4L as DCBH trip event (Ored) 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
23	COMP3H	RW	0x0	Enable COMP3H as DCBH trip event (Ored) 0: Disable 1: Enable
22	COMP3L	RW	0x0	Enable COMP3L as DCBH trip event (Ored) 0: Disable 1: Enable
21	COMP2H	RW	0x0	Enable COMP2H as DCBH trip event (Ored) 0: Disable 1: Enable
20	COMP2L	RW	0x0	Enable COMP2L as DCBH trip event (Ored) 0: Disable 1: Enable
19	COMP1H	RW	0x0	Enable COMP1H as DCBH trip event (Ored) 0: Disable 1: Enable
18	COMP1L	RW	0x0	Enable COMP1L as DCBH trip event (Ored) 0: Disable 1: Enable
17	COMP0H	RW	0x0	Enable COMP0H as DCBH trip event (Ored) 0: Disable 1: Enable
16	COMP0L	RW	0x0	Enable COMP0L as DCBH trip event (Ored) 0: Disable 1: Enable
15	ADCPPU7TZ	RW	0x0	Enable ADCPPU7TZ as DCBH trip event (Ored) 0: Disable 1: Enable
14	ADCPPU6TZ	RW	0x0	Enable ADCPPU6TZ as DCBH trip event (Ored) 0: Disable 1: Enable
13	ADCPPU5TZ	RW	0x0	Enable ADCPPU5TZ as DCBH trip event (Ored) 0: Disable 1: Enable
12	ADCPPU4TZ	RW	0x0	Enable ADCPPU4TZ as DCBH trip event (Ored) 0: Disable 1: Enable

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Bits	Field Name	Type	Reset	Description
11	ADCPPU3TZ	RW	0x0	Enable ADCPPU3TZ as DCBH trip event (Ored) 0: Disable 1: Enable
10	ADCPPU2TZ	RW	0x0	Enable ADCPPU2TZ as DCBH trip event (Ored) 0: Disable 1: Enable
9	ADCPPU1TZ	RW	0x0	Enable ADCPPU1TZ as DCBH trip event (Ored) 0: Disable 1: Enable
8	ADCPPU0TZ	RW	0x0	Enable ADCPPU0TZ as DCBH trip event (Ored) 0: Disable 1: Enable
7:5	RESERVED_7_5	RO	0x0	Reserved
4	TZ4	RW	0x0	Enable TZ4 as DCBH trip event (Ored) 0: Disable 1: Enable
3	TZ3	RW	0x0	Enable TZ3 as DCBH trip event (Ored) 0: Disable 1: Enable
2	TZ2	RW	0x0	Enable TZ2 as DCBH trip event (Ored) 0: Disable 1: Enable
1	TZ1	RW	0x0	Enable TZ1 as DCBH trip event (Ored) 0: Disable 1: Enable
0	TZ0	RW	0x0	Enable TZ0 as DCBH trip event (Ored) 0: Disable 1: Enable

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10.11.2.50 Digital Compare A Control Register (DCACTL)

Table 10-106: Digital Compare A Control Register (DCACTL) Layout

DCACTL (Digital Compare A Control Register) Offset: 0xC4 Default: 0x00000000 Access: PWM -> DCACTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		EVT1SRCASYNC	EVT1SRCSEL	EVT0SYNCE	EVT0SOCE	EVT0SRCASYNC	EVT0SRCSEL

Table 10-107: Digital Compare A Control Register (DCACTL) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	EVT1SRCASYNC	RW	0x0	DCAEVT1 source signal is asynchronous/synchronous (1/0) 0: Synchronous 1: Asynchronous
4	EVT1SRCSEL	RW	0x0	DCAEVT1 source signal select 0: Source signal is DCAEVT1 1: Source signal is DCEVTFILT
3	EVT0SYNCE	RW	0x0	DCAEVT0 SYNC generation 0: Disable 1: Enable
2	EVT0SOCE	RW	0x0	DCAEVT0 SOC generation 0: Disable 1: Enable
1	EVT0SRCASYNC	RW	0x0	DCAEVT0 source signal is asynchronous/synchronous (1/0) 0: Synchronous 1: Asynchronous
0	EVT0SRCSEL	RW	0x0	DCAEVT0 source signal select 0: Source signal is DCAEVT0 1: Source signal is DCEVTFILT

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10.11.2.51 Digital Compare B Control Register (DCBCTL)

Table 10-108: Digital Compare B Control Register (DCBCTL) Layout

DCBCTL (Digital Compare B Control Register) Offset: 0xC8 Default: 0x00000000 Access: PWM -> DCBCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		EVT1SRCASYNC	EVT1SRCSEL	EVT0SYNCE	EVT0SOCE	EVT0SRCASYNC	EVT0SRCSEL

Table 10-109: Digital Compare B Control Register (DCBCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	EVT1SRCASYNC	RW	0x0	DCBEVT1 source signal is asynchronous/synchronous (1/0) 0: Synchronous 1: Asynchronous
4	EVT1SRCSEL	RW	0x0	DCBEVT1 source signal select 0: Source signal is DCBEVT1 1: Source signal is DCEVTFILT
3	EVT0SYNCE	RW	0x0	DCBEVT0 SYNC generation 0: Disable 1: Enable
2	EVT0SOCE	RW	0x0	DCBEVT0 SOC generation 0: Disable 1: Enable
1	EVT0SRCASYNC	RW	0x0	DCBEVT0 source signal is asynchronous/synchronous (1/0) 0: Synchronous 1: Asynchronous
0	EVT0SRCSEL	RW	0x0	DCBEVT0 source signal select 0: Source signal is DCBEVT0 1: Source signal is DCEVTFILT

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10.11.2.52 Digital Compare Filter Register (DCFCTL)

Table 10-110: Digital Compare Filter Register (DCFCTL) Layout

DCFCTL (Digital Compare Filter Register) Offset: 0xCC Default: 0x00000010 Access: PWM -> DCFCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED		WIN7EN	WIN6EN	WIN5EN	WIN4EN	WIN3EN	WIN2EN
7	6	5	4	3	2	1	0
WIN1EN	WIN0EN	PULSESEL		BLANKINV	BLANKEN	SRCSEL	

Table 10-111: Digital Compare Filter Register (DCFCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:14	RESERVED_31_14	RO	0x0	Reserved
13	WIN7EN	RW	0x0	Enable blank window from PWM7 (Ored) 0: Disable 1: Enable
12	WIN6EN	RW	0x0	Enable blank window from PWM6 (Ored) 0: Disable 1: Enable
11	WIN5EN	RW	0x0	Enable blank window from PWM5 (Ored) 0: Disable 1: Enable
10	WIN4EN	RW	0x0	Enable blank window from PWM4 (Ored) 0: Disable 1: Enable
9	WIN3EN	RW	0x0	Enable blank window from PWM3 (Ored) 0: Disable 1: Enable
8	WIN2EN	RW	0x0	Enable blank window from PWM2 (Ored) 0: Disable 1: Enable
7	WIN1EN	RW	0x0	Enable blank window from PWM1 (Ored) 0: Disable 1: Enable
6	WIN0EN	RW	0x0	Enable blank window from PWM0 (Ored) 0: Disable 1: Enable

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Bits	Field Name	Type	Reset	Description
5:4	PULSESEL	RW	0x1	Pulse select for blanking and capture alignment for this module 00: Align on TBCNT=0 01: Align on TBCNT=TBPRD 10: Align on TBCNT=0 or TBCNT=TBPRD 11: Reserved
3	BLANKINV	RW	0x0	Blanking window inversion 0: Disable 1: Enable
2	BLANKEN	RW	0x0	Blanking window 0: Disable 1: Enable
1:0	SRCSEL	RW	0x0	DCEVTFILT signal source select 00: Source is DCAEVT0 01: Source is DCAEVT1 10: Source is DCBEVT0 11: Source is DCBEVT1

10.11.2.53 Digital Compare Filter Offset Register (DCFOFFSET)

Table 10-112: Digital Compare Filter Offset Register (DCFOFFSET) Layout

DCFOFFSET (Digital Compare Filter Offset Register) Offset: 0xD0 Default: 0x00000000
Access: PWM -> DCFOFFSET.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-113: Digital Compare Filter Offset Register (DCFOFFSET) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Blanking window offset It defines the number of TBCLK cycles from the blanking window reference specified by DCFCTL.PULSESEL to the point when the blanking window is applied.

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10.11.2.54 Digital Compare Filter Offset Counter Register (DCFOFFSETCNT)

Table 10-114: Digital Compare Filter Offset Counter Register (DCFOFFSETCNT) Layout

DCFOFFSETCNT (Digital Compare Filter Offset Counter Register) Offset: 0xD4 Default: 0x00000000 Access: PWM -> DCFOFFSETCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-115: Digital Compare Filter Offset Counter Register (DCFOFFSETCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Blanking offset counter It is read only and indicates the current value of the offset counter. The counter counts down to zero and then stops until it is re-loaded on the next event defined by DCFCTL.PULSESEL.

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10.11.2.55 Digital Compare Filter Window Register (DCFWINDOW)

Table 10-116: Digital Compare Filter Window Register (DCFWINDOW) Layout

DCFWINDOW (Digital Compare Filter Window Register) Offset: 0xD8 Default: 0x00000000 Access: PWM -> DCFWINDOW.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-117: Digital Compare Filter Window Register (DCFWINDOW) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Blanking window width in TBCLK cycles The blanking window begins when the offset counter expires. When this occurs, the window counter is loaded and begins to count down. If the blanking window is currently active and the offset counter expires, the blanking window counter is restarted. The blanking window can cross a PWM period boundary. No blanking window is generated when it is set to zero.

SPINTROL

10.11.2.56 Digital Compare Filter Window Counter Register (DCFWINDOWCNT)

Table 10-118: Digital Compare Filter Window Counter Register (DCFWINDOWCNT) Layout

DCFWINDOWCNT (Digital Compare Filter Window Counter Register) Offset: 0xDC Default: 0x00000000 Access: PWM -> DCFWINDOWCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-119: Digital Compare Filter Window Counter Register (DCFWINDOWCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Blanking window counter It is read only and indicates the current value of the window counter. The counter counts down to zero and then stops until it is re-loaded when the offset counter reaches zero again.

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10.11.2.57 Digital Compare Capture Control Register (DCCAPCTL)

Table 10-120: Digital Compare Capture Control Register (DCCAPCTL) Layout

DCCAPCTL (Digital Compare Capture Control Register) Offset: 0xE0 Default: 0x00000000 Access: PWM -> DCCAPCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				CAPSTS	CAPCLR	DIRECT	CAPEN

Table 10-121: Digital Compare Capture Control Register (DCCAPCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	CAPSTS	RO	0x0	Latched capture status 0: No DC capture event occurred 1: DC capture event has occurred
2	CAPCLR	W1C	0x0	Latched capture status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the latched status. This bit is self-cleared to 0
1	DIRECT	RW	0x0	DCCAP direct load mode 0: Shadow mode. The DCCAP active value is copied to shadow register on a TBCNT=TBPRD or TBCNT=zero event as defined by DCFCTL.PULSESEL. Reads of the DCCAP register always returns the shadow register contents. 1: Direct mode. Reads of the DCCAP register always returns the active value.
0	CAPEN	RW	0x0	TBCNT counter capture enable 0: Disable 1: Enable

SPINTROL

10.11.2.58 Digital Compare Counter Capture Register (DCCAP)

Table 10-122: Digital Compare Counter Capture Register (DCCAP) Layout

DCCAP (Digital Compare Counter Capture Register) Offset: 0xE4 Default: 0x00000000 Access: PWM -> DCCAP.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 10-123: Digital Compare Counter Capture Register (DCCAP) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Captured TBCNT value upon a rising-edge of DCEVTFLT In shadow mode, the captured value is copied to the shadow register on a TBCNT=TBPRD or TBCNT=zero event as defined by DCFCTL.PULSESEL. Reads of the DCCAP register always returns the shadow register contents. In direct mode, reads of the DCCAP register always returns the active value.

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10.11.2.59 Event-Trigger Control Register (ETCTL)

Table 10-124: Event-Trigger Control Register (ETCTL) Layout

ETCTL (Event-Trigger Control Register) Offset: 0xE8 Default: 0x0007B16F
Access: PWM -> ETCTL.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED				SOCCEN	SOCCSEL		
15	14	13	12	11	10	9	8
SOCCSEL	SOCBEN	SOCBSEL				SOCAEN	SOCASEL
7	6	5	4	3	2	1	0
SOCASEL			INTEN	INTSEL			

Table 10-125: Event-Trigger Control Register (ETCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19	SOCCEN	RW	0x0	ADC start of conversion C (SOCC) pulse enable 0: Disable 1: Enable
18:15	SOCCSEL	RW	0xF	SOCC event select 0000: Enable event TBCNT=0 0001: Enable event TBCNT=TBPRD 0010: Enable event TBCNT=0 or TBCNT=TBPRD 0011: Enable event TBCNT=CMPA when TBCNT is counting up 0100: Enable event TBCNT=CMPA when TBCNT is counting down 0101: Enable event TBCNT=CMPB when TBCNT is counting up 0110: Enable event TBCNT=CMPB when TBCNT is counting down 0111: Enable event TBCNT=CMPC when TBCNT is counting up 1000: Enable event TBCNT=CMPC when TBCNT is counting down 1001: Enable event TBCNT=CMPD when TBCNT is counting up 1010: Enable event TBCNT=CMPD when TBCNT is counting down 1011: Enable DCAEVT0.SOC event 1100: Enable DCBEVT0.SOC event Others: SOCC event is disabled

SPINTROL

Bits	Field Name	Type	Reset	Description
14	SOCBEN	RW	0x0	ADC start of conversion B (SOCB) pulse enable 0: Disable 1: Enable
13:10	SOCBSEL	RW	0xC	SOCB event select 0000: Select event TBCNT=0 0001: Select event TBCNT=TBPRD 0010: Select event TBCNT=0 or TBCNT=TBPRD 0011: Select event TBCNT=CMPA when TBCNT is counting up 0100: Select event TBCNT=CMPA when TBCNT is counting down 0101: Select event TBCNT=CMPB when TBCNT is counting up 0110: Select event TBCNT=CMPB when TBCNT is counting down 0111: Select event TBCNT=CMPC when TBCNT is counting up 1000: Select event TBCNT=CMPC when TBCNT is counting down 1001: Select event TBCNT=CMPD when TBCNT is counting up 1010: Select event TBCNT=CMPD when TBCNT is counting down 1011: Select DCAEVT0.SOC event 1100: Select DCBEVT0.SOC event Others: SOCB event is disabled
9	SOCAEN	RW	0x0	ADC start of conversion A (SOCA) pulse enable 0: Disable 1: Enable
8:5	SOCASEL	RW	0xB	SOCA event select 0000: Select event TBCNT=0 0001: Select event TBCNT=TBPRD 0010: Select event TBCNT=0 or TBCNT=TBPRD 0011: Select event TBCNT=CMPA when TBCNT is counting up 0100: Select event TBCNT=CMPA when TBCNT is counting down 0101: Select event TBCNT=CMPB when TBCNT is counting up

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Bits	Field Name	Type	Reset	Description
				0110: Select event TBCNT=CMPB when TBCNT is counting down 0111: Select event TBCNT=CMPC when TBCNT is counting up 1000: Select event TBCNT=CMPC when TBCNT is counting down 1001: Select event TBCNT=CMPD when TBCNT is counting up 1010: Select event TBCNT=CMPD when TBCNT is counting down 1011: Select DCAEVT0.SOC event 1100: Select DCBEVT0.SOC event Others: SOCA event is disabled
4	INTEN	RW	0x0	PWM interrupt enable 0: Disable 1: Enable
3:0	INTSEL	RW	0xF	PWM interrupt select 0000: Select event TBCNT=0 0001: Select event TBCNT=TBPRD 0010: Select event TBCNT=0 or TBCNT=TBPRD 0011: Select event TBCNT=CMPA when TBCNT is counting up 0100: Select event TBCNT=CMPA when TBCNT is counting down 0101: Select event TBCNT=CMPB when TBCNT is counting up 0110: Select event TBCNT=CMPB when TBCNT is counting down 0111: Select event TBCNT=CMPC when TBCNT is counting up 1000: Select event TBCNT=CMPC when TBCNT is counting down 1001: Select event TBCNT=CMPD when TBCNT is counting up 1010: Select event TBCNT=CMPD when TBCNT is counting down 1011: Select DCAEVT0.SOC event 1100: Select DCBEVT0.SOC event Others: Interrupt event is disabled

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10.11.2.60 Event-Trigger Prescale Register (ETPS)

Table 10-126: Event-Trigger Prescale Register (ETPS) Layout

ETPS (Event-Trigger Prescale Register) Offset: 0xEC Default: 0x00000000 Access: PWM -> ETPS.all							
31	30	29	28	27	26	25	24
SOCCCNT				SOCCPRD			
23	22	21	20	19	18	17	16
SOCBCNT				SOCBPRD			
15	14	13	12	11	10	9	8
SOCACNT				SOCAPRD			
7	6	5	4	3	2	1	0
INTCNT				INTPRD			

Table 10-127: Event-Trigger Prescale Register (ETPS) Field Description

Bits	Field Name	Type	Reset	Description
31:28	SOCCCNT	RO	0x0	PWM ADC start-of-conversion C event (SOCC) counter It indicates how many selected ETCTL.SOCCSEL events have occurred. It is automatically cleared when an SOCC pulse is generated. 0000: No events have occurred 0001: 1 event has occurred 0010: 2 events have occurred …… 1111: 15 events have occurred
27:24	SOCCPRD	RW	0x0	PWM ADC start-of-conversion C event (SOCC) period select SOCC is generated upon SOCCPRD<=SOCCCNT and ETCTL.SOCCEN=1. No SOCC will be generated if SOCCPRD=0 0000: Disable SOCC event counter and do not generate SOCC 0001: Generate SOCC when ETPS.SOCCCNT=0001 (1st event) 0010: Generate SOCC when ETPS.SOCCCNT=0010 (2nd event) …… 1111: Generate SOCC when ETPS.SOCCCNT=1111 (15th event)
23:20	SOCBCNT	RO	0x0	PWM ADC start-of-conversion B event (SOCB) counter It indicates how many selected ETCTL.SOCBSEL events have occurred. It is automatically cleared when an SOCB pulse is generated. 0000: No events have occurred 0001: 1 event has occurred 0010: 2 events have occurred …… 1111: 15 events have occurred
19:16	SOCBPRD	RW	0x0	PWM ADC start-of-conversion B event (SOCB) period select SOCB is generated upon SOCBPRD<=SOCBCNT and ETCTL.SOCBEN=1. No SOCB will be generated if SOCBPRD=0

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Bits	Field Name	Type	Reset	Description
				0000: Disable SOCB event counter and do not generate SOCB. 0001: Generate SOCB when ETPS.SOCBCNT=0001 (1st event) 0010: Generate SOCB when ETPS.SOCBCNT=0010 (2nd event) …… 1111: Generate SOCB when ETPS.SOCBCNT=1111 (15th event)
15:12	SOCACNT	RO	0x0	PWM ADC start-of-conversion A event (SOCA) counter It indicates how many selected ETCTL.SOCASEL events have occurred. It is automatically cleared when an SOCA pulse is generated. 0000: No events have occurred 0001: 1 event has occurred 0010: 2 events have occurred …… 1111: 15 events have occurred
11:8	SOCAPRD	RW	0x0	PWM ADC start-of-conversion A event (SOCA) period select SOCA is generated upon SOCAPRD<=SOCACNT and ETCTL.SOCAEN=1. No SOCA will be generated if SOCAPRD=0 0000: Disable SOCA event counter and do not generate SOCA. 0001: Generate SOCA when ETPS.SOCACNT=0001 (1st event) 0010: Generate SOCA when ETPS.SOCACNT=0010 (2nd event) …… 1111: Generate SOCA when ETPS.SOCACNT=1111 (15th event)
7:4	INTCNT	RO	0x0	PWM interrupt counter It indicates how many selected ETCTL.INTSEL events have occurred. It is automatically cleared when an interrupt pulse is generated. 0000: No events have occurred 0001: 1 event has occurred 0010: 2 events have occurred …… 1111: 15 events have occurred
3:0	INTPRD	RW	0x0	PWM interrupt period select Interrupt is generated upon INTPRD<=INTCNT and ETCTL.INTEN=1. No interrupt will be generated if INTPRD=0 0000: Disable the interrupt event counter. No interrupt will be generated. 0001: Generate an interrupt when ETPS.INTCNT=0001 0010: Generate an interrupt when ETPS.INTCNT=0010 …… 1111: Generate an interrupt when ETPS.INTCNT=1111

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10.11.2.61 Event-Trigger Flag Register (ETFLG)

Table 10-128: Event-Trigger Flag Register (ETFLG) Layout

ETFLG (Event-Trigger Flag Register) Offset: 0xF0 Default: 0x00000000 Access: PWM -> ETFLG.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				SOCC	SOCB	SOCA	INT

Table 10-129: Event-Trigger Flag Register (ETFLG) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	SOCC	RO	0x0	Latched PWM ADC start-of-conversion C flag 0: Indicates no event occurred. 1: Indicates a SOCC event was generated. The pulse will continue to be generated even if the flag is set.
2	SOCB	RO	0x0	Latched PWM ADC start-of-conversion B flag 0: Indicates no event occurred. 1: Indicates a SOCB event was generated. The pulse will continue to be generated even if the flag is set.
1	SOCA	RO	0x0	Latched PWM ADC start-of-conversion A flag 0: Indicates no event occurred. 1: Indicates a SOCA event was generated. The pulse will continue to be generated even if the flag is set.
0	INT	RO	0x0	Latched PWM interrupt flag 0: Indicates no event occurred. 1: Indicates a PWM interrupt was generated. No further interrupts will be generated until the flag bit is cleared.

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10.11.2.62 Event-Trigger Clear Register (ETCLR)

Table 10-130: Event-Trigger Clear Register (ETCLR) Layout

ETCLR (Event-Trigger Clear Register) Offset: 0xF4 Default: 0x00000000 Access: PWM -> ETCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				SOCC	SOCB	SOCA	INT

Table 10-131: Event-Trigger Clear Register (ETCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	SOCC	W1C	0x0	Latched PWM ADC start-of-conversion C flag clear 0: Write a 0 has no effect and always readback 0. 1: Write a 1 clears ETFLG.SOCC. This bit is self-cleared to 0
2	SOCB	W1C	0x0	Latched PWM ADC start-of-conversion B flag clear 0: Write a 0 has no effect and always readback 0. 1: Write a 1 clears ETFLG.SOCB. This bit is self-cleared to 0
1	SOCA	W1C	0x0	Latched PWM ADC start-of-conversion A flag clear 0: Write a 0 has no effect and always readback 0. 1: Write a 1 clears ETFLG.SOCA. This bit is self-cleared to 0
0	INT	W1C	0x0	Latched PWM interrupt flag clear 0: Write a 0 has no effect and always readback 0. 1: Write a 1 clears ETFLG.INT. This bit is self-cleared to 0

SPINTROL

10.11.2.63 Event-Trigger Force Register (ETFRC)

Table 10-132: Event-Trigger Force Register (ETFRC) Layout

ETFRC (Event-Trigger Force Register) Offset: 0xF8 Default: 0x00000000 Access: PWM -> ETFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				SOCC	SOCB	SOCA	INT

Table 10-133: Event-Trigger Force Register (ETFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	SOCC	W1S	0x0	Software force a start-of-conversion C pulse This bit is ignored if ETCTL.SOCCEN=0 or ETPS.SOCCPRD=0 0: Write a 0 has no effect and always readback 0. 1: Write a 1 generates a SOCC event. This bit is self-cleared to 0.
2	SOCB	W1S	0x0	Software force a start-of-conversion B pulse This bit is ignored if ETCTL.SOCBEN=0 or ETPS.SOCBPRD=0 0: Write a 0 has no effect and always readback 0. 1: Write a 1 generates a SOCB event. This bit is self-cleared to 0.
1	SOCA	W1S	0x0	Software force a start-of-conversion A pulse This bit is ignored if ETCTL.SOCAEN=0 or ETPS.SOCAPRD=0 0: Write a 0 has no effect and always readback 0. 1: Write a 1 generates a SOCA event. This bit is self-cleared to 0.
0	INT	W1S	0x0	Software force a PWM interrupt This bit is ignored if ETCTL.INTEN=0 or ETPS.INTPRD=00 0: Write a 0 has no effect and always readback 0. 1: Write a 1 generates an interrupt event. This bit is self-cleared to 0.

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10.11.2.64 PWM Register Write-Allow Key Register (PWMREGKEY)

Table 10-134: PWM Register Write-Allow Key Register (PWMREGKEY) Layout

PWMREGKEY (PWM Register Write-Allow Key Register) Offset: 0xFC Default: 0x1ACCE551 Access: PWM -> PWMREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 10-135: PWM Register Write-Allow Key Register (PWMREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected PWM registers

SPINTROL

10.11.3 PWMCFG register map

Table 10-136: PWMCFG Module Base Address

Peripheral Module	Base Address
PWMCFG	0x4000 9F00

Table 10-137: PWMCFG Register Map

Register	Offset	Description	Reset Value
TZ0SRCCTL*	0x00	TZ0 Source Control Register	0x0000007F
TZ1SRCCTL*	0x04	TZ1 Source Control Register	0x0000007F
TZ2SRCCTL*	0x08	TZ2 Source Control Register	0x0000007F
TZ3SRCCTL*	0x0C	TZ3 Source Control Register	0x0000007F
TZ4SRCCTL*	0x10	TZ4 Source Control Register	0x0000007F
FRCSYNC	0x14	Global PWM Force Synchronization Register	0x00000000
GPIOSYNCCTL*	0x18	GPIO PWMSYNCI Control Register	0x0000007F
GPIOSYNCEN*	0x1C	GPIO Force PWMSYNCI Enable Register	0x00000009
TMR0SYNCEN*	0x20	Timer 0 Force PWMSYNCI Enable Register	0x00000000
TMR1SYNCEN*	0x24	Timer 1 Force PWMSYNCI Enable Register	0x00000000
TMR2SYNCEN*	0x28	Timer 2 Force PWMSYNCI Enable Register	0x00000000
SYNCOCTL*	0x2C	PWMSYNCO Control Register	0x00000007
SOCAOCTL*	0x30	PWMSOCA Output Control Register	0x00000007
SOCBOCTL*	0x34	PWMSOCB Output Control Register	0x00000007
SOCCOCTL*	0x38	PWMSOCC Output Control Register	0x00000007
PWMCFGKEY	0x3C	PWMCFG Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the PWMCFGKEY=0x1ACCE551.

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10.11.4 PWMCFG registers

10.11.4.1 TZ0 Source Control Register (TZ0SRCCTL)

Table 10-138: TZ0 Source Control Register (TZ0SRCCTL) Layout

TZ0SRCCTL (TZ0 Source Control Register) Offset: 0x0 Default: 0x0000007F Access: PWMCFG -> TZ0SRCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 10-139: TZ0 Source Control Register (TZ0SRCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	TZ0 polarity 0: Active when low 1: Active when high
5:0	IOSEL	RW	0x3F	GPIO number for TZ0 event

10.11.4.2 TZ1 Source Control Register (TZ1SRCCTL)

Table 10-140: TZ1 Source Control Register (TZ1SRCCTL) Layout

TZ1SRCCTL (TZ1 Source Control Register) Offset: 0x4 Default: 0x0000007F Access: PWMCFG -> TZ1SRCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 10-141: TZ1 Source Control Register (TZ1SRCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	TZ1 polarity 0: Active when low 1: Active when high
5:0	IOSEL	RW	0x3F	GPIO number for TZ1 event

SPINTROL

10.11.4.3 TZ2 Source Control Register (TZ2SRCCTL)

Table 10-142: TZ2 Source Control Register (TZ2SRCCTL) Layout

TZ2SRCCTL (TZ2 Source Control Register) Offset: 0x8 Default: 0x0000007F Access: PWMCFG -> TZ2SRCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 10-143: TZ2 Source Control Register (TZ2SRCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	TZ2 polarity 0: Active when low 1: Active when high
5:0	IOSEL	RW	0x3F	GPIO number for TZ2 event

10.11.4.4 TZ3 Source Control Register (TZ3SRCCTL)

Table 10-144: TZ3 Source Control Register (TZ3SRCCTL) Layout

TZ3SRCCTL (TZ3 Source Control Register) Offset: 0xC Default: 0x0000007F Access: PWMCFG -> TZ3SRCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 10-145: TZ3 Source Control Register (TZ3SRCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	TZ3 polarity 0: Active when low 1: Active when high
5:0	IOSEL	RW	0x3F	GPIO number for TZ3 event

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10.11.4.5 TZ4 Source Control Register (TZ4SRCCTL)

Table 10-146: TZ4 Source Control Register (TZ4SRCCTL) Layout

TZ4SRCCTL (TZ4 Source Control Register) Offset: 0x10 Default: 0x0000007F Access: PWMCFG -> TZ4SRCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 10-147: TZ4 Source Control Register (TZ4SRCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	TZ4 polarity 0: Active when low 1: Active when high
5:0	IOSEL	RW	0x3F	GPIO number for TZ4 event

SPINTROL

10.11.4.6 Global PWM Force Synchronization Register (FRCSYNC)

Table 10-148: Global PWM Force Synchronization Register (FRCSYNC) Layout

FRCSYNC (Global PWM Force Synchronization Register) Offset: 0x14 Default: 0x00000000 Access: PWMCFG -> FRCSYNC.all							
31	30	29	28	27	26	25	24
PWMCLK	RESERVED						
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
PWM7SYNC	PWM6SYNC	PWM5SYNC	PWM4SYNC	PWM3SYNC	PWM2SYNC	PWM1SYNC	PWM0SYNC

Table 10-149: Global PWM Force Synchronization Register (FRCSYNC) Field Description

Bits	Field Name	Type	Reset	Description
31	PWMCLK	W1S	0x0	Software forced synchronization on clock for all PWMs 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC on all PWM clocks This bit is self-cleared
30:8	RESERVED_30_8	RO	0x0	Reserved
7	PWM7SYNC	W1S	0x0	Software forced synchronization on PWM7 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM7. This bit is self-cleared
6	PWM6SYNC	W1S	0x0	Software forced synchronization on PWM6 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM6. This bit is self-cleared
5	PWM5SYNC	W1S	0x0	Software forced synchronization on PWM5 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM5. This bit is self-cleared
4	PWM4SYNC	W1S	0x0	Software forced synchronization on PWM4 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM4. This bit is self-cleared

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Bits	Field Name	Type	Reset	Description
3	PWM3SYNC	W1S	0x0	Software forced synchronization on PWM3 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM3. This bit is self-cleared
2	PWM2SYNC	W1S	0x0	Software forced synchronization on PWM2 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM2. This bit is self-cleared
1	PWM1SYNC	W1S	0x0	Software forced synchronization on PWM1 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM1. This bit is self-cleared
0	PWM0SYNC	W1S	0x0	Software forced synchronization on PWM0 0: Write a 0 has no effect. Always readback 0. 1: Write a 1 will force a SYNC event on PWM0. This bit is self-cleared

10.11.4.7 GPIO PWMSYNCI Control Register (GPIOSYNCCTL)

Table 10-150: GPIO PWMSYNCI Control Register (GPIOSYNCCTL) Layout

GPIOSYNCCTL (GPIO PWMSYNCI Control Register) Offset: 0x18 Default: 0x0000007F Access: PWMCFG -> GPIOSYNCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 10-151: GPIO PWMSYNCI Control Register (GPIOSYNCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	PWMSYNCI input polarity 0: Active when low 1: Active when high
5:0	IOSEL	RW	0x3F	GPIO number for PWMSYNCI input

SPINTROL

10.11.4.8 GPIO Force PWMSYNCI Enable Register (GPIOSYNCEN)

Table 10-152: GPIO Force PWMSYNCI Enable Register (GPIOSYNCEN) Layout

GPIOSYNCEN (GPIO Force PWMSYNCI Enable Register) Offset: 0x1C Default: 0x00000009 Access: PWMCFG -> GPIOSYNCEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7 PWM7SYNC	6 PWM6SYNC	5 PWM5SYNC	4 PWM4SYNC	3 PWM3SYNC	2 PWM2SYNC	1 PWM1SYNC	0 PWM0SYNC

Table 10-153: GPIO Force PWMSYNCI Enable Register (GPIOSYNCEN) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	PWM7SYNC	RW	0x0	Enable PWM7 synchronization by GPIO 0: Disable 1: Enable
6	PWM6SYNC	RW	0x0	Enable PWM6 synchronization by GPIO 0: Disable 1: Enable
5	PWM5SYNC	RW	0x0	Enable PWM5 synchronization by GPIO 0: Disable 1: Enable
4	PWM4SYNC	RW	0x0	Enable PWM4 synchronization by GPIO 0: Disable 1: Enable
3	PWM3SYNC	RW	0x1	Enable PWM3 synchronization by GPIO 0: Disable 1: Enable
2	PWM2SYNC	RW	0x0	Enable PWM2 synchronization by GPIO 0: Disable 1: Enable
1	PWM1SYNC	RW	0x0	Enable PWM1 synchronization by GPIO 0: Disable 1: Enable
0	PWM0SYNC	RW	0x1	Enable PWM0 synchronization by GPIO 0: Disable 1: Enable

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10.11.4.9 Timer 0 Force PWMSYNCI Enable Register (TMR0SYNCEN)

Table 10-154: Timer 0 Force PWMSYNCI Enable Register (TMR0SYNCEN) Layout

TMR0SYNCEN (Timer 0 Force PWMSYNCI Enable Register) Offset: 0x20 Default: 0x00000000 Access: PWMCFG -> TMR0SYNCEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7 PWM7SYNC	6 PWM6SYNC	5 PWM5SYNC	4 PWM4SYNC	3 PWM3SYNC	2 PWM2SYNC	1 PWM1SYNC	0 PWM0SYNC

Table 10-155: Timer 0 Force PWMSYNCI Enable Register (TMR0SYNCEN) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	PWM7SYNC	RW	0x0	Enable PWM7 synchronization by Timer 0 0: Disable 1: Enable
6	PWM6SYNC	RW	0x0	Enable PWM6 synchronization by Timer 0 0: Disable 1: Enable
5	PWM5SYNC	RW	0x0	Enable PWM5 synchronization by Timer 0 0: Disable 1: Enable
4	PWM4SYNC	RW	0x0	Enable PWM4 synchronization by Timer 0 0: Disable 1: Enable
3	PWM3SYNC	RW	0x0	Enable PWM3 synchronization by Timer 0 0: Disable 1: Enable
2	PWM2SYNC	RW	0x0	Enable PWM2 synchronization by Timer 0 0: Disable 1: Enable
1	PWM1SYNC	RW	0x0	Enable PWM1 synchronization by Timer 0 0: Disable 1: Enable
0	PWM0SYNC	RW	0x0	Enable PWM0 synchronization by Timer 0 0: Disable 1: Enable

SPINTROL

10.11.4.10 Timer 1 Force PWMSYNCI Enable Register (TMR1SYNCEN)

Table 10-156: Timer 1 Force PWMSYNCI Enable Register (TMR1SYNCEN) Layout

TMR1SYNCEN (Timer 1 Force PWMSYNCI Enable Register) Offset: 0x24 Default: 0x00000000 Access: PWMCFG -> TMR1SYNCEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7 PWM7SYNC	6 PWM6SYNC	5 PWM5SYNC	4 PWM4SYNC	3 PWM3SYNC	2 PWM2SYNC	1 PWM1SYNC	0 PWM0SYNC

Table 10-157: Timer 1 Force PWMSYNCI Enable Register (TMR1SYNCEN) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	PWM7SYNC	RW	0x0	Enable PWM7 synchronization by Timer 1 0: Disable 1: Enable
6	PWM6SYNC	RW	0x0	Enable PWM6 synchronization by Timer 1 0: Disable 1: Enable
5	PWM5SYNC	RW	0x0	Enable PWM5 synchronization by Timer 1 0: Disable 1: Enable
4	PWM4SYNC	RW	0x0	Enable PWM4 synchronization by Timer 1 0: Disable 1: Enable
3	PWM3SYNC	RW	0x0	Enable PWM3 synchronization by Timer 1 0: Disable 1: Enable
2	PWM2SYNC	RW	0x0	Enable PWM2 synchronization by Timer 1 0: Disable 1: Enable
1	PWM1SYNC	RW	0x0	Enable PWM1 synchronization by Timer 1 0: Disable 1: Enable
0	PWM0SYNC	RW	0x0	Enable PWM0 synchronization by Timer 1 0: Disable 1: Enable

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10.11.4.11 Timer 2 Force PWMSYNCI Enable Register (TMR2SYNCEN)

Table 10-158: Timer 2 Force PWMSYNCI Enable Register (TMR2SYNCEN) Layout

TMR2SYNCEN (Timer 2 Force PWMSYNCI Enable Register) Offset: 0x28 Default: 0x00000000 Access: PWMCFG -> TMR2SYNCEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7 PWM7SYNC	6 PWM6SYNC	5 PWM5SYNC	4 PWM4SYNC	3 PWM3SYNC	2 PWM2SYNC	1 PWM1SYNC	0 PWM0SYNC

Table 10-159: Timer 2 Force PWMSYNCI Enable Register (TMR2SYNCEN) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	PWM7SYNC	RW	0x0	Enable PWM7 synchronization by Timer 2 0: Disable 1: Enable
6	PWM6SYNC	RW	0x0	Enable PWM6 synchronization by Timer 2 0: Disable 1: Enable
5	PWM5SYNC	RW	0x0	Enable PWM5 synchronization by Timer 2 0: Disable 1: Enable
4	PWM4SYNC	RW	0x0	Enable PWM4 synchronization by Timer 2 0: Disable 1: Enable
3	PWM3SYNC	RW	0x0	Enable PWM3 synchronization by Timer 2 0: Disable 1: Enable
2	PWM2SYNC	RW	0x0	Enable PWM2 synchronization by Timer 2 0: Disable 1: Enable
1	PWM1SYNC	RW	0x0	Enable PWM1 synchronization by Timer 2 0: Disable 1: Enable
0	PWM0SYNC	RW	0x0	Enable PWM0 synchronization by Timer 2 0: Disable 1: Enable

SPINTROL

10.11.4.12 PWMSYNCO Control Register (SYNCOCTL)

Table 10-160: PWMSYNCO Control Register (SYNCOCTL) Layout

SYNCOCTL (PWMSYNCO Control Register) Offset: 0x2C Default: 0x00000007 Access: PWMCFG -> SYNCOCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		SRCSEL			POL	DURATION	

Table 10-161: PWMSYNCO Control Register (SYNCOCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5:3	SRCSEL	RW	0x0	PWMSYNCO source select 000: Source select from PWM0 001: Source select from PWM1 010: Source select from PWM2 011: Source select from PWM3 100: Source select from PWM4 101: Source select from PWM5 110: Source select from PWM6 111: Source select from PWM7
2	POL	RW	0x1	Polarity of PWMSYNCO to the pin 0: Active when low 1: Active when high
1:0	DURATION	RW	0x3	Pulse duration of PWMSYNCO to the pin 00: Duration of PWMSYNCO pulse to the pin is 4 PWM clocks 01: Duration of PWMSYNCO pulse to the pin is 8 PWM clocks 10: Duration of PWMSYNCO pulse to the pin is 16 PWM clocks 11: Duration of PWMSYNCO pulse to the pin is 32 PWM clocks

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10.11.4.13 PWMSOCA Output Control Register (SOCAOCTL)

Table 10-162: PWMSOCA Output Control Register (SOCAOCTL) Layout

SOCAOCTL (PWMSOCA Output Control Register) Offset: 0x30 Default: 0x00000007 Access: PWMCFG -> SOCAOCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					SOCA7EN	SOCA6EN	SOCA5EN
7	6	5	4	3	2	1	0
SOCA4EN	SOCA3EN	SOCA2EN	SOCA1EN	SOCA0EN	POL	DURATION	

Table 10-163: PWMSOCA Output Control Register (SOCAOCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	SOCA7EN	RW	0x0	Enable PWM7SOCA output to the pin 0: Disable 1: Enable
9	SOCA6EN	RW	0x0	Enable PWM6SOCA output to the pin 0: Disable 1: Enable
8	SOCA5EN	RW	0x0	Enable PWM5SOCA output to the pin 0: Disable 1: Enable
7	SOCA4EN	RW	0x0	Enable PWM4SOCA output to the pin 0: Disable 1: Enable
6	SOCA3EN	RW	0x0	Enable PWM3SOCA output to the pin 0: Disable 1: Enable
5	SOCA2EN	RW	0x0	Enable PWM2SOCA output to the pin 0: Disable 1: Enable
4	SOCA1EN	RW	0x0	Enable PWM1SOCA output to the pin 0: Disable 1: Enable
3	SOCA0EN	RW	0x0	Enable PWM0SOCA output to the pin 0: Disable 1: Enable
2	POL	RW	0x1	Polarity of PWMSOCA output to the pin

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Bits	Field Name	Type	Reset	Description
				0: Active when low 1: Active when high
1:0	DURATION	RW	0x3	Pulse duration of PWMSOCA output to the pin 00: Pulse duration to the pin is 4 PWM clocks 01: Pulse duration to the pin is 8 PWM clocks 10: Pulse duration to the pin is 16 PWM clocks 11: Pulse duration to the pin is 32 PWM clocks

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10.11.4.14 PWMSOCB Output Control Register (SOCBOCTL)

Table 10-164: PWMSOCB Output Control Register (SOCBOCTL) Layout

SOCBOCTL (PWMSOCB Output Control Register) Offset: 0x34 Default: 0x00000007 Access: PWMCFG -> SOCBOCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					SOCB7EN	SOCB6EN	SOCB5EN
7	6	5	4	3	2	1	0
SOCB4EN	SOCB3EN	SOCB2EN	SOCB1EN	SOCB0EN	POL	DURATION	

Table 10-165: PWMSOCB Output Control Register (SOCBOCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	SOCB7EN	RW	0x0	Enable PWM7SOCB output to the pin 0: Disable 1: Enable
9	SOCB6EN	RW	0x0	Enable PWM6SOCB output to the pin 0: Disable 1: Enable
8	SOCB5EN	RW	0x0	Enable PWM5SOCB output to the pin 0: Disable 1: Enable
7	SOCB4EN	RW	0x0	Enable PWM4SOCB output to the pin 0: Disable 1: Enable
6	SOCB3EN	RW	0x0	Enable PWM3SOCB output to the pin 0: Disable 1: Enable
5	SOCB2EN	RW	0x0	Enable PWM2SOCB output to the pin 0: Disable 1: Enable
4	SOCB1EN	RW	0x0	Enable PWM1SOCB output to the pin 0: Disable 1: Enable
3	SOCB0EN	RW	0x0	Enable PWM0SOCB output to the pin 0: Disable 1: Enable
2	POL	RW	0x1	Polarity of PWMSOCB output to the pin

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Bits	Field Name	Type	Reset	Description
				0: Active when low 1: Active when high
1:0	DURATION	RW	0x3	Pulse duration of PWMSOCB output to the pin 00: Pulse duration to the pin is 4 PWM clocks 01: Pulse duration to the pin is 8 PWM clocks 10: Pulse duration to the pin is 16 PWM clocks 11: Pulse duration to the pin is 32 PWM clocks

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10.11.4.15 PWMSOCC Output Control Register (SOCCOCTL)

Table 10-166: PWMSOCC Output Control Register (SOCCOCTL) Layout

SOCCOCTL (PWMSOCC Output Control Register) Offset: 0x38 Default: 0x00000007 Access: PWMCFG -> SOCCOCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					SOCC7EN	SOCC6EN	SOCC5EN
7	6	5	4	3	2	1	0
SOCC4EN	SOCC3EN	SOCC2EN	SOCC1EN	SOCC0EN	POL	DURATION	

Table 10-167: PWMSOCC Output Control Register (SOCCOCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	SOCC7EN	RW	0x0	Enable PWM7SOCC output to the pin 0: Disable 1: Enable
9	SOCC6EN	RW	0x0	Enable PWM6SOCC output to the pin 0: Disable 1: Enable
8	SOCC5EN	RW	0x0	Enable PWM5SOCC output to the pin 0: Disable 1: Enable
7	SOCC4EN	RW	0x0	Enable PWM4SOCC output to the pin 0: Disable 1: Enable
6	SOCC3EN	RW	0x0	Enable PWM3SOCC output to the pin 0: Disable 1: Enable
5	SOCC2EN	RW	0x0	Enable PWM2SOCC output to the pin 0: Disable 1: Enable
4	SOCC1EN	RW	0x0	Enable PWM1SOCC output to the pin 0: Disable 1: Enable
3	SOCC0EN	RW	0x0	Enable PWM0SOCC output to the pin 0: Disable 1: Enable
2	POL	RW	0x1	Polarity of PWMSOCC output to the pin

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Bits	Field Name	Type	Reset	Description
				0: Active when low 1: Active when high
1:0	DURATION	RW	0x3	Pulse duration of PWMSOCC output to the pin 00: Pulse duration to the pin is 4 PWM clocks 01: Pulse duration to the pin is 8 PWM clocks 10: Pulse duration to the pin is 16 PWM clocks 11: Pulse duration to the pin is 32 PWM clocks

10.11.4.16 PWMCFG Register Write-Allow Key Register (PWMCFGKEY)

Table 10-168: PWMCFG Register Write-Allow Key Register (PWMCFGKEY) Layout

PWMCFGKEY (PWMCFG Register Write-Allow Key Register) Offset: 0x3C Default: 0x1ACCE551 Access: PWMCFG -> PWMCFGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 10-169: PWMCFG Register Write-Allow Key Register (PWMCFGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected PWMCFG registers

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11 ECAP

11.1 Introduction

The enhanced capture (ECAP) module is used in situations where accurate timing of external events is important. This chapter describes the module and how to use it.

Uses for ECAP include:

- Speed measurements of rotating machinery (e.g., e-bike motor with Hall sensors)
- Measure period and duty cycle of pulse signals
- Decoding information derived from duty cycle encoded systems

The ECAP module described in this guide includes the following features:

- 32-bit time base with 5 ns time resolution (max 200 MHz system clock)
- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single shot capture of up to four event time-stamps
- Continuous mode capture of time-stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- All above resources dedicated to a single input pin
- The ECAP module can be configured as a PWM output if not used in capture mode

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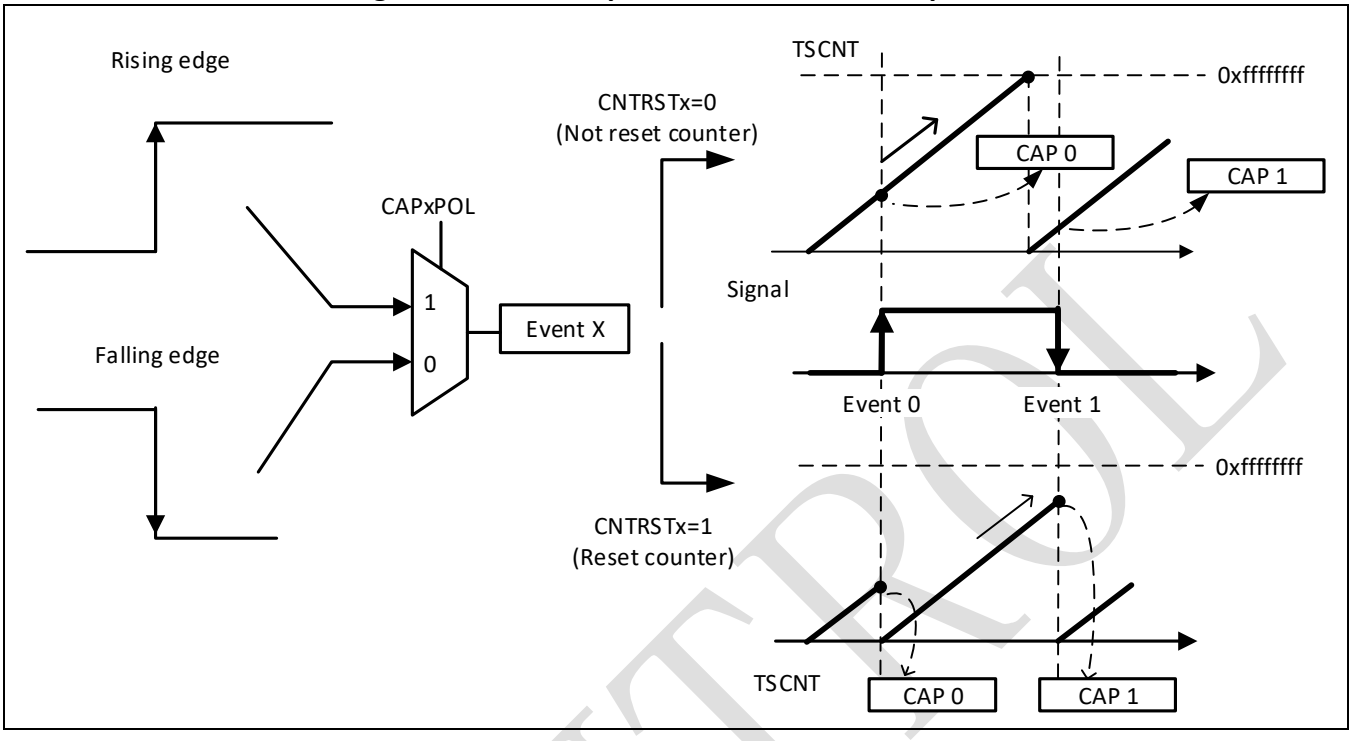
11.2 Description

Figure 11-1: Basic operation of enhanced capture



The philosophy of enhanced capture (ECAP) module is regarded “rising” and “falling” edge of signal captured as abstract symbols–called events, which can be named as four number sequence with time. In other words, Event0 to Event3 symbolize consequence in time, and each of them can be programmed as rising or falling edge. This is set by CAPCTL.CAPxPOL field.

The second is to set counter behavior after event happened. This behavior can clear ECAP counter or do nothing about it by setting CAPCTL.CNTRSTx.

With above two basic configuration of events and counter, users can make complicated capture function such as period and duty calculation with other registers illustrated later. Figure 11-1 shows the basic two operation of ECAP.

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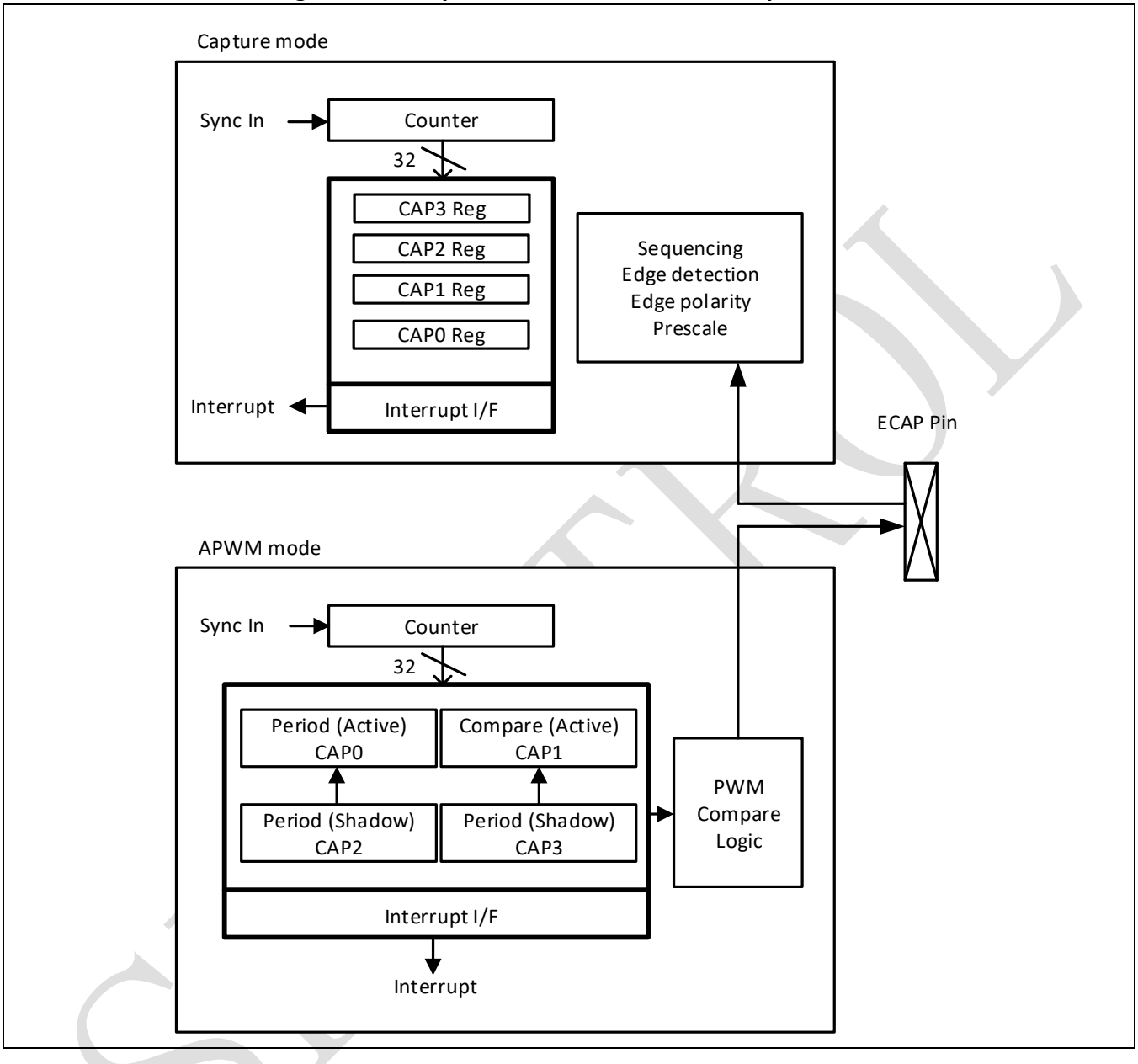
11.3 Capture and APWM operating mode

Figure 11-2: Capture and APWM modes of operation



User can take ECAP module resources to implement a single-channel PWM generator (with 32 bit capabilities) when it is not being used for input captures. The counter operates in count-up mode, providing a time-base for asymmetrical pulse width modulation (PWM) waveforms.

The CAP0 and CAP1 registers become the active period and compare registers, respectively, while CAP2 and CAP3 registers become the period and capture shadow registers, respectively. Figure 11-2 is a high-level view of both the capture and auxiliary pulse-width modulator (APWM) modes of operation.

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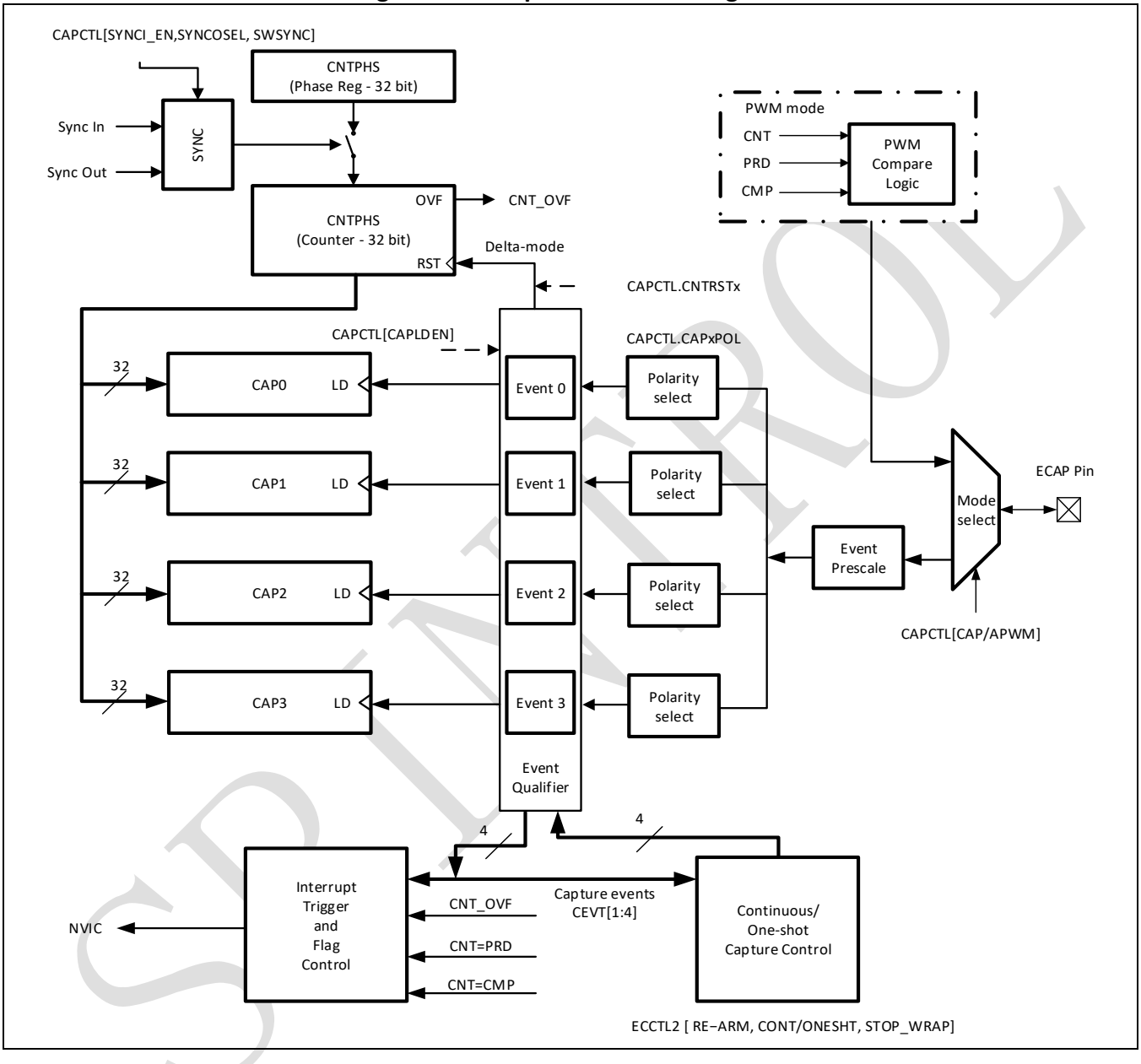
11.4 Capture mode description

Figure 11-3 shows the various components that implement the capture function. The ECAP Pin is sourced from GPIO pin according to CAPSRCCTL register.

Figure 11-3: Capture function diagram



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11.4.1 Event prescaler

An input capture signal (continuous pulse series) can be prescaled by N = CAPCTL.EVTDIV+1. This is useful when very high frequency signals are used as inputs. Figure 11-4 shows a functional diagram and Figure 11-5 shows the operation of the prescale function.

Figure 11-4: Event prescale control

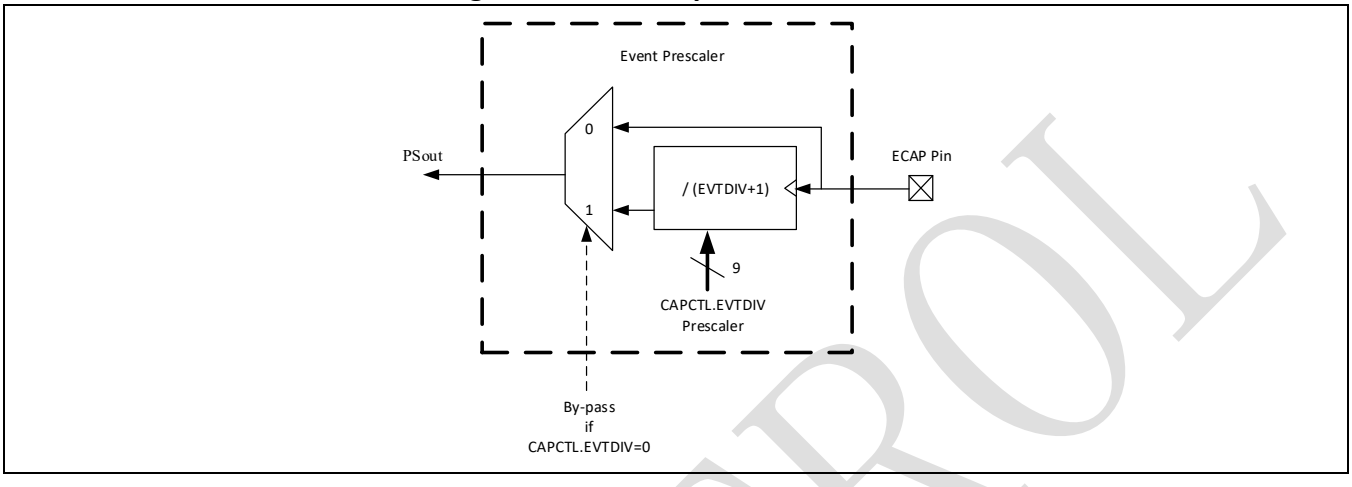
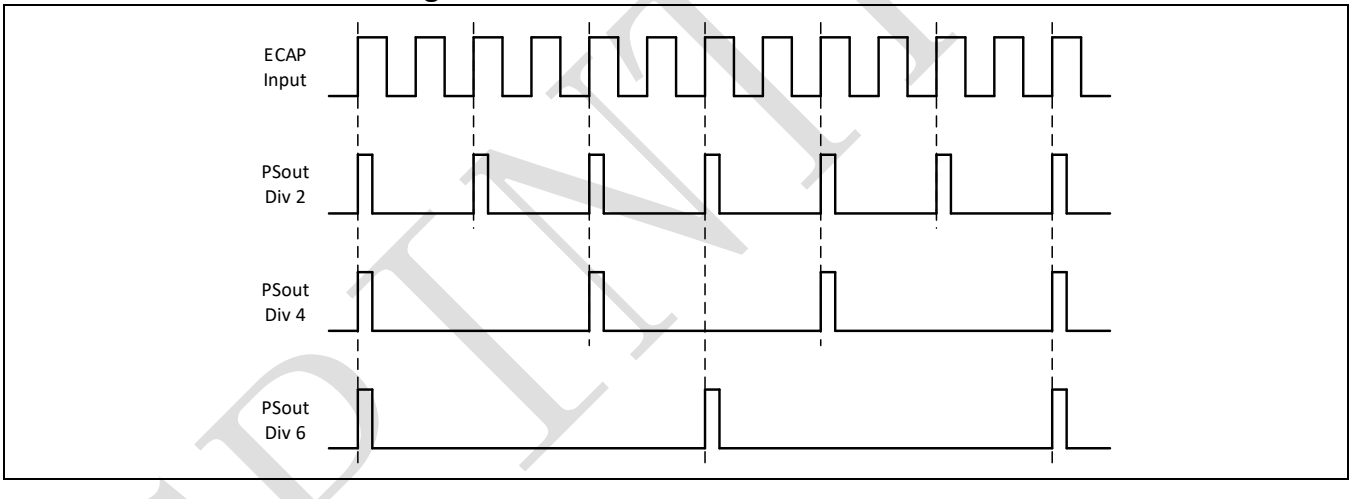


Figure 11-5: Prescale function waveforms



Note: The ECAP event prescaler is implemented with existing clock divider IP, so there is extra four event cycles (regarded as clock cycles to the divider) required to initialize the divider after power-up. For one shot mode, in which the user cares about exactly each incoming event, the first 4 events may not work correctly. We add software work-around to purposely generate 4 dummy events via GPIO toggling to initialize the event prescaler in ECAP module demo code.

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11.4.2 Edge polarity select and qualifier

Four independent edge polarity (rising edge/falling edge) selection MUXes are used, one for each capture event.

- Each edge (up to 4) is event qualified by the Modulo-4 sequencer.
- The edge event is gated to its respective CAPx register by the Mod4 counter. The CAPx register is loaded on the falling edge.

11.4.3 Continuous/one-shot control

The Mod4 (2 bit) counter is incremented via edge qualified events (CEVT0-CEVT3). The function of this counter index which event in sequence occurs now. It will cooperate with CAPCTL.STOPWARP to control the length of such capture event sequence.

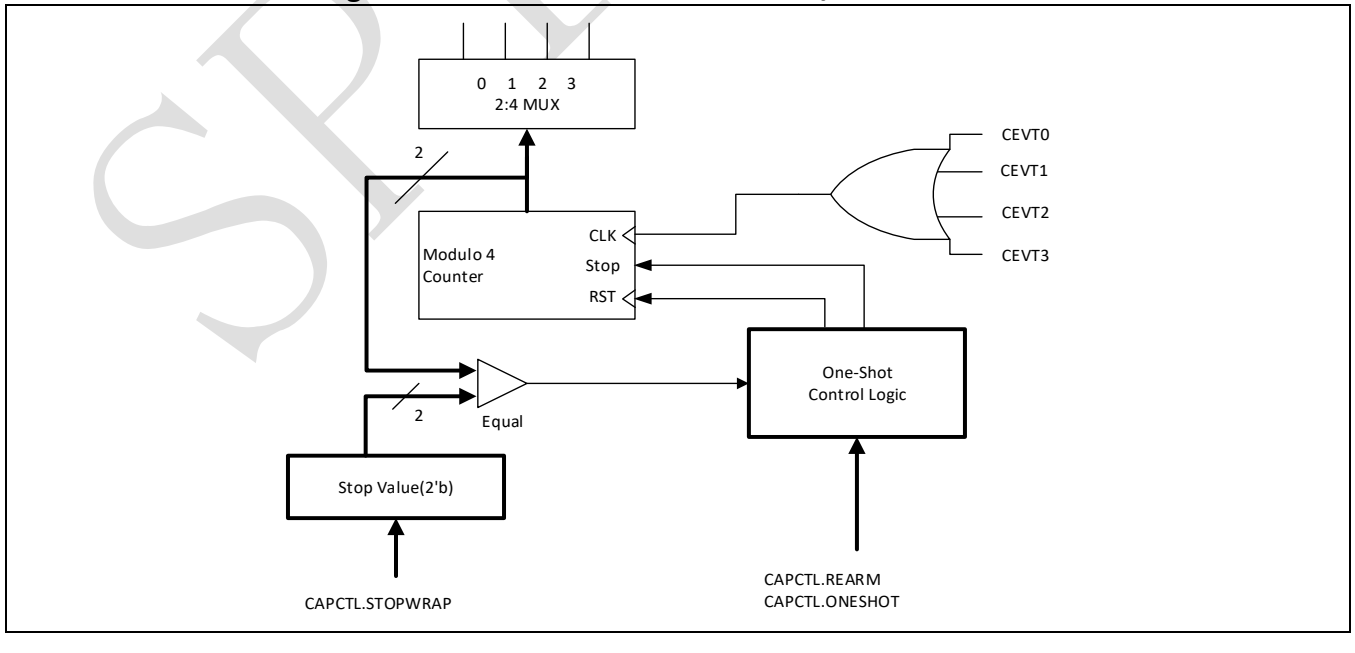
- The Mod4 counter continues counting (0->1->2->3->0) and wraps around unless stopped.
- A 2-bit stop register (CAPCTL.STOPWARP) is used to compare the Mod4 counter output, and when equal stops the Mod4 counter and inhibits further loads of the CAP0-CAP3 registers. This occurs during one-shot operation.

The continuous/one-shot block controls the start/stop and reset (zero) functions of the Mod4 counter via a mono-shot type of action that can be triggered by the stop-value comparator and re-armed via software control.

Once armed, the ECAP module waits for 1-4 (defined by stop-value) capture events before freezing both the Mod4 counter and contents of CAP0-3 registers (i.e., time-stamps).

Re-arming prepares the ECAP module for another capture sequence. Also re-arming clears (to zero) theMod4 counter and permits loading of CAP0-3 registers again, providing the CAPLDEN bit is set. In continuous mode, the Mod4 counter continues to run (0->1->2->3->0, the one-shot action is ignored, and capture values continue to be written to CAP0-3 in a circular buffer sequence.

Figure 11-6: Details of the continuous/one-shot block



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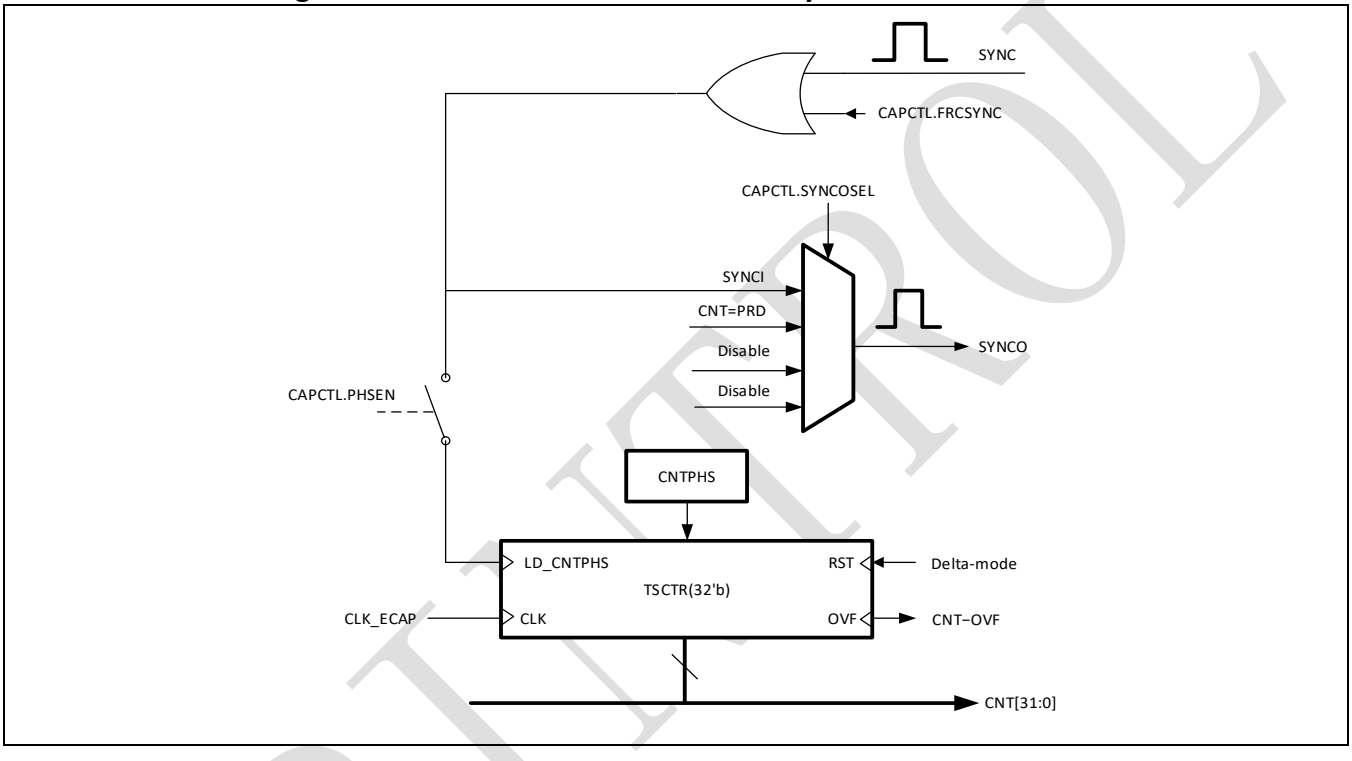
11.4.4 32-bit counter and phase control

This counter provides the time-base for event captures, and is clocked via the CLK_ECAP. A phase register is provided to achieve synchronization with other counters, via a hardware and software forced sync. This is useful in APWM mode when a phase offset between modules is needed.

On any of the four event loads, an option to reset the 32-bit counter is given. This is useful for time difference capture. The 32-bit counter value is captured first, then it is reset to 0 by any of the LD0-LD3 signals.

Figure 11-7: Details of the counter and synchronization block



11.4.5 CAP0-CAP3 registers

These 32-bit registers are fed by the 32-bit counter timer bus TSCNT and are loaded (i.e., capture a time-stamp) when their respective LD inputs are strobed. Loading of the capture registers can be inhibited via control bit CAPLDEN. During one-shot operation, this bit is cleared (loading is inhibited) automatically when a stop condition occurs, i.e. Stop Value = Mod4.

CAP0 and CAP1 registers become the active period and compare registers, respectively, in APWM mode.CAP2 and CAP3 registers become the respective shadow registers (APRD and ACMP) for CAP0 and CAP1 during APWM operation.

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11.4.6 Interrupt control

An Interrupt can be generated on capture events (CEVT0-CEVT3, CNTOVF) or APWM events (CNT = PRD, CNT = CMP).A counter overflow event (0xFFFFFFFF->0x00000000) is also provided as an interrupt source (CNTOVF).The capture events are edge and sequencer qualified (i.e., ordered in time) by the polarity select andMod4 gating, respectively.

One of these events can be selected as the interrupt source (from the ECAP module) going to the PIE. Seven interrupt events (CEVT0, CEVT1, CEVT2, CEVT3, CNTOVF, CNT=PRD, CNT=CMP) can be generated. The interrupt enable register (CAPIE) is used to enable/disable individual interrupt event sources.

The interrupt flag register (CAPIF) indicates if any interrupt event has been latched and contains the global interrupt flag bit (INT). An interrupt pulse is generated to the NVIC only if any of the interrupt events happens and the corresponding flag bit as well as the INT flag bit is 0. The interrupt service routine must clear the global interrupt flag bit and the serviced event via the interrupt clear register (CAPIC) before any other interrupt pulses are generated. Keeping the interrupt event flag bit as 1 prevents interrupt generation by future occurrence of the same event, while keeping the INT flag as 1 prevents interrupt generation by all future events. You can force an interrupt event via the interrupt force register (CAPIFRC).This is useful for test purposes.

Note: The CEVT0, CEVT1, CEVT2, CEVT3 flags are only active in capture mode (CAPCTL.CAPAPWM = 0). The CNT=PRD, CNT=CMP flags are only valid in APWM mode (CAPCTL.CAPAPWM = 1). CNTOVF flag is valid in both modes.

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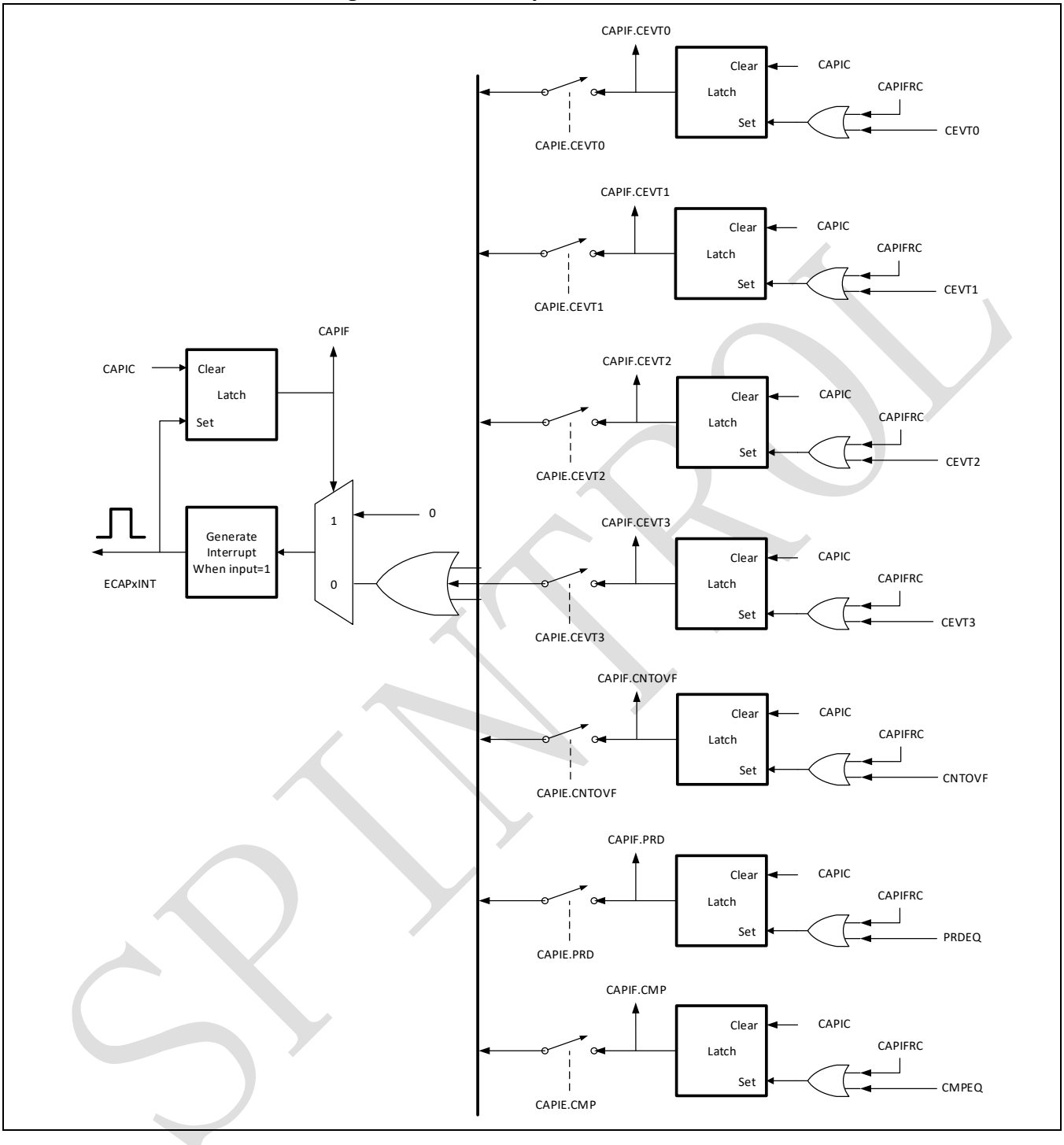
Figure 11-8: Interrupts in ECAP module



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11.4.7 Shadow load and lockout control

In capture mode, this logic inhibits (locks out) any shadow loading of CAP0 or CAP1 from APRD and ACMP registers, respectively.

In APWM mode, shadow loading is active and two choices are permitted:

- Immediate – APRD or ACMP are transferred to CAP0 or CAP1 immediately upon writing a new value.
- On period equal, i.e., CNT[31:0] = PRD[31:0]

11.5 APWM mode operation

Main operating highlights of the APWM section:

- The time-stamp counter bus is made available for comparison via 2 digital (32-bit) comparators.
- When CAP0/1 registers are not used in capture mode, their contents can be used as Period and Compare values in APWM mode.
- Double buffering is achieved via shadow registers APRD and ACMP (CAP2/3). The shadow register contents are transferred over to CAP0/1 registers either immediately upon a write, or on a CNT = PRD trigger.
- In APWM mode, writing to CAP0/CAP1 active registers will also write the same value to the corresponding shadow registers CAP2/CAP3. This emulates immediate mode. Writing to the shadow registers CAP2/CAP3 will invoke the shadow mode.
- During initialization, you must write to the active registers for both period and compare. This automatically copies the initial values into the shadow values. For subsequent compare updates, i.e., during run-time, you only need to use the shadow registers.

Figure 11-9: Active and shadow register when APWM mode

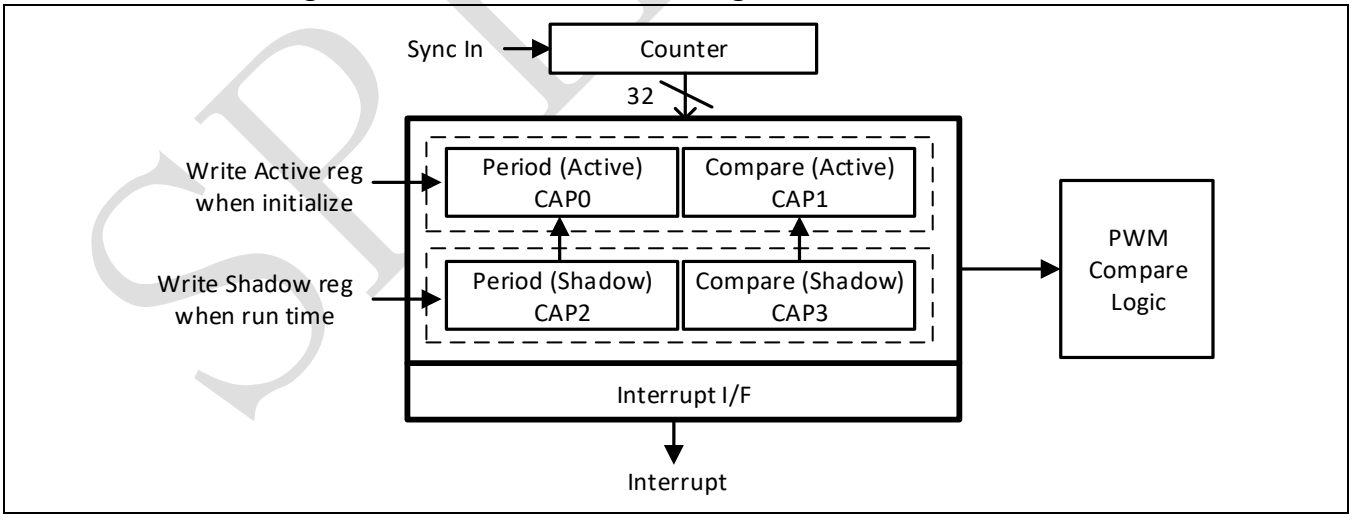

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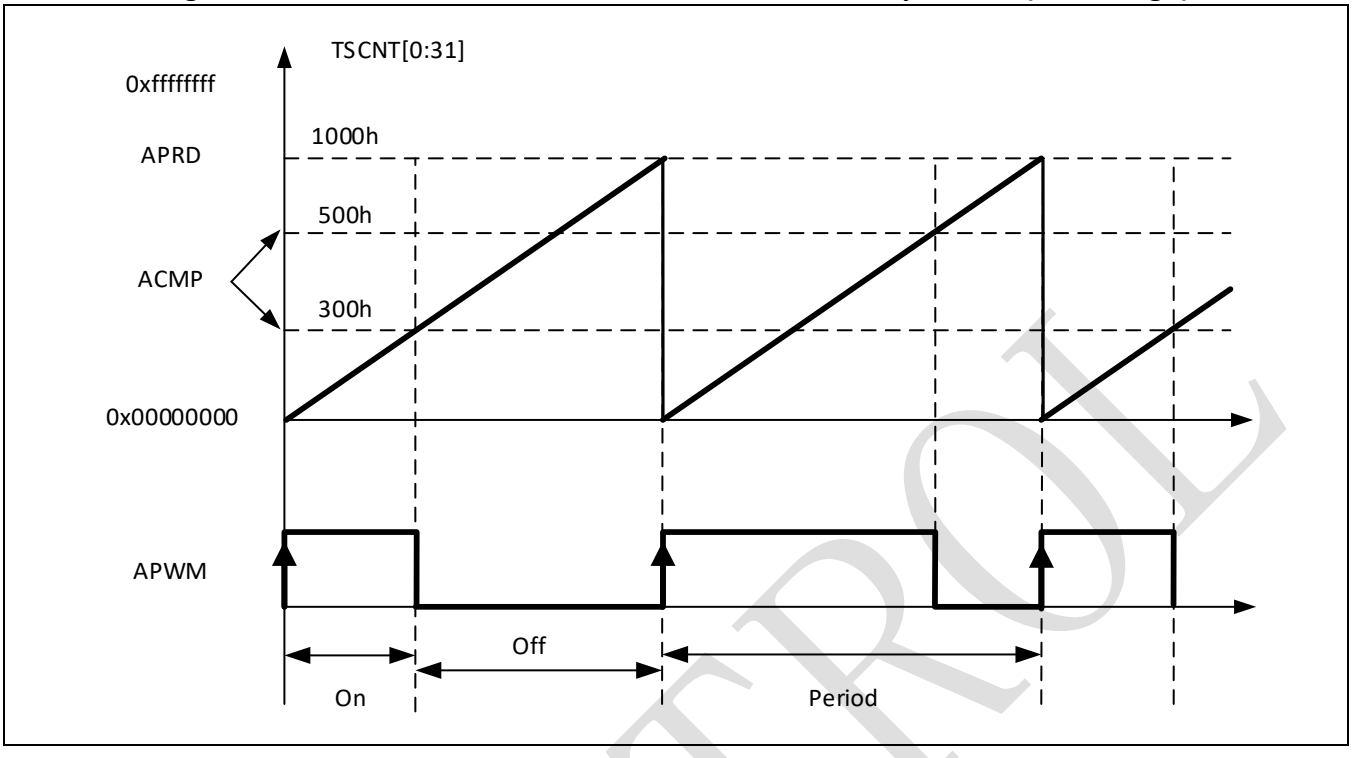
Figure 11-10: PWM waveform details Of APWM mode operation (active High)



11.6 Application of the ECAP module

The following sections will provide Applications examples and code snippets to show how to configure and operate the ECAP module. For clarity and ease of use, the examples use the SPC2168 ECAP "C" header files.

Example 1 – Absolute time-stamp operation rising edge trigger

Figure 11-11 shows an example of continuous capture operation (Mod4 counter wraps around). In this figure, TSCNT counts-up without resetting and capture events are qualified on the rising edge only, this gives period (and frequency) information.

On an event, the TSCNT contents (i.e., time-stamp) is first captured, then Mod4 counter is incremented to the next state. When the TSCNT reaches 0xFFFFFFFF (i.e. maximum value), it wraps around to 0x00000000 (not shown in Figure 11-11), if this occurs, the CNTOVF (counter overflow) flag is set, and an interrupt (if enabled) occurs. Captured Time-stamps are valid at the point indicated by the diagram, i.e. after the 4th event, hence event CEVT3 can conveniently be used to trigger an interrupt and the CPU can read data from the CAPx registers.

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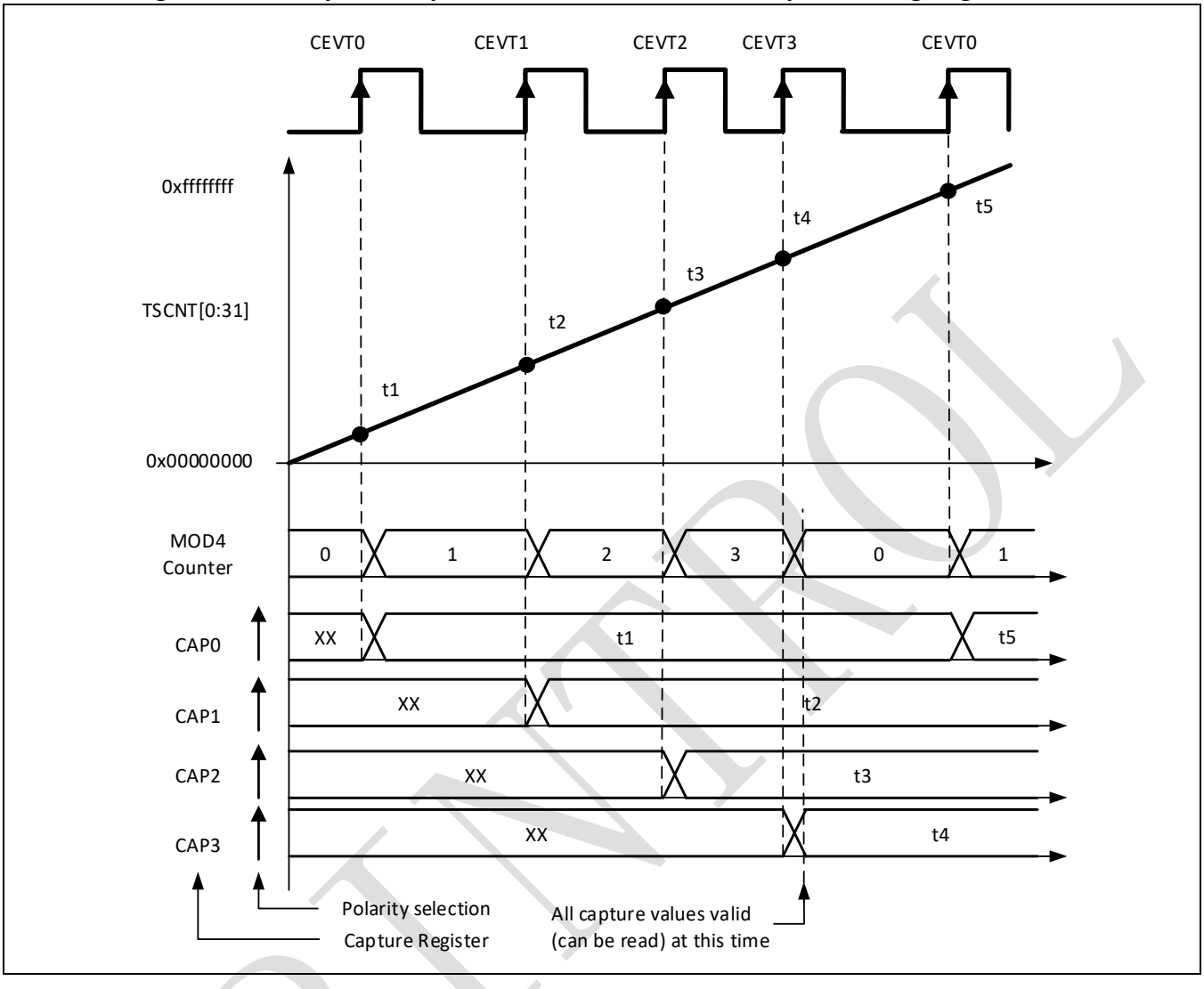
Figure 11-11: Capture sequence for absolute time-stamp and rising edge detect



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Example Code

```
// Code snippet for CAP mode Absolute Time, Rising edge trigger
// Initialization Time
//=======================
// Spintrol Co., Ltd.. All rights reserved.

ECAP->CAPCTL.bit.CAP0POL = EC_RISING;
ECAP->CAPCTL.bit.CAP1POL = EC_RISING;
ECAP->CAPCTL.bit.CAP2POL = EC_RISING;
ECAP->CAPCTL.bit.CAP3POL = EC_RISING;
ECAP->CAPCTL.bit.CNTRST0 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CNTRST1 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CNTRST2 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CNTRST3 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CAPLDEN = EC_ENABLE;
ECAP->CAPCTL.bit.EVTDIV = EC_DIV1;
ECAP->CAPCTL.bit.CAPAPWM = EC_CAP_MODE;
ECAP->CAPCTL.bit.MODE = EC_CONTINUOUS;
ECAP->CAPCTL.bit.SYNCOSEL = EC_SYNCO_DIS;
ECAP->CAPCTL.bit.SYNCIEN = EC_DISABLE;
ECAP->CAPCTL.bit.TSCNTRUN = EC_RUN; // Allow TSCNT to run

// Run Time (e.g. CEVT3 triggered ISR call)
//=========================================
TSt1 = ECAP->CAP0; // Fetch Time-Stamp captured at t1
TSt2 = ECAP->CAP1; // Fetch Time-Stamp captured at t2
TSt3 = ECAP->CAP2; // Fetch Time-Stamp captured at t3
TSt4 = ECAP->CAP3; // Fetch Time-Stamp captured at t4
Period1 = TSt2-TSt1; // Calculate 1st period
Period2 = TSt3-TSt2; // Calculate 2nd period
Period3 = TSt4-TSt3; // Calculate 3rd period
```

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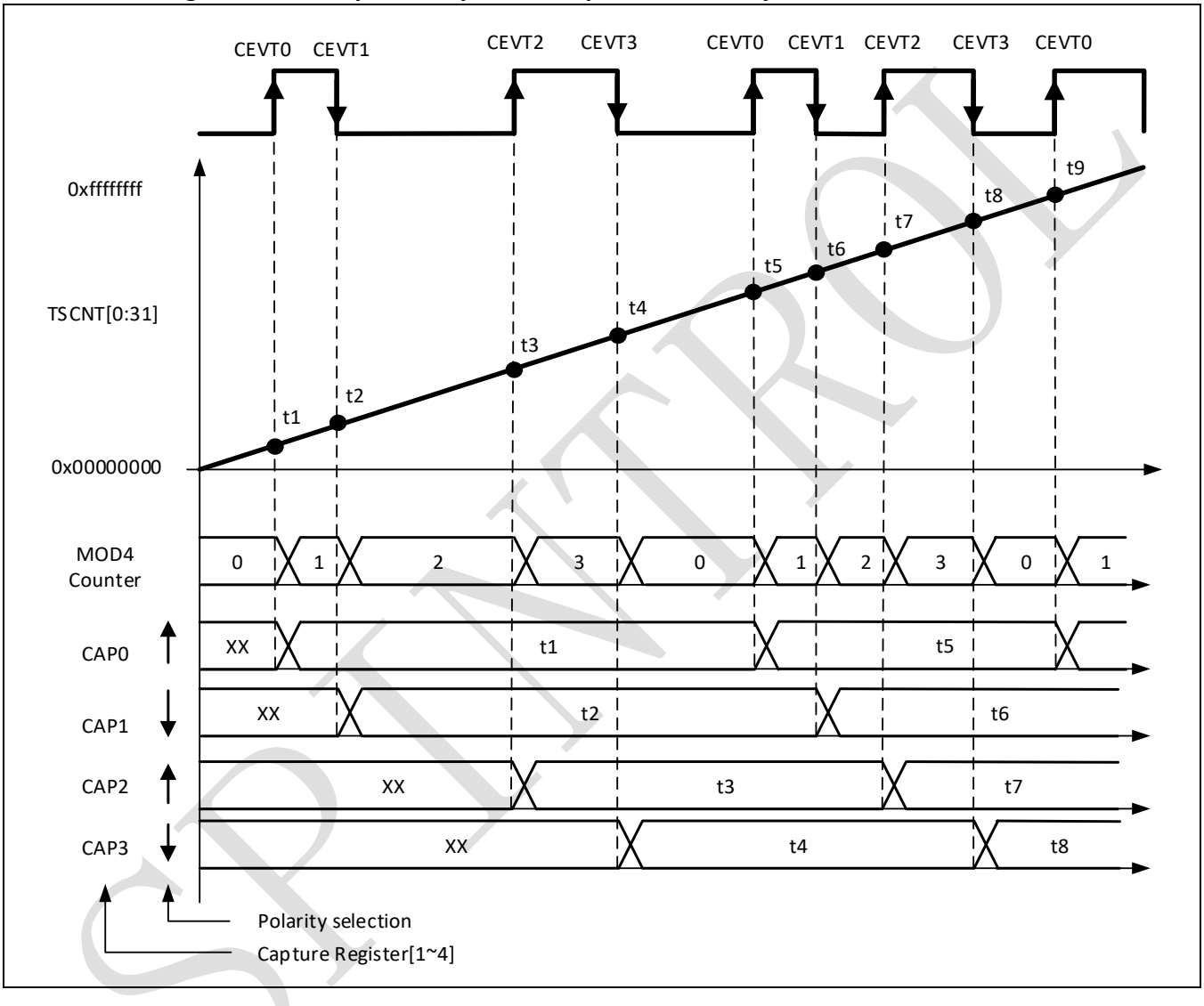
Example 2 – Absolute time-stamp operation for duty and period

The ECAP operating mode shown in Figure 11-12 is almost the same as in the previous section except capture events are qualified as either rising or falling edge, this now gives both period and duty cycle information, i.e: Period1 = $t_3 - t_1$, Period2 = $t_5 - t_3$, etc. Duty Cycle1 (on-time %) = ($t_2 - t_1$) / Period1 x 100%, etc. Duty Cycle1 (off-time %) = ($t_3 - t_2$) / Period1 x 100%, etc.

Figure 11-12: Capture sequence for period and duty without counter reset



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Example Code

```
// Initialization Time
//=======================
// Spintrol Co., Ltd.. All rights reserved.

ECAP->CAPCTL.bit.CAP0POL = EC_RISING;
ECAP->CAPCTL.bit.CAP1POL = EC_FALLING;
ECAP->CAPCTL.bit.CAP2POL = EC_RISING;
ECAP->CAPCTL.bit.CAP3POL = EC_FALLING;
ECAP->CAPCTL.bit.CNTRST0 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CNTRST1 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CNTRST2 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CNTRST3 = EC_ABS_MODE;
ECAP->CAPCTL.bit.CAPLDEN = EC_ENABLE;
ECAP->CAPCTL.bit.EVTDIV = EC_DIV1;
ECAP->CAPCTL.bit.CAPAPWM = EC_CAP_MODE;
ECAP->CAPCTL.bit.MODE = EC_CONTINUOUS;
ECAP->CAPCTL.bit.SYNCOSEL = EC_SYNCO_DIS;
ECAP->CAPCTL.bit.SYNCIEN = EC_disable;
ECAP->CAPCTL.bit.TSCNTRUN = EC_RUN; // Allow TSCNT to run

// Run Time (e.g. CEVT3 triggered ISR call)
//=========================================
TSt1 = ECAP->CAP0; // Fetch Time-Stamp captured at t1
TSt2 = ECAP->CAP1; // Fetch Time-Stamp captured at t2
TSt3 = ECAP->CAP2; // Fetch Time-Stamp captured at t3
TSt4 = ECAP->CAP3; // Fetch Time-Stamp captured at t4
Period1 = TSt3-TSt1; // Calculate 1st period
DutyOnTime1 = TSt2-TSt1; // Calculate On time
DutyOffTime1 = TSt3-TSt2; // Calculate Off time
```

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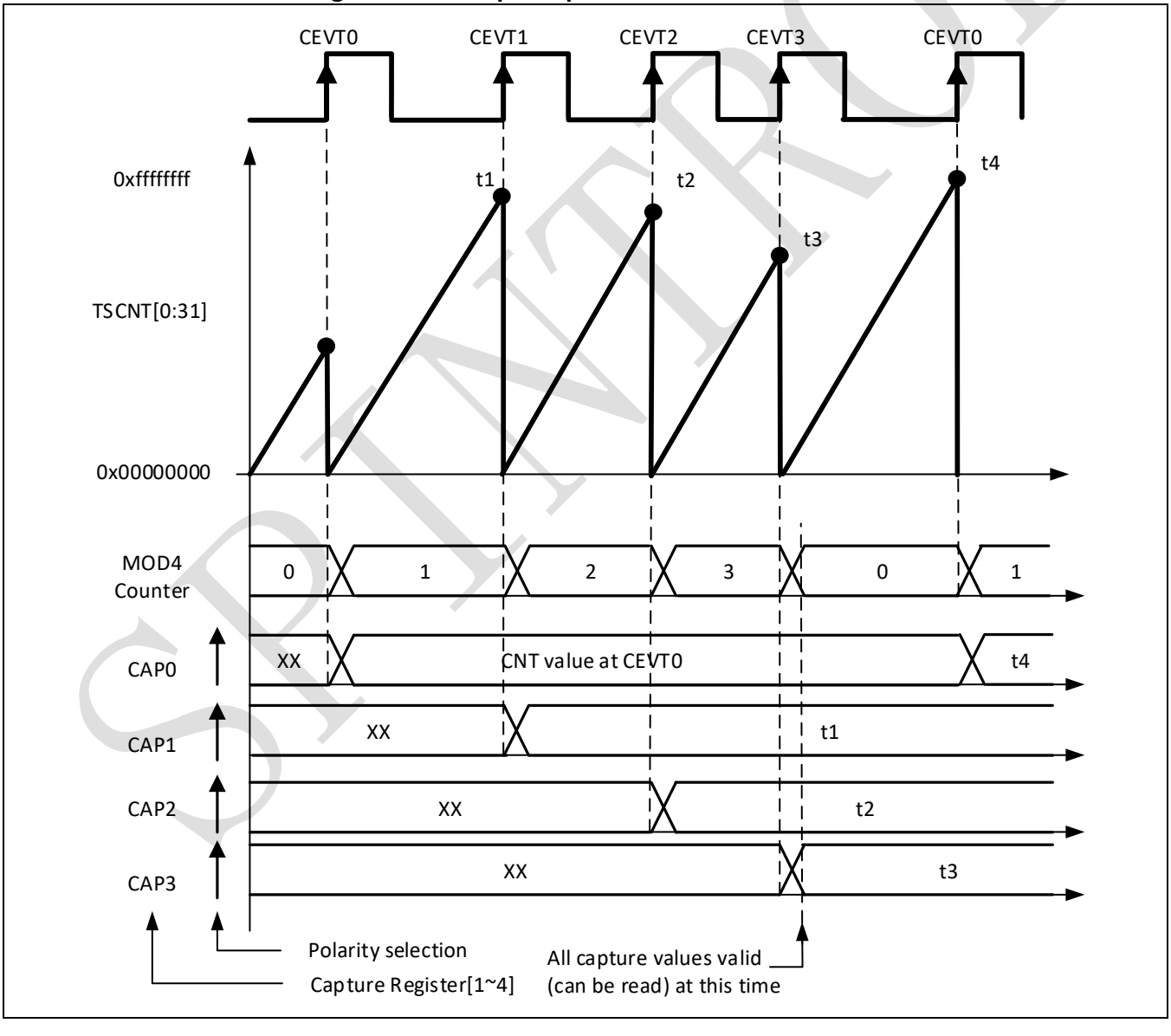
Example 3 – Time difference (Delta) operation with counter reset

Figure 11-13 shows how the ECAP module can be used to collect Delta timing data from pulse train waveforms. Here Continuous Capture mode (TSCNT counts-up without resetting, and Mod4 counter wraps around) is used. In Delta-time mode, TSCNT is reset back to Zero on every valid event. Here Capture events are qualified as rising edge only. On an event, TSCNT contents (i.e. Time-Stamp) is captured first, and then TSCNT is reset to Zero. The Mod4 counter then increments to the next state.

If TSCNT reaches 0xFFFFFFFF (i.e. Max value), before the next event, it wraps around to 0x00000000 and continues, a CNTOVF (counter overflow) Flag is set, and an Interrupt (if enabled) occurs. The advantage of Delta-time Mode is that the CAPx contents directly give timing data without the need for CPU calculations, i.e. Period1 = T_1, Period2 = T_2, etc. As shown in the diagram, the CEVT0 event is a good trigger point to read the timing data, T_1, T_2, T_3, T_4 are all valid here.

Figure 11-13: Capture period with counter reset



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Example Code

```
// Initialization Time
//=======================
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ECAP->CAPCTL.bit.CAP0POL = EC_RISING;
ECAP->CAPCTL.bit.CAP1POL = EC_RISING;
ECAP->CAPCTL.bit.CAP2POL = EC_RISING;
ECAP->CAPCTL.bit.CAP3POL = EC_RISING;
ECAP->CAPCTL.bit.CNTRST0 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CNTRST1 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CNTRST2 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CNTRST3 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CAPLDEN = EC_ENABLE;
ECAP->CAPCTL.bit.EVTDIV = EC_DIV1;
ECAP->CAPCTL.bit.CAPAPWM = EC_CAP_MODE;
ECAP->CAPCTL.bit.MODE = EC_CONTINUOUS;
ECAP->CAPCTL.bit.SYNCOSEL = EC_SYNCO_DIS;
ECAP->CAPCTL.bit.SYNCIEN = EC_disable;
ECAP->CAPCTL.bit.TSCNTRUN = EC_RUN; // Allow TSCNT to run

// Run Time (e.g. CEVT0 triggered ISR call)
//=========================================
// Note: here Time-stamp directly represents the Period value.
Period3 = ECAP->CAP0; // Fetch Time-Stamp captured at T1
Period0 = ECAP->CAP1; // Fetch Time-Stamp captured at T2
Period1 = ECAP->CAP2; // Fetch Time-Stamp captured at T3
Period2 = ECAP->CAP3; // Fetch Time-Stamp captured at T4
```

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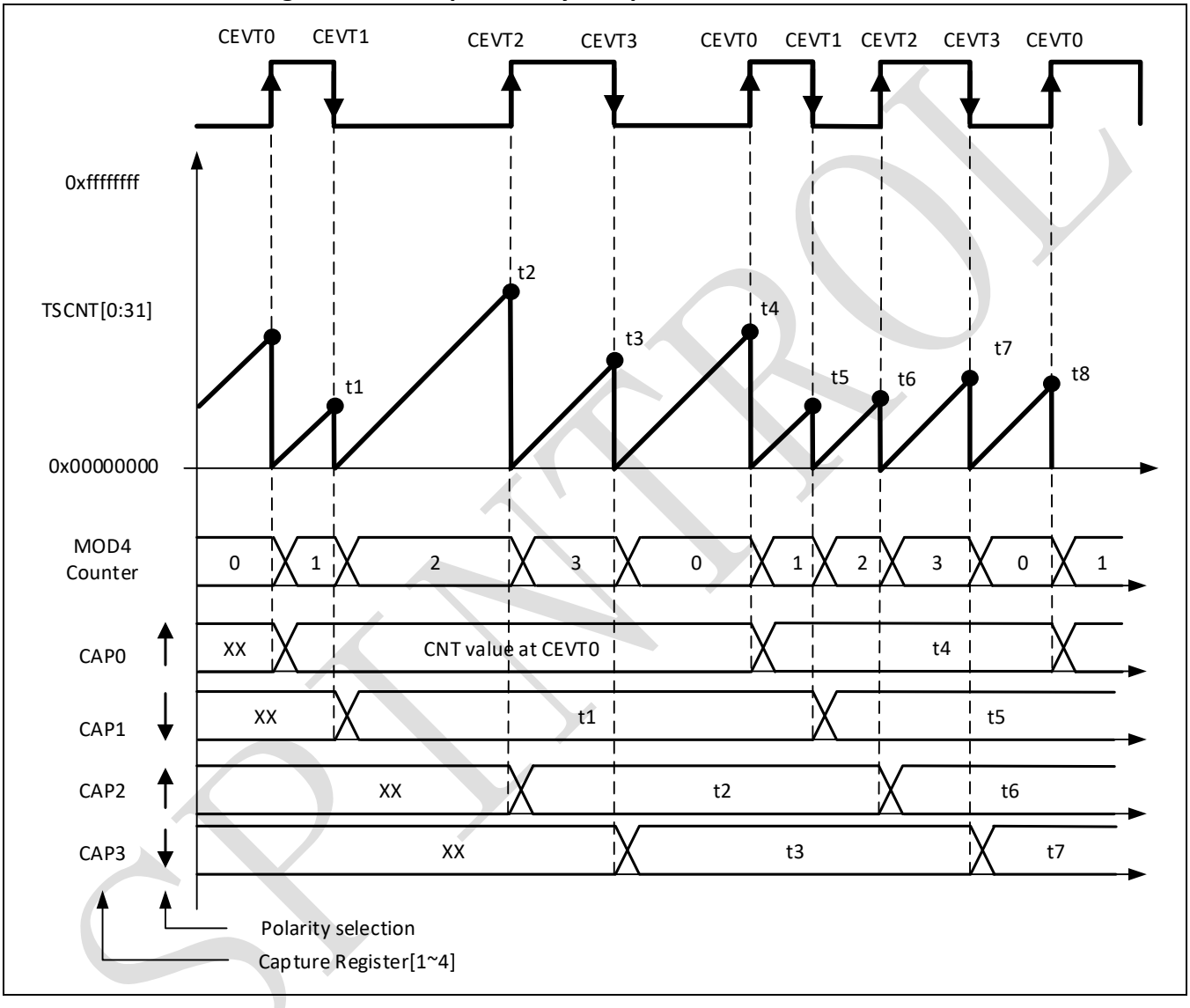
Example 4 – Time difference operation rising and falling edge trigger

In Figure 11-14 the ECAP operating mode is almost the same as in previous section except Capture events are qualified as either Rising or Falling edge, this now gives both Period and Duty cycle information, i.e:Period1 = T_1+T_2, Period2 = T_3+T_4,etc Duty Cycle1 (on-time %) = T_1 / Period1 x 100%, etc Duty Cycle1(off-time %) = T_2 / Period1 x 100%, etc.

Figure 11-14: Capture duty and period with counter reset



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Example Code

```
// Initialization Time
//=======================
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ECAP->CAPCTL.bit.CAP0POL = EC_RISING;
ECAP->CAPCTL.bit.CAP1POL = EC_FALLING;
ECAP->CAPCTL.bit.CAP2POL = EC_RISING;
ECAP->CAPCTL.bit.CAP3POL = EC_FALLING;
ECAP->CAPCTL.bit.CNTRST0 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CNTRST1 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CNTRST2 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CNTRST3 = EC_DELTA_MODE;
ECAP->CAPCTL.bit.CAPLDEN = EC_ENABLE;
ECAP->CAPCTL.bit.EVTDIV = EC_DIV1;
ECAP->CAPCTL.bit.CAPAPWM = EC_CAP_MODE;
ECAP->CAPCTL.bit.MODE = EC_CONTINUOUS;
ECAP->CAPCTL.bit.SYNCOSEL = EC_SYNCO_DIS;
ECAP->CAPCTL.bit.SYNCIEN = EC_disable;
ECAP->CAPCTL.bit.TSCNTRUN = EC_RUN; // Allow TSCNT to run

// Run Time (e.g. CEVT0 triggered ISR call)
//=========================================
// Note: here Time-stamp directly represents the Duty cycle values.
DutyOnTime1 = ECAP->CAP1; // Fetch Time-Stamp captured at T2
DutyOffTime1 = ECAP->CAP2; // Fetch Time-Stamp captured at T3
DutyOnTime2 = ECAP->CAP3; // Fetch Time-Stamp captured at T4
DutyOffTime2 = ECAP->CAP0; // Fetch Time-Stamp captured at T1
Period1 = DutyOnTime1 + DutyOffTime1;
Period2 = DutyOnTime2 + DutyOffTime2;
```

SPINTROL

11.7 Registers

11.7.1 ECAP register map

Table 11-1: ECAP Module Base Address

Peripheral Module	Base Address
ECAP	0x4000 A000

Table 11-2: ECAP Register Map

Register	Offset	Description	Reset Value
CAPSRCCTL	0x00	Capture Source Input Control Register	0x0000007F
CAPSYNCICTL	0x04	Capture Synchronization Source Input Control Register	0x0000007F
CAPTSCNT	0x08	Time-Stamp Counter Register	0x00000000
CAPCNTPHS	0x0C	Counter Phase Offset Value Register	0x00000000
CAP0	0x10	Capture Register 0	0x00000000
CAP1	0x14	Capture Register 1	0x00000000
CAP2	0x18	Capture Register 2	0x00000000
CAP3	0x1C	Capture Register 3	0x00000000
CAPCTL	0x20	Capture Control Register	0x000C0000
CAPIF	0x24	Capture Interrupt Flag Register	0x00000000
CAPIE	0x28	Capture Interrupt Enable Register	0x00000000
CAPIC	0x2C	Capture Interrupt Clear Register	0x00000000
CAPIFRC	0x30	Capture Interrupt Force Register	0x00000000
CAPREGKEY	0x34	Capture Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the CAPREGKEY=0x1ACCE551.

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11.7.2 ECAP registers

11.7.2.1 Capture Source Input Control Register (CAPSRCCTL)

Table 11-3: Capture Source Input Control Register (CAPSRCCTL) Layout

CAPSRCCTL (Capture Source Input Control Register) Offset: 0x0 Default: 0x0000007F Access: ECAP -> CAPSRCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 11-4: Capture Source Input Control Register (CAPSRCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	Source input polarity 0: Active low 1: Active high
5:0	IOSEL	RW	0x3F	GPIO number to be selected as capture input

11.7.2.2 Capture Synchronization Source Input Control Register (CAPSYNCICTL)

Table 11-5: Capture Synchronization Source Input Control Register (CAPSYNCICTL) Layout

CAPSYNCICTL (Capture Synchronization Source Input Control Register) Offset: 0x4 Default: 0x0000007F Access: ECAP -> CAPSYNCICTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 11-6: Capture Synchronization Source Input Control Register (CAPSYNCICTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	Source input polarity 0: Active low 1: Active high
5:0	IOSEL	RW	0x3F	GPIO number to be selected as sync input

SPINTROL

11.7.2.3 Time-Stamp Counter Register (CAPTSCNT)

Table 11-7: Time-Stamp Counter Register (CAPTSCNT) Layout

CAPTSCNT (Time-Stamp Counter Register) Offset: 0x8 Default: 0x00000000 Access: ECAP -> CAPTSCNT.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 11-8: Time-Stamp Counter Register (CAPTSCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Active 32-bit counter register that is used as the capture time-base.

11.7.2.4 Counter Phase Offset Value Register (CAPCNTPHS)

Table 11-9: Counter Phase Offset Value Register (CAPCNTPHS) Layout

CAPCNTPHS (Counter Phase Offset Value Register) Offset: 0xC Default: 0x00000000 Access: ECAP -> CAPCNTPHS.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 11-10: Counter Phase Offset Value Register (CAPCNTPHS) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Counter phase value register that can be programmed for phase lag/lead.

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11.7.2.5 Capture Register 0 (CAP0)

Table 11-11: Capture Register 0 (CAP0) Layout

CAP0 (Capture Register 0) Offset: 0x10 Default: 0x00000000 Access: ECAP -> CAP0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 11-12: Capture Register 0 (CAP0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	This register can be loaded by: – Time-Stamp(i.e., counter value) during a capture event – Software – may be useful for test purposes – PRD active value from shadow register(i.e., CAP2) when used in APWM mode NOTE: In APWM mode, writing to CAP0/CAP1 active registers also writes the same value to the corresponding shadow registers CAP2/CAP3. This emulates immediate mode. Writing to the shadow registers CAP2/CAP3 invokes the shadow mode.

SPINTROL

11.7.2.6 Capture Register 1 (CAP1)

Table 11-13: Capture Register 1 (CAP1) Layout

CAP1 (Capture Register 1) Offset: 0x14 Default: 0x00000000 Access: ECAP -> CAP1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 11-14: Capture Register 1 (CAP1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	This register can be loaded by: – Time-Stamp(i.e., counter value) during a capture event – Software – may be useful for test purposes – CMP active value from shadow register(i.e., CAP3) when used in APWM mode NOTE: In APWM mode, writing to CAP0/CAP1 active registers also writes the same value to the corresponding shadow registers CAP2/CAP3. This emulates immediate mode. Writing to the shadow registers CAP2/CAP3 invokes the shadow mode.

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11.7.2.7 Capture Register 2 (CAP2)

Table 11-15: Capture Register 2 (CAP2) Layout

CAP2 (Capture Register 2) Offset: 0x18 Default: 0x00000000 Access: ECAP -> CAP2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 11-16: Capture Register 2 (CAP2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	In capture mode, it is a time-stamp capture register. In APWM mode, this is the period shadow(PRD) register. You update the PWM period value through this register. In this mode, CAP2(APRD) shadows CAP0.

11.7.2.8 Capture Register 3 (CAP3)

Table 11-17: Capture Register 3 (CAP3) Layout

CAP3 (Capture Register 3) Offset: 0x1C Default: 0x00000000 Access: ECAP -> CAP3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 11-18: Capture Register 3 (CAP3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	In capture mode, this is a time-stamp capture register. In APWM mode, this is the compare shadow(CMP) register. You update the PWM compare value via this register. In this mode, CAP3(ACMP) shadows CAP1.

SPINTROL

11.7.2.9 Capture Control Register (CAPCTL)

Table 11-19: Capture Control Register (CAPCTL) Layout

CAPCTL (Capture Control Register) Offset: 0x20 Default: 0x000C0000
Access: ECAP -> CAPCTL.all

31	30	29	28	27	26	25	24
RESERVED		DBGRUN		APWMPOL	APWMMODE	FRCSYNC	SYNCOSEL
23	22	21	20	19	18	17	16
SYNCOSEL	PHSEN	TSCNTRUN	REARM	STOPWRAP		ONESHOT	EVTDIV
15	14	13	12	11	10	9	8
EVTDIV							CAPLDEN
7	6	5	4	3	2	1	0
CNTRST3	CAP3POL	CNTRST2	CAP2POL	CNTRST1	CAP1POL	CNTRST0	CAP0POL

Table 11-20: Capture Control Register (CAPCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29:28	DBGRUN	RW	0x0	ECAP counter 358rotocol when CPU is halted Note: Debug operation and CPU fault exceptions both can cause CPU halted. 00: Counter stops immediately when CPU is lockup or halted 01: Counter runs until CAPTSCNT=0 when CPU is lockup or halted 1x: Counter is unaffected when CPU is lockup or halted
27	APWMPOL	RW	0x0	APWM output polarity select. This is applicable only in APWM operating mode. 0: Output is active low (i.e., Compare value defines low time) 1: Output is active high (i.e., Compare value defines high time)
26	APWMMODE	RW	0x0	CAP/APWM operating mode select 0: ECAP module operates in capture mode. This mode forces the following configuration: – Inhibits CAPTSCNT resets via CNT = PRD event – Inhibits shadow loads on CAP0 and CAP1 registers – Permits user to enable CAP0-3 register load – CAPx/APWMx pin operates as a capture input 1: ECAP module operates in APWM mode. This mode forces the following configuration: – Resets CAPTSCNT on CNT = PRD event – Permits shadow loading on CAP0 and CAP1 registers – Disables loading of time-stamps into CAP0-3

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Bits	Field Name	Type	Reset	Description
				registers – CAPx/APWMx pin operates as a APWM output
25	FRCSYNC	W1S	0x0	Software-forced counter synchronizing. 0: Writing a 0 has no effect and always read back 0. 1: Writing a 1 force load from CAPCNTPHS to CAPTSCNT. This bit is self-cleared to 0
24:23	SYNCOSEL	RW	0x0	Sync-out Select 0x: Disable sync-out signal 10: Select sync-in event to be the sync-out signal (pass through) 11: Select CNT = PRD event to be the sync-out signal
22	PHSEN	RW	0x0	Phase synchronization enable 0: Disable synchronization 1: Enable counter (CAPTSCNT) to be loaded from CAPCNTPHS register upon either a SYNCI signal or a S/W force event
21	TSCNTRUN	RW	0x0	Time stamp counter run/stop control 0: Counter stopped 1: Couter is free-running
20	REARM	W1S	0x0	One-shot re-arming control In one-shot mode, further interrupt events are blocked until re-armed. 0: Write a 0 has no effect and always reads back 0. 1: Arms the one-shot sequence as follows: 1) Reset the MOD4 counter to zero 2) Unfreeze the MOD4 counter 3) Enable capture register loads
19:18	STOPWRAP	RW	0x3	Stop value for one-shot mode and wrap value for continuous mode. When STOPWRAP is equal to MOD4 counter – MOD4 counter is stopped (frozen) – Capture register loads are inhibited 00: Stop after event 0 in one-shot mode. Wrap after event 0 in continuous mode. 01: Stop after event 1 in one-shot mode. Wrap after event 1 in continuous mode. 10: Stop after event 2 in one-shot mode. Wrap after event 2 in continuous mode.

SPINTROL

Bits	Field Name	Type	Reset	Description
				11: Stop after event 3 in one-shot mode. Wrap after event 3 in continuous mode.
17	ONESHOT	RW	0x0	One-shot mode enable. This bit is applicable only in capture mode. 0: Operate in continuous mode 1: Operate in one-shot mode
16:9	EVTDIV	RW	0x0	Event filter prescale select Event is scaled down by (EVTDIV+1)
8	CAPLDEN	RW	0x0	Enable CAP0 ~ CAP3 loading upon a capture event 0: Disable 1: Enable
7	CNTRST3	RW	0x0	Counter reset on capture event 3 0: Do not reset counter on capture event 3 (Absolute time stamp operation) 1: Reset counter on capture event 3 (Relative time difference operation)
6	CAP3POL	RW	0x0	Capture event 3 polarity select 0: Capture event 3 is triggered on a falling edge 1: Capture event 3 is triggered on a rising edge
5	CNTRST2	RW	0x0	Counter reset on capture event 2 0: Do not reset counter on capture event 2 (Absolute time stamp operation) 1: Reset counter on capture event 2 (Relative time difference operation)
4	CAP2POL	RW	0x0	Capture event 2 polarity select 0: Capture event 2 is triggered on a falling edge 1: Capture event 2 is triggered on a rising edge
3	CNTRST1	RW	0x0	Counter reset on capture event 1 0: Do not reset counter on capture event 1 (Absolute time stamp operation) 1: Reset counter on capture event 1 (Relative time difference operation)
2	CAP1POL	RW	0x0	Capture event 1 polarity select 0: Capture event 1 is triggered on a falling edge 1: Capture event 1 is triggered on a rising edge
1	CNTRST0	RW	0x0	Counter reset on capture event 0 0: Do not reset counter on capture event 0 (Absolute time stamp operation)

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Bits	Field Name	Type	Reset	Description
				1: Reset counter on capture event 0 (Relative time difference operation)
0	CAP0POL	RW	0x0	Capture event 0 polarity select 0: Capture event 0 is triggered on a falling edge 1: Capture event 0 is triggered on a rising edge

SPINTROL

11.7.2.10 Capture Interrupt Flag Register (CAPIF)

Table 11-21: Capture Interrupt Flag Register (CAPIF) Layout

CAPIF (Capture Interrupt Flag Register) Offset: 0x24 Default: 0x00000000 Access: ECAP -> CAPIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
INT	CMP	PRD	CNTOVF	CEVT3	CEVT2	CEVT1	CEVT0

Table 11-22: Capture Interrupt Flag Register (CAPIF) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	INT	RO	0x0	Global interrupt flag 0: Interrupt does not occur 1: Interrupt occurred. Futher interrupt will not be generated until this bit is cleared.
6	CMP	RO	0x0	Counter comparison equal flag. This flag is active only in APWM mode. 0: Event does not occur 1: Event occurred. Futher event is ignored until this bit is cleared.
5	PRD	RO	0x0	Counter equal period flag. This flag is only active in APWM mode. 0: Event does not occur 1: Event occurred. Futher event is ignored until this bit is cleared.
4	CNTOVF	RO	0x0	Counter overflow status Flag. This flag is active in CAP and APWM mode. 0: Event does not occur 1: Event occurred. Futher event is ignored until this bit is cleared.
3	CEVT3	RO	0x0	Capture event 3 flag. This flag is only active in CAP mode. 0: Event does not occur 1: Event occurred. Futher event is ignored until this bit is cleared.
2	CEVT2	RO	0x0	Capture event 2 flag. This flag is active only in CAP mode.

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Bits	Field Name	Type	Reset	Description
				0: Event does not occur 1: Event occurred. Futher event is ignored until this bit is cleared.
1	CEVT1	RO	0x0	Capture event 1 flag. This flag is only active in CAP mode. 0: Event does not occur 1: Event occurred. Futher event is ignored until this bit is cleared.
0	CEVT0	RO	0x0	Capture event 0 flag. This flag is only active in CAP mode. 0: Event does not occur 1: Event occurred. Futher event is ignored until this bit is cleared.

SPINTROL

11.7.2.11 Capture Interrupt Enable Register (CAPIE)

Table 11-23: Capture Interrupt Enable Register (CAPIE) Layout

CAPIE (Capture Interrupt Enable Register) Offset: 0x28 Default: 0x00000000 Access: ECAP -> CAPIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	CMP	PRD	CNTOVF	CEVT3	CEVT2	CEVT1	CEVT0

Table 11-24: Capture Interrupt Enable Register (CAPIE) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	CMP	RW	0x0	Counter comparison equal interrupt enable 0: Disable 1: Enable
5	PRD	RW	0x0	Counter equal period interrupt enable 0: Disable 1: Enable
4	CNTOVF	RW	0x0	Counter overflow interrupt enable 0: Disable 1: Enable
3	CEVT3	RW	0x0	Capture event 3 interrupt enable 0: Disable 1: Enable
2	CEVT2	RW	0x0	Capture event 2 interrupt enable 0: Disable 1: Enable
1	CEVT1	RW	0x0	Capture event 1 interrupt enable 0: Disable 1: Enable
0	CEVT0	RW	0x0	Capture event 0 interrupt enable 0: Disable 1: Enable

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11.7.2.12 Capture Interrupt Clear Register (CAPIC)

Table 11-25: Capture Interrupt Clear Register (CAPIC) Layout

CAPIC (Capture Interrupt Clear Register) Offset: 0x2C Default: 0x00000000 Access: ECAP -> CAPIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
INT	CMP	PRD	CNTOVF	CEVT3	CEVT2	CEVT1	CEVT0

Table 11-26: Capture Interrupt Clear Register (CAPIC) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	INT	W1C	0x0	Global interrupt clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.
6	CMP	W1C	0x0	Counter comparison equal flag clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.
5	PRD	W1C	0x0	Counter equal to period flag clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.
4	CNTOVF	W1C	0x0	Counter overflow flag clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.
3	CEVT3	W1C	0x0	Capture event 3 flag clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.
2	CEVT2	W1C	0x0	Capture event 2 flag clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.
1	CEVT1	W1C	0x0	Capture event 1 flag clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.
0	CEVT0	W1C	0x0	Capture event 0 flag clear 0: Writing a 0 has no effect and always readback 0. 1: Writing a 1 clears flag. This bit is self-cleared to 0.

SPINTROL

11.7.2.13 Capture Interrupt Force Register (CAPIFRC)

Table 11-27: Capture Interrupt Force Register (CAPIFRC) Layout

CAPIFRC (Capture Interrupt Force Register) Offset: 0x30 Default: 0x00000000 Access: ECAP -> CAPIFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	CMP	PRD	CNTOVF	CEVT3	CEVT2	CEVT1	CEVT0

Table 11-28: Capture Interrupt Force Register (CAPIFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	CMP	W1S	0x0	Counter comparison equal flag force 0: Writing a 0 has no effect and always read back 0 1: Writing a 1 forces flag. This bit is self-cleared to 0.
5	PRD	W1S	0x0	Counter equal to period flag force 0: Writing a 0 has no effect and always read back 0 1: Writing a 1 forces flag. This bit is self-cleared to 0.
4	CNTOVF	W1S	0x0	Counter overflow flag force 0: Writing a 0 has no effect and always read back 0 1: Writing a 1 forces flag. This bit is self-cleared to 0.
3	CEVT3	W1S	0x0	Capture event 3 flag force 0: Writing a 0 has no effect and always read back 0 1: Writing a 1 forces flag. This bit is self-cleared to 0.
2	CEVT2	W1S	0x0	Capture event 2 flag force 0: Writing a 0 has no effect and always read back 0 1: Writing a 1 forces flag. This bit is self-cleared to 0.
1	CEVT1	W1S	0x0	Capture event 1 flag force 0: Writing a 0 has no effect and always read back 0 1: Writing a 1 forces flag. This bit is self-cleared to 0.
0	CEVT0	W1S	0x0	Capture event 0 flag force 0: Writing a 0 has no effect and always read back 0 1: Writing a 1 forces flag. This bit is self-cleared to 0.

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11.7.2.14 Capture Register Write-Allow Key Register (CAPREGKEY)

Table 11-29: Capture Register Write-Allow Key Register (CAPREGKEY) Layout

CAPREGKEY (Capture Register Write-Allow Key Register) Offset: 0x34 Default: 0x1ACCE551 Access: ECAP -> CAPREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 11-30: Capture Register Write-Allow Key Register (CAPREGKEY) Filed Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected capture registers

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12 ADC

12.1 ADC overview

The SPC2168 implements a 14-bit successive approximation A/D converter (SAR-ADC). There are triple sample and hold circuits in front of ADC. The sample and hold circuits can be sampled sequentially or simultaneously. There are 20 analog input channels to ADC. The converter can be configured with an internal bandgap reference or an external voltage reference.

This ADC is easy for the user to create a series of conversions from a single trigger. The basic principle of operation is based on the configurations of individual conversions, called SOC's, or State-Of-Conversions.

Functions of the ADC module include:

- 14-bit resolution ADC core with built-in triple sample-and-hold (S/H)
  - Up to 4 Million samples per second (Msps)
  - Up to 20-channel, multiplexed inputs
- Support 3 channel simultaneous sampling
- Analog full scale input: 3.657 V fixed, or an external voltage reference ratio-metric from GPIO12
- 16 SOC's, configurable trigger source, sampling mode, channel selection, averaging time and sample time
- 16 result registers (individually addressable) to store conversion values
- Multiple trigger sources
  - Software immediate start
  - Timer 0/1/2
  - GPIO external interrupt
  - PWMxSOCA, PWMxSOCB and PWMxSOCC (x=0~7) with configurable timing
- 16 independent interrupt signals with 16 independent NVIC interrupts, can configure interrupt request after any conversion

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12.2 ADC architecture

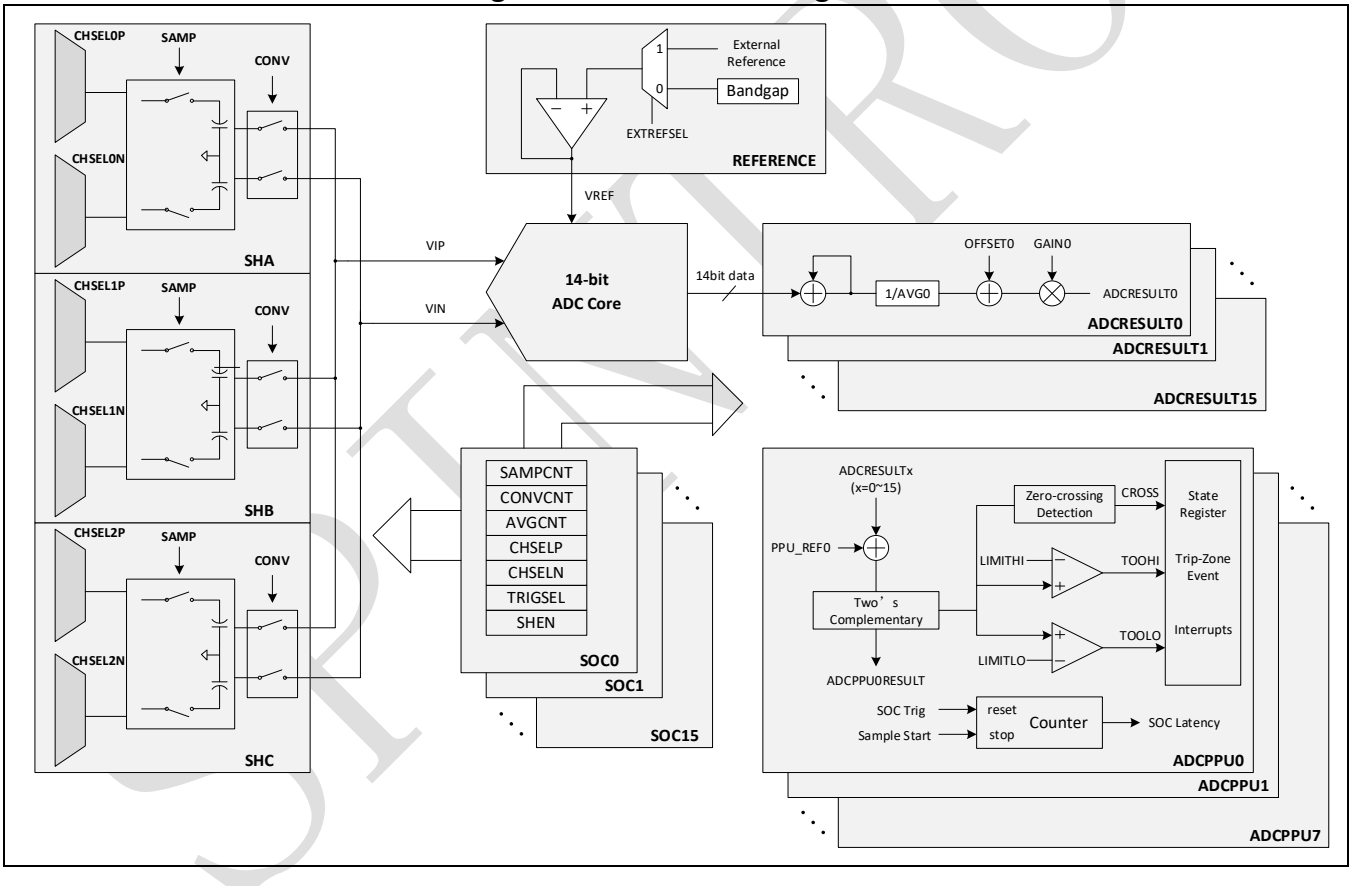
As shown in Figure 12-1, the ADC analog circuit includes:

- 3 ADC samplers (SHA, SHB, SHC)
- 1 ADC Core
- ADC reference, as well as other analog supporting circuits

The digital circuit includes:

- 16 SOC configuration control
- 16 ADC result modules (ADCRESULT) with averaging, gain and offset calibration
- 8 post-processing units (PPU)
- Interface to other on-chip modules (not showed in diagram)

Figure 12-1: ADC block diagram



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12.3 SOC principle of operation

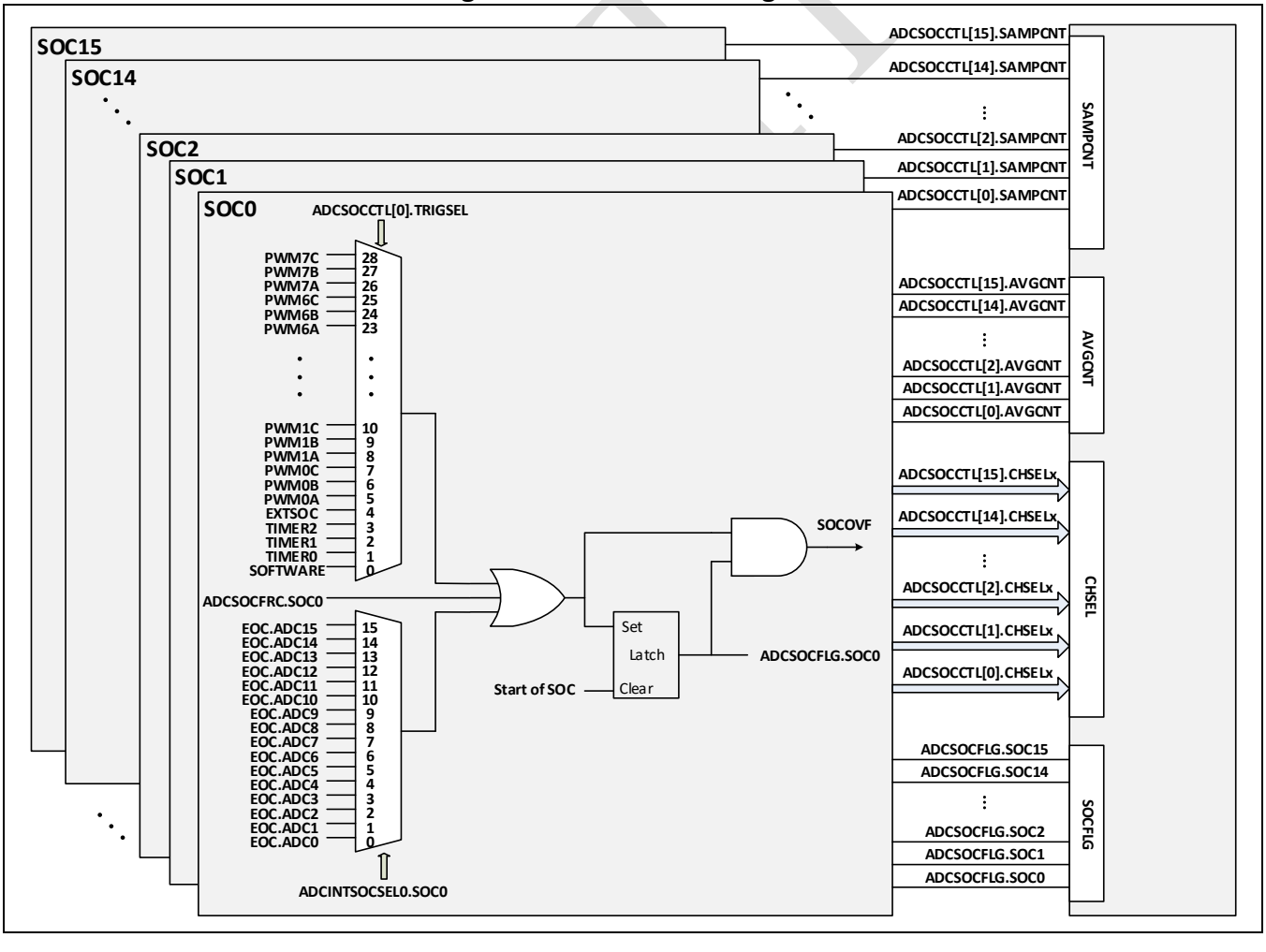
This ADC is SOC-based. The term SOC means a configuration set defining a single conversion. In one SOC there are four configurations: the trigger source that starts the conversion, the channel selection, the average times and the windows size of sample control. In additional, the sampling mode control also is set in SOC which is described in Section 12.3.2. As showed in Figure 12-2, each SOC is independently configured and can have any combination of the trigger, channel selection, averaging times and sample window size available. Multiple SOC's can be configured for the same trigger, channel selection, averaging times and sample window size as desired. It can be implemented for individual samples of different channels with different triggers, or to oversample the same channel using a single trigger, or to create a series of conversions of different channels all from a single trigger.

The trigger source for SOCx is configured by a combination of the TRIGSEL field in the ADCSOCCTL[x] register and the appropriate bits in the ADCINTSOCSEL0~1 register. Software can also force an SOC event with the ADCSOCFRC register.

The channel selection is configured by a combination of SHEN and CHSELx (x=P or N) field in ADCSOCCTL[x] register.

The sample time for SOCx are configured with SAMPCNT fields in ADCSOCCTL[x] register respectively.

Figure 12-2: SOC block diagram



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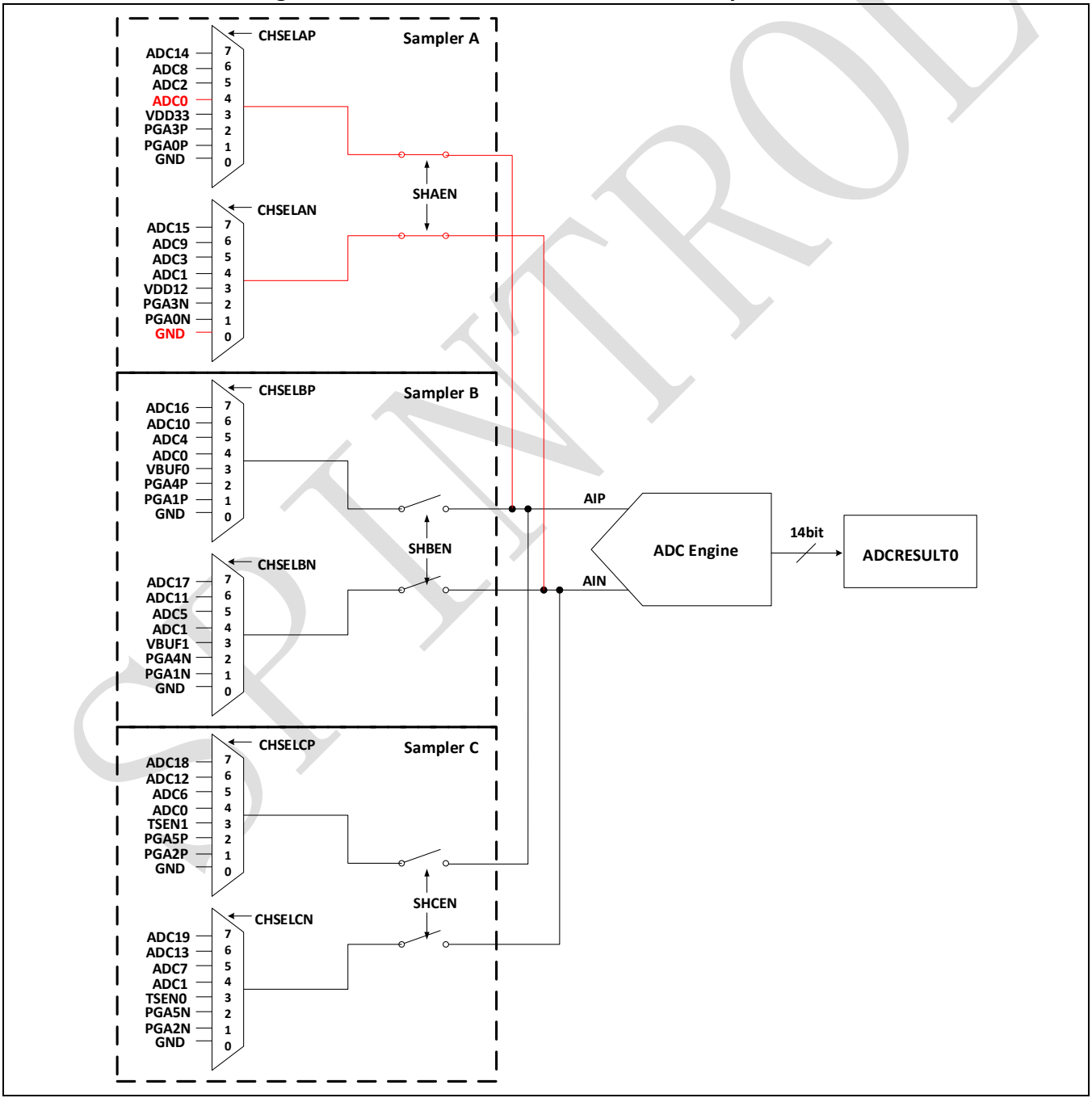
Example 12.3.1 PWMSOC1A trigger SOC0 to convert ADC0

To configure a single conversion on channel ADC0 to occur when the PWM1SOCA timer reaches its period match, one must first setup PWM1SOCA to output an SOC signal on a period match. Let's configure one of the SOC's using its ADCSOCCTL[x] register. It makes no difference which SOC to choose, so as an example use SOC0. Setting PWMSOC1A for the SOC0 trigger source, select averaging is 4 times, selecting channel ADC0 to convert and choosing 4 cycles and 4 cycles for the sample and convert time. So we'll set the TRIGSEL field to 8, the AVGCNT field to 2(power 2 based), the SHEN=1(only Sampler A on work), CHSELP to 4 (ADC0), the CHSELN to 0 (GND), the SAMPCNT field to 3, the CONVCNT field to 3, respectively.

Figure 12-3: ADC channel selection for Example 12.3.1



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It can be divided in to the followed lines:

Example 12.3.1

```
void   ADC_Example12_3_1(void)
{
   ADC->ADCSOCCTL[0].bit.SHEN        = 1;/* Enable Sampler A                          */
   ADC->ADCSOCCTL[0].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[0].bit.CHSELP    = 4;/* Sampler A Positive = ADC0                */
   ADC->ADCSOCCTL[0].bit.CHSELN    = 0;/* Sampler A Negative = GND                 */
   ADC->ADCSOCCTL[0].bit.AVGCNT    = 2;/* Averaging 4 times (2^2)                  */
   ADC->ADCSOCCTL[0].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock        */
   ADC->ADCSOCCTL[0].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock     */
}
```

Assume that ADC clock is 32MHz, 31.25ns for one cycle. So the fastest configuration are 125ns sampling time (SAMPCNT=3) and 156.25ns conversion time (CONVCNT=4). Single conversion of ADC0 will be started on a PWM1SOCA event with the resulting value stored in the ADCRESULT[0] register. In this example, we use positive input as ADC channel and negative input as GND. That means the differential input sign is plus. Alternately, we can also use positive input as GND and use negative input as ADC channel. That means the differential input sign is minus.

Example 12.3.2 Oversample ADC0

If ADC0 needed to be oversampled by 3X, then SOC1 and SOC2 could all be given the same configuration as SOC0.

Example 12.3.2

```
void   ADC_Example12_3_2(void)
{
   ADC->ADCSOCCTL[0].bit.SHEN        = 1;/* Enable Sampler A                          */
   ADC->ADCSOCCTL[0].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[0].bit.CHSELP    = 4;/* Sampler A Positive = ADC0                */
   ADC->ADCSOCCTL[0].bit.CHSELN    = 0;/* Sampler A Negative = GND                 */
   ADC->ADCSOCCTL[0].bit.AVGCNT    = 2;/* Averaging 4 times (2^2)                  */
   ADC->ADCSOCCTL[0].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock        */
   ADC->ADCSOCCTL[0].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock     */

   ADC->ADCSOCCTL[1].bit.SHEN        = 1;/* Enable Sampler A                          */
   ADC->ADCSOCCTL[1].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[1].bit.CHSELP    = 4;/* Sampler A Positive = ADC0                */
   ADC->ADCSOCCTL[1].bit.CHSELN    = 0;/* Sampler A Negative = GND                 */
   ADC->ADCSOCCTL[1].bit.AVGCNT    = 2;/* Averaging 4 times (2^2)                  */
   ADC->ADCSOCCTL[1].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock        */
   ADC->ADCSOCCTL[1].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock     */

   ADC->ADCSOCCTL[2].bit.SHEN        = 1;/* Enable Sampler A                          */
   ADC->ADCSOCCTL[2].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[2].bit.CHSELP    = 4;/* Sampler A Positive = ADC0                */
   ADC->ADCSOCCTL[2].bit.CHSELN    = 0;/* Sampler A Negative = GND                 */
   ADC->ADCSOCCTL[2].bit.AVGCNT    = 2;/* Averaging 4 times (2^2)                  */
   ADC->ADCSOCCTL[2].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock        */
   ADC->ADCSOCCTL[2].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock     */
}
```

When configured as such, three conversions of ADC0 will be started in series on a PWM1SOCA event with the resulting values stored in the ADCRESULT[0] ~ ADCRESULT[2] registers.

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Example 12.3.3 Same trigger converts different channels (ADC0, ADC2, ADC8)

Example 12.3.3

```
void   ADC_Example12_3_3(void)
{
   ADC->ADCSOCCTL[0].bit.SHEN        = 1;/* Enable Sampler A                                */
   ADC->ADCSOCCTL[0].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[0].bit.CHSELP = 4;/* Sampler A Positive = ADC0                 */
   ADC->ADCSOCCTL[0].bit.CHSELN = 0;/* Sampler A Negative = GND                  */
   ADC->ADCSOCCTL[0].bit.AVGCNT = 2;/* Averaging 4 times (2^2)                   */
   ADC->ADCSOCCTL[0].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock          */
   ADC->ADCSOCCTL[0].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock        */

   ADC->ADCSOCCTL[1].bit.SHEN        = 1;/* Enable Sampler A                                */
   ADC->ADCSOCCTL[1].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[1].bit.CHSELP = 5;/* Sampler A Positive = ADC2                 */
   ADC->ADCSOCCTL[1].bit.CHSELN = 0;/* Sampler A Negative = GND                  */
   ADC->ADCSOCCTL[1].bit.AVGCNT = 2;/* Averaging 4 times (2^2)                   */
   ADC->ADCSOCCTL[1].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock          */
   ADC->ADCSOCCTL[1].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock        */

   ADC->ADCSOCCTL[2].bit.SHEN        = 1;/* Enable Sampler A                                */
   ADC->ADCSOCCTL[2].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[2].bit.CHSELP = 6;/* Sampler A Positive = ADC8                 */
   ADC->ADCSOCCTL[2].bit.CHSELN = 0;/* Sampler A Negative = GND                  */
   ADC->ADCSOCCTL[2].bit.AVGCNT = 2;/* Averaging 4 times (2^2)                   */
   ADC->ADCSOCCTL[2].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock          */
   ADC->ADCSOCCTL[2].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock        */
}
```

When configured this way, three conversions will be started in series on a PWM1SOCA event. The result of the conversion on channel ADC0 will show up in ADCRESULT0. The result of the conversion on channel ADC2 will show up in ADCRESULT[1]. The result of the conversion on channel ADC8 will show up in ADCRESULT[2]. The channel converted and the trigger has no bearing on where the result of the conversion shows up. The RESULT register is associated with the SOC.

If the application requires three different signals to be sampled from the same trigger, this can be done by simply changing the CHSELx field for SOC0-SOC2 while leaving the TRIGSEL field unchanged.

SPIN

12.3.1 Trigger operation

Each SOC can be configured to start on one of many input triggers. Multiple SOC's can be configured for the same channel if desired. Following is a list of the available input triggers:

- Software
- Timer 0/1/2 interrupts
- External SOC
- PWMxSOCA, PWMxSOCB and PWMxSOCC (x=0~7)

Table 12-1: Trigger source selection

TRIGSEL	Trigger Source
other	Invalid Selection
28	PWM7SOCC
27	PWM7SOCB
26	PWM7SOCA
25	PWM6SOCC
24	PWM6SOCB
23	PWM6SOCA
22	PWM5SOCC
21	PWM5SOCB
20	PWM5SOCA
19	PWM4SOCC
18	PWM4SOCB
17	PWM4SOCA
16	PWM3SOCC
15	PWM3SOCB
14	PWM3SOCA
13	PWM2SOCC
12	PWM2SOCB
11	PWM2SOCA
10	PWM1SOCC
9	PWM1SOCB
8	PWM1SOCA
7	PWM0SOCC
6	PWM0SOCB
5	PWM0SOCA
4	EXTSOC
3	Timer 2
2	Timer 1
1	Timer 0
0	Software

Table 12-1 lists the available trigger source. If TRIGSEL = 4, select the EXTSOC (External SOC event) as the SOC trigger source. Please refer to the ADCSOCCTL[x] register bit definitions for the configuration details

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of these triggers. Please see Table 12-38 and Table 12-39 for how to select GPIO pin as external SOC event source (ADCEXTSOCCTL).

12.3.2 ADC sampling mode and channel selection

The SHEN bit field controls ADC sampling mode. As Table 12-2 shown, when SHEN equals 0~3, all SOCs have the same control for the sequential sampling model. When SHEN equals 4~7, SOC0/SOC3/SOC6/SOC9/SOC12 have their dedicate control for the simultaneous sampling control.

Table 12-2: Sample mode description

ADCSOCCTL[x].SHEN[2:0] (x=0,3,6,9,12)	ADC Sampling Mode	ADCSOC[y]CTL.SHEN[1:0] (y=1,2,4,5,7,8,10,11,13,14,15)	ADC Sampling Mode
7	Sampler A, B, C Simultaneous	/	/
6	Sampler A and C Simultaneous	/	/
5	Sampler B and C Simultaneous	/	/
4	Sampler A and B Simultaneous	/	/
3	Sampler C Single	3	Sampler C Single
2	Sampler B Single	2	Sampler B Single
1	Sampler A Single	1	Sampler A Single
0	Disable	0	Disable

Although 3 sampler need 3 pair channel selection CHSELxP and CHSELxN (x=A,B,C), there are only one pair field CHSELP and CHSELN in each ADCSOCCTL[x] register. The sampler control bit-fields (SHEN) in ADCSOCCTL[x] register is to select which sampler should work and be converted. The CHSELP and CHSELN are associated with SHEN.

In sequential sampling mode, the SHEN control which sampler's channels are related to CHSELP and CHSELN. Please see Table 12-3 for details.

Table 12-3: ADCSOCCTL[x] channel selection for sequential sampler sampling

SHEN	CHSELAP	CHSELAN	CHSELBP	CHSELBN	CHSELCP	CHSELCN
3	Disable	Disable	Disable	Disable	CHSELP[2:0]	CHSELN[2:0]
2	Disable	Disable	CHSELP[2:0]	CHSELN[2:0]	Disable	Disable
1	CHSELP[2:0]	CHSELN[2:0]	Disable	Disable	Disable	Disable
0	Disable	Disable	Disable	Disable	Disable	Disable

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The detail channel selection for each sampler are showed in Table 12-4.

Table 12-4: ADC channel selection

Option	CHSELAP	CHSELAN	CHSELBP	CHSELBN	CHSELCP	CHSELCN
7	ADC14	ADC15	ADC16	ADC17	ADC18	ADC19
6	ADC8	ADC9	ADC10	ADC11	ADC12	ADC13
5	ADC2	ADC3	ADC4	ADC5	ADC6	ADC7
4	ADC0	ADC1	ADC0	ADC1	ADC0	ADC1
3	VDD33	VDD12	VBUF0	VBUF1	TSEN1	TSEN0
2	PGA3P	PGA3N	PGA4P	PGA4N	PGA5P	PGA5N
1	PGA0P	PGA0N	PGA1P	PGA1N	PGA2P	PGA2N
0	GND	GND	GND	GND	GND	GND

In simultaneous mode, the CHSELP and CHSELN control the channel related to SHEN and SOC. For example, we can use SOC0/SOC1/SOC2 to make 3 samplers simultaneous sampling according to the settings in Table 12-5. The channel selection for Sampler A is in ADCSOCCTL[0]. The channel selection for Sampler B is in ADCSOCCTL[1]. The channel selection for Sampler C is in ADCSOCCTL[2].

Table 12-5: Use SOC0/SOC1/SOC2 for 3 sampler simultaneous sampling

SHEN	CHSELAP	CHSELAN	CHSELBP	CHSELBN	CHSELCP	CHSELCN
7	ADCSOCCTL[0].CHSELP[2:0]	ADCSOCCTL[0].CHSELN[2:0]	ADCSOCCTL[1].CHSELP[2:0]	ADCSOCCTL[1].CHSELN[2:0]	ADCSOCCTL[2].CHSELP[2:0]	ADCSOCCTL[2].CHSELN[2:0]

And we can also use SOC4/SOC5 to make sampler B and sampler C simultaneous sampling according to the settings in Table 12-6. In this case, sampler A can't be used because simultaneous configuration is set in ADCSOCCTL[3]. The channel selection for Sampler B is in ADCSOCCTL[4]. The channel selection for Sampler C is in ADCSOCCTL[5].

Table 12-6: Use SOC4/SOC5 for 2 sampler simultaneous sampling

SHEN	CHSELAP	CHSELAN	CHSELBP	CHSELBN	CHSELCP	CHSELCN
6	Disable	Disable	ADCSOCCTL[4].CHSELP[2:0]	ADCSOCCTL[4].CHSELN[2:0]	ADCSOCCTL[5].CHSELP[2:0]	ADCSOCCTL[5].CHSELN[2:0]

For more detail description about simultaneous mode, please refer to Section 12.5.

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Example 12.3.4 ADC2, ADC4, ADC6 simultaneous sampling

It can be divided in to the followed lines:

Example 12.3.4

```
void   ADC_Example12_3_4(void)
{
   ADC->ADCSOCCTL[0].bit.SHEN        = 7;/* Enable Sampler A/B/C simultaneous      */
   ADC->ADCSOCCTL[0].bit.TRIGSEL = 8;/* Select PWM1SOCA as the trigger source   */
   ADC->ADCSOCCTL[0].bit.CHSELP = 5;/* Sampler A Positive = ADC2                  */
   ADC->ADCSOCCTL[0].bit.CHSELN = 0;/* Sampler A Negative = GND                    */
   ADC->ADCSOCCTL[0].bit.AVGCNT = 2;/* Averaging 4 times (2^2)                  */
   ADC->ADCSOCCTL[0].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock         */
   ADC->ADCSOCCTL[0].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock        */

   ADC->ADCSOCCTL[1].bit.SHEN        = 1;/* Will be ignore                        */
   ADC->ADCSOCCTL[1].bit.TRIGSEL = 8;/* Will be ignore    */
   ADC->ADCSOCCTL[1].bit.CHSELP = 5;/* Sampler B Positive = ADC4                  */
   ADC->ADCSOCCTL[1].bit.CHSELN = 0;/* Sampler B Negative = GND                    */
   ADC->ADCSOCCTL[1].bit.AVGCNT = 2;/* Will be ignore                        */
   ADC->ADCSOCCTL[1].bit.SAMPCNT = 3;/* Will be ignore        */
   ADC->ADCSOCCTL[1].bit.CONVCNT = 4;/* Will be ignore         */

   ADC->ADCSOCCTL[2].bit.SHEN        = 1;/* Will be ignore                        */
   ADC->ADCSOCCTL[2].bit.TRIGSEL = 8;/* Will be ignore    */
   ADC->ADCSOCCTL[2].bit.CHSELP = 5;/* Sampler C Positive = ADC6                  */
   ADC->ADCSOCCTL[2].bit.CHSELN = 0;/* Sampler C Negative = GND                    */
   ADC->ADCSOCCTL[2].bit.AVGCNT = 2;/* Will be ignore                        */
   ADC->ADCSOCCTL[2].bit.SAMPCNT = 3;/* Will be ignore         */
   ADC->ADCSOCCTL[2].bit.CONVCNT = 4;/* Will be ignore          */
}
```

Configure that SOC0 for 3 sampler simultaneous mode, so SOC0/SOC1/SOC2 channel control will be add to sampler A/B/C separately. The trigger source, averaging times, sampling count and conversion count will all use SOC0's configuration. Then the result will be saved to ADCRESULT[0]/[1]/[2], which are correspond to Sampler A/B/C.

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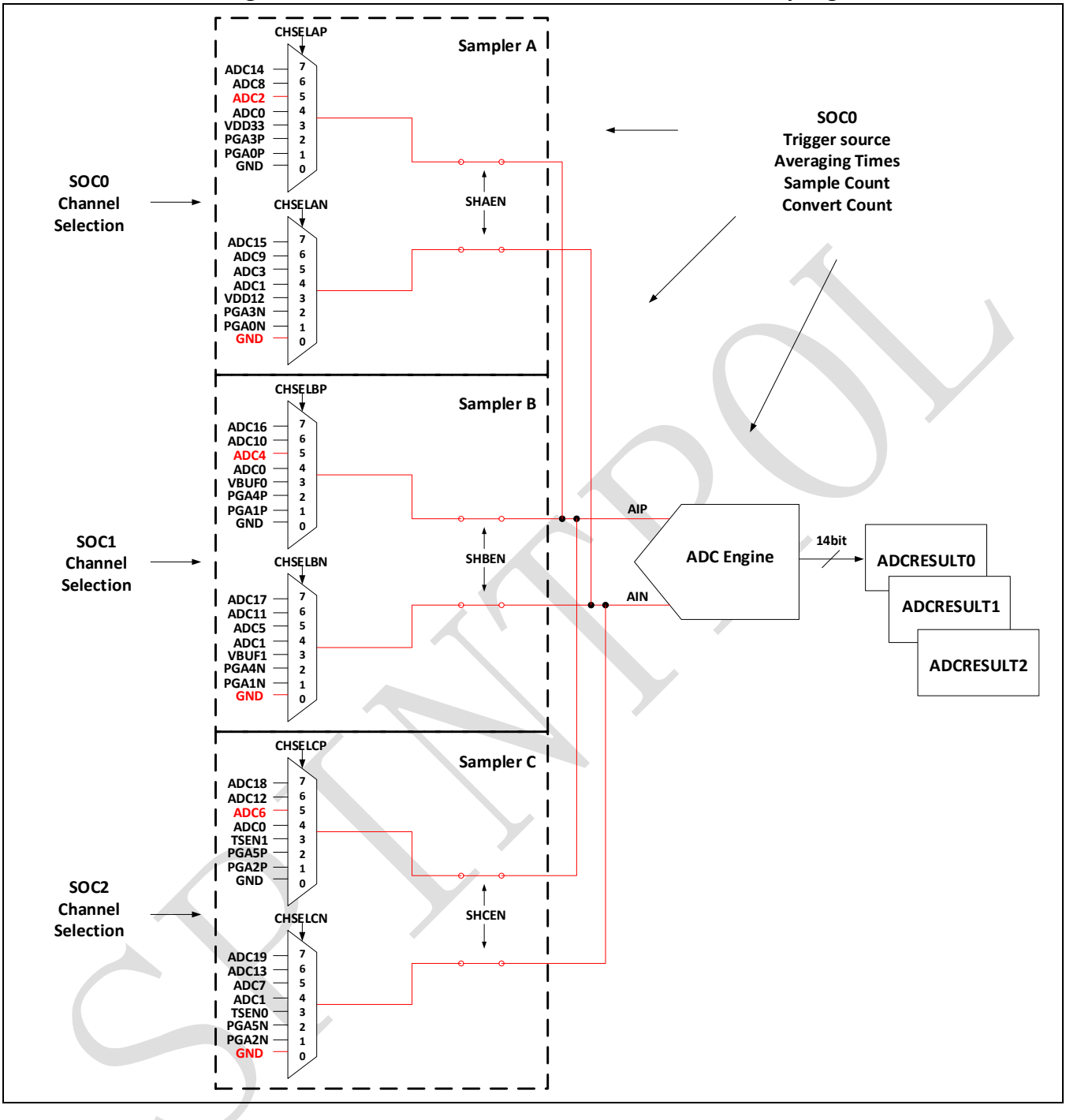
Figure 12-4: ADC2, ADC4 and ADC6 simultaneous sampling



12.3.3 Averaging control

Usually, there are some thermal noise source existing in sampling system such as input signal noise, KT/C noise, comparator noise, reference noise and power supply noise and so on. If use software to do post-averaging, it will make response time longer and waste CPU source. Use averaging control in SOC configuration, ADC can continuously sample many times and get an averaging result in hardware.

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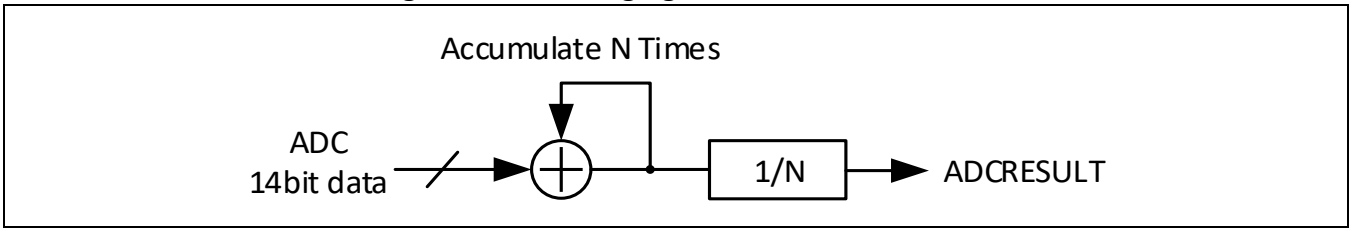
Figure 12-5: Averaging control for ADC result



Each SOC use the bit field AVGCNT in ADCSOCCTL[x] to set averaging times, which is a 3-bit field register.

Table 12-7: Averaging time selection

AVGCNT[2:0]	Averaging Times
7	128
6	64
5	32
4	16
3	8
2	4
1	2
0	1

12.3.4 ADC sample and convert window

External drivers vary in their ability to drive an analog signal quickly and effectively. Some circuits require longer times to properly transfer the charge into the sampling capacitor of an ADC. To address this, the ADC supports control over the sample window length for each individual SOC-configuration. Each ADCSOCCTL[x] register has an 8-bit field for SAMPCNT that determines the sampling time and a 7-bit field for CONVCNT that determines the conversion time.

$$Sample_Time = (\text{Sampcnt} + 1) \times \text{ADC_Clk_Cycle}$$
$$Conversion_Time = (\text{Convcnt} + 1) \times \text{ADC_Clk_Cycle}$$

The minimum conversion time is 140 ns. Spintrol suggests that sampling time should be at least as 125 ns. The total time to process analog signal is the sample time plus the conversion time. Examples of various sample window size are shown below in Table 12-8.

ADC clock cycle and CONVCNT setting must confirm this. For example, if ADC clock frequency is 32 MHz (clock cycle = 31.25ns), CONVCNT should be set above 4 to confirm conversion time over 140 ns.

Table 12-8: Sampling time with different SAMPCNT and CONVCNT (Example)

ADC Frequency	SAMPCNT	Sample Time(ns)	CONVCNT	Conversion Time(ns)	Total time to process analog signal(ns)	Sampling Rate
32 MHz	3	125	4	156.25	281.25	3.56MHz
32 MHz	27	875	4	156.25	1031.15	970kHz
40 MHz	4	125	5	150	275	3.64MHz
40 MHz	34	875	5	150	1025	976kHz
64 MHz	7	125	8	140.625	265.625	3.76MHz
64 MHz	55	875	8	140.625	1015.625	985kHz

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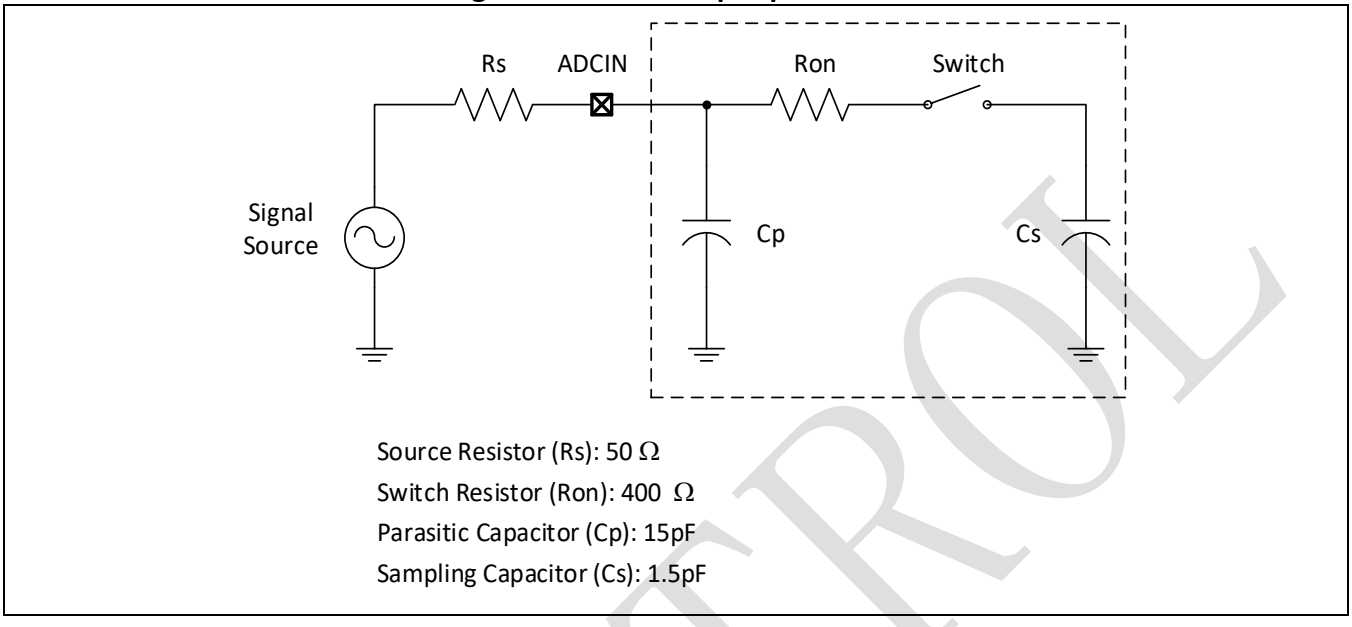
The minimum sampling time is decided by signal source impedance, parasitic resistor and parasitic capacitor in signal path. As shown in Figure 12-6, the ADCIN pins can be modeled as an RC circuit. A voltage swing from 0 to 3.3 V on ADCIN needs 70ns settling time for 12 bits precision.

Figure 12-6: ADCx input pin model



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12.4 ADC conversion priority

When multiple SOC flags are set at the same time, one of two forms of priority determines the order in which they are converted. The default priority method is round robin. In this scheme, no SOC has an inherent higher priority than another. Priority depends on the round robin pointer (RRPOINTER). The RRPOINTER reflected in the ADCSOCPRICTL register points to the last SOC converted. The highest priority SOC is given to the next value greater than the RRPOINTER value, wrapping around back to SOC0 after SOC15. At reset the value is 0. The RRPOINTER is reset by a device reset, when the ADCCTL0.RST bit is set, or when the ADCSOCPRICTL register is written.

An example of the round robin priority method is given in Figure 12-7.

Step1. After reset, SOC0 is highest priority SOC.

Step2. SOC7 receives trigger; SOC7 configured channel is converted immediately.

Step3. RRPOINTER changes to point to SOC7; SOC8 is now highest priority SOC. SOC2 & SOC12 triggers happen simultaneously; SOC12 is first on round robin wheel; SOC12 configured channel is converted while SOC2 stays pending.

Step4. RRPOINTER changes to point to SOC12; SOC2 configured channel is now converted.

Step5. RRPOINTER changes to point to SOC2; SOC3 is now highest priority SOC.

The PRIORITY field in the ADCSOCPRICTL register can be used to assign high priority, from a single SOC to all of the SOC's. When configured as high priority, an SOC will interrupt the round robin wheel after any current conversion completes and insert itself in as the next conversion. After its conversion completes, the round robin wheel will continue where it was interrupted. If two high priority SOC's are triggered at the same time, the SOC with the lower number will take precedence.

High priority mode is assigned first to SOC0, then in increasing numerical order. The value written in the PRIORITY field defines the first SOC that is not high priority. In other words, if a value of 4 is written into PRIORITY, then SOC0, SOC1, SOC2, and SOC3 are defined as high priority, with SOC0 the highest.

An example using high priority SOC's is given in Figure 12-8.

Example when PRIORITY = 4

Step1. After reset, SOC4 is 1st on round robin wheel; SOC7 receives trigger; SOC7 configured channel is converted immediately.

Step2. RRPOINTER changes to point to SOC7; SOC8 is now 1st on round robin wheel.

Step3. SOC2 & SOC12 triggers happen simultaneously; SOC2 interrupts round robin wheel and SOC2 configured channel is converted while SOC12 stays pending.

Step4. RRPOINTER stays pointing to 7; SOC12 configured channel is now converted.

Step5. RRPOINTER changes to point to SOC12; SOC13 is now 1st on round robin wheel.

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Figure 12-7: Round ring priority example

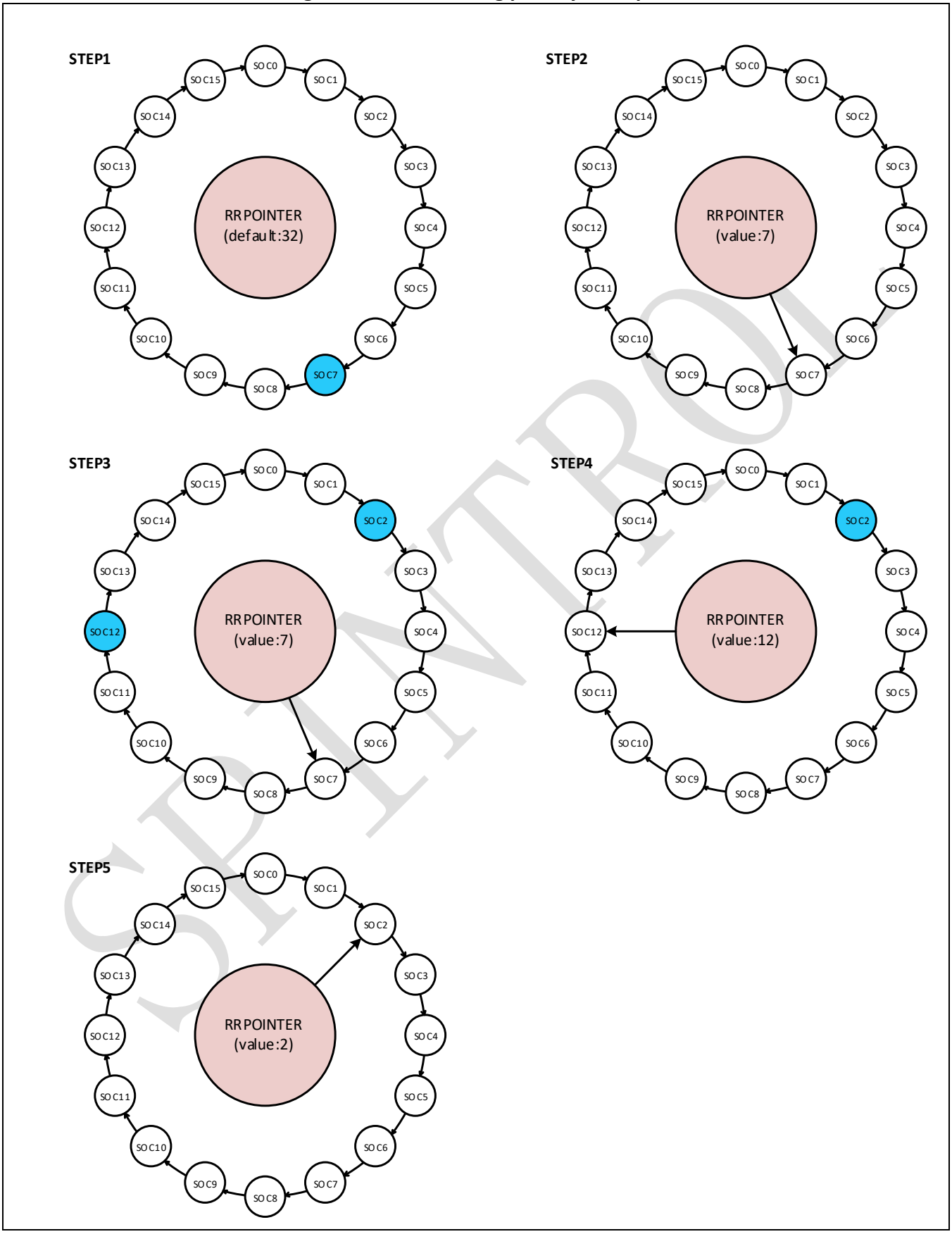

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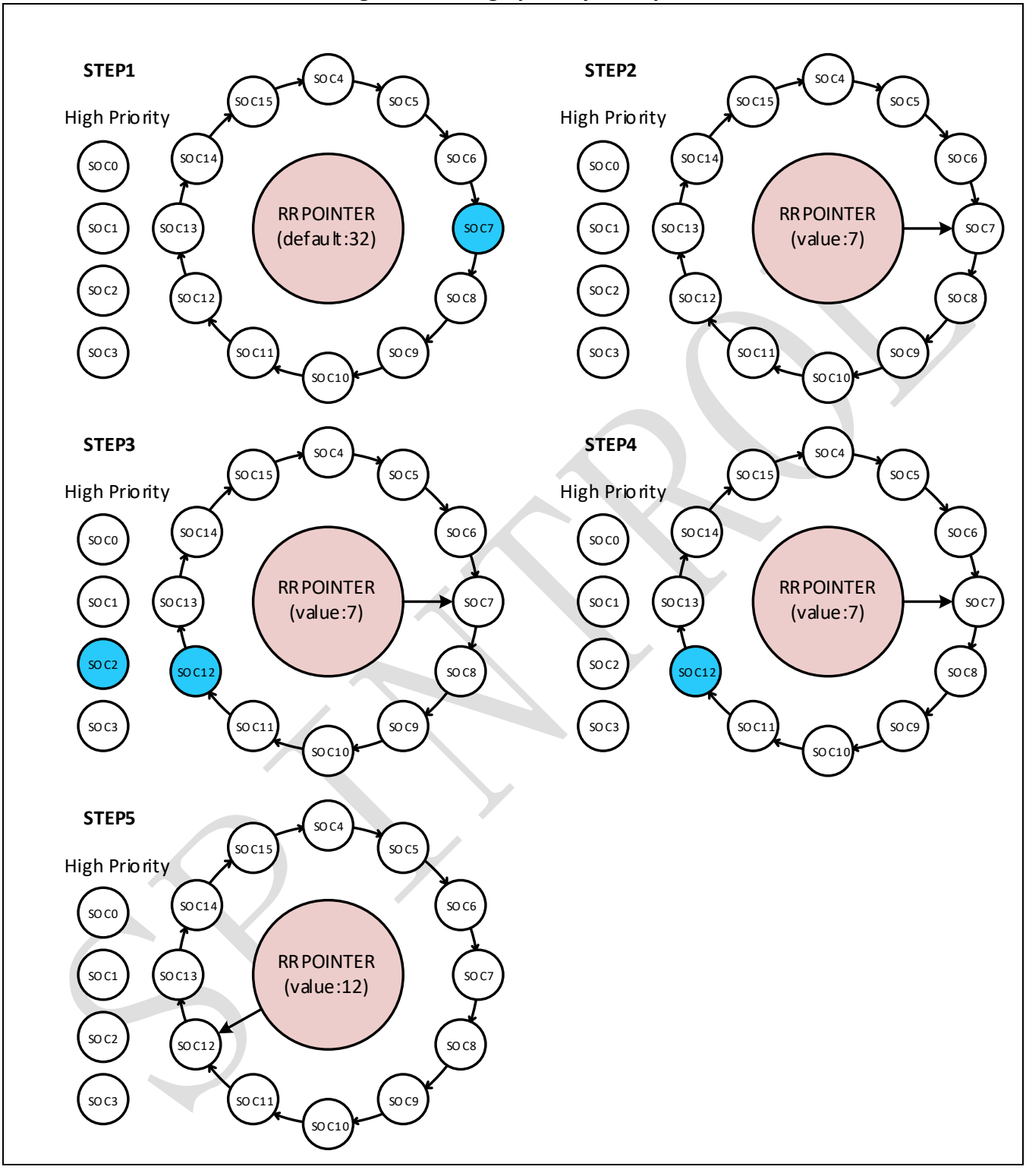
Figure 12-8: High priority example



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12.5 Simultaneous sampling mode

In some applications it is important to keep the delay minimal between the sampling of several signals. The ADC contains dual sample and hold circuits to allow two or three different channels to be sampled simultaneously. Simultaneous sampling mode is configured for SHEN with the ADCSOCCTL[x] register.

The behavior is as follows:

- The ADC system will combine SOC0~2, SOC3~SOC5, SCO6~SOC8, SOC9~SOC11, SOC12~SOC14 as 5 simultaneous sampling groups.
- For the simultaneous configuration like simultaneous mode, trigger source, averaging times, sampling count, conversion count will just can be set in SOC0, SOC3, SOC6, SOC9, SOC12.
- For the simultaneous channel selection, it is decided by simultaneous mode and SOC channel together.
- For different simultaneous mode, the channels selection of sampler A/B/C will be set in SOC[x], SOC[x+1], SOC[x+2]. (x=0, 3, 6, 9, 12)
- Sampler A channel will be always convert firstly. Then sampler B will be converted. At last, it's turn for sampler C conversion.
- The results of Sampler A/B/C conversion are placed in the ADCRESULT[x]/ ADCRESULT[x+1]/ ADCRESULT[x+2] register (x=0, 3, 6, 9, 12).
- When SHEN equals 4, Sampler A and B are simultaneous mode. The result will be saved to ADCRESULT[x]/ADCRESULT[x+1] register. Sampler C can be used separately, which can be configured by ADCSOCCTLx (x=0, 3, 6, 9, 12).
- When SHEN equals 5, Sampler B and C are simultaneous mode. Sampler A can't be used separately any more. The result will be saved to ADCRESULT[x+1]/ADCRESULT[x+2] register (x=0, 3, 6, 9, 12).
- When SHEN equal 6, Sampler A and C are simultaneous mode. The result will be saved to ADCRESULT[x]/ADCRESULT[x+2] register. Sampler B can be used separately, which can be configured by ADCSOCCTL[x+1] (x=0, 3, 6, 9, 12).

Table 12-9: Simultaneous sampling mode control

ADCSOCCTL[x].SHEN[2:0] (x=0,3,6,9,12)	SOCx	SOCx+1	SOCx+2	Sampling Mode Description
7	Sampler A	Sampler B	Sampler C	Sampler A, B, C Simultaneous
6	Sampler A	/	Sampler C	Sampler A and C Simultaneous
5	/	Sampler B	Sampler C	Sampler B and C Simultaneous
4	Sampler A	Sampler B	/	Sampler A and B Simultaneous

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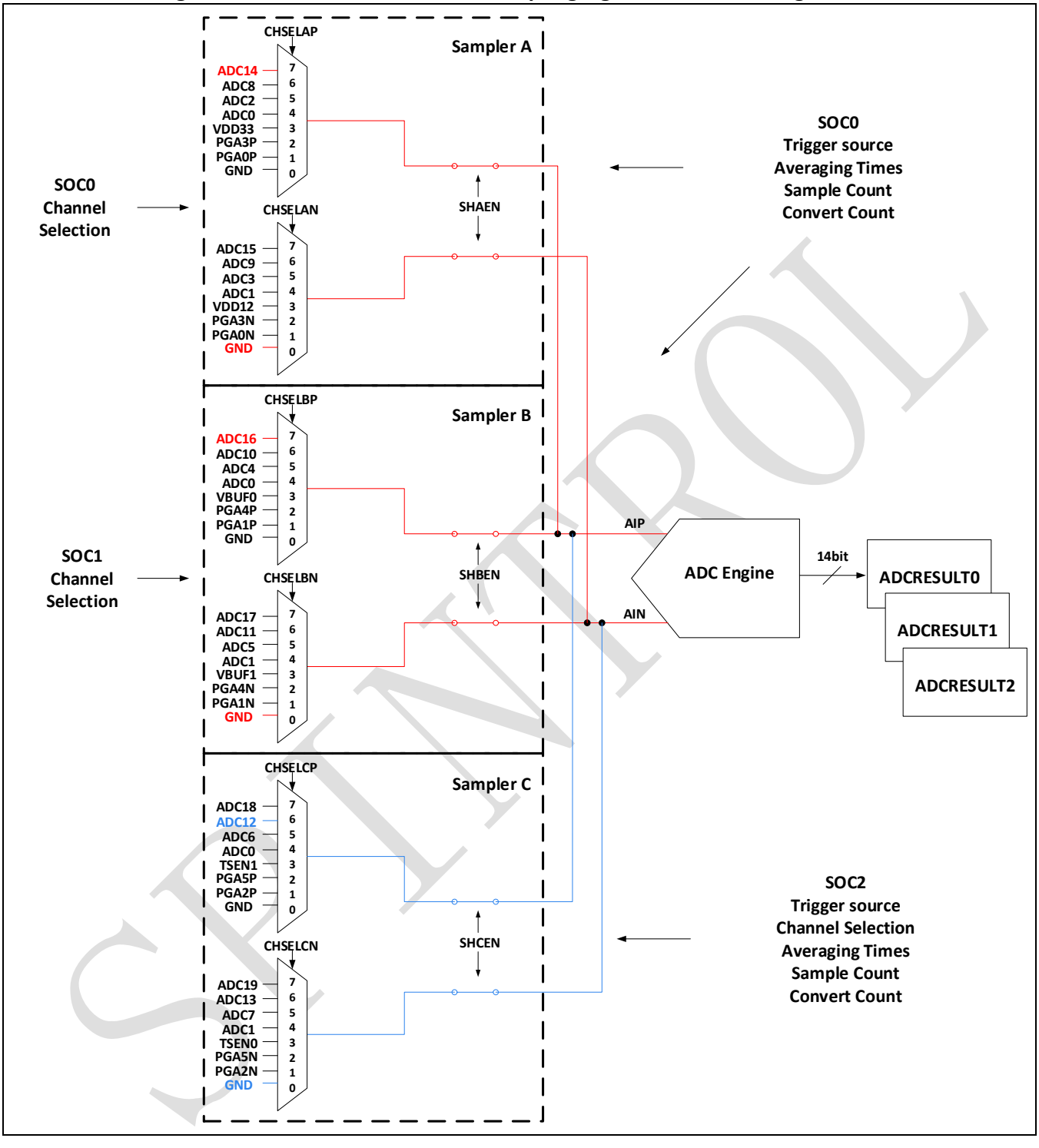
Figure 12-9: SOC0 simultaneous sampling signal flow and configuration



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Example 12.5.1 PWM0SOCA trigger SOC0 to convert ADC14, ADC16 simultaneously

Example 12.5.1

```
void   ADC_Example12_5_1(void)
{
   ADC->ADCSOCCTL[0].bit.SHEN        = 4;/* Enable Sampler A and B simultaneous       */
   ADC->ADCSOCCTL[0].bit.TRIGSEL = 5;/* Select PWM0SOCA as the trigger source   */
   ADC->ADCSOCCTL[0].bit.CHSELP = 7;/* Sampler A Positive = ADC14                  */
   ADC->ADCSOCCTL[0].bit.CHSELN = 0;/* Sampler A Negative = GND                    */
   ADC->ADCSOCCTL[0].bit.AVGCNT = 2;/* Averaging 4 times (2^2)                   */
   ADC->ADCSOCCTL[0].bit.SAMPCNT = 3;/* Sampling time = (3+1)*ADC_Clock          */
   ADC->ADCSOCCTL[0].bit.CONVCNT = 4;/* Conversion time = (4+1)*ADC_Clock          */

   ADC->ADCSOCCTL[1].bit.SHEN        = 1;/* Will be ignore                          */
   ADC->ADCSOCCTL[1].bit.TRIGSEL = 6;/* Will be ignore    */
   ADC->ADCSOCCTL[1].bit.CHSELP = 7;/* Sampler B Positive = ADC16                  */
   ADC->ADCSOCCTL[1].bit.CHSELN = 0;/* Sampler B Negative = GND                    */
   ADC->ADCSOCCTL[1].bit.AVGCNT = 2;/* Will be ignore                        */
   ADC->ADCSOCCTL[1].bit.SAMPCNT = 3;/* Will be ignore         */
   ADC->ADCSOCCTL[1].bit.CONVCNT = 4;/* Will be ignore          */

   ADC->ADCSOCCTL[2].bit.SHEN        = 3;/* Enable Sampler C single sampling          */
   ADC->ADCSOCCTL[2].bit.TRIGSEL = 9;/* Select PWM1SOCB as the trigger source   */
   ADC->ADCSOCCTL[2].bit.CHSELP = 6;/* Sampler C Positive = ADC12                  */
   ADC->ADCSOCCTL[2].bit.CHSELN = 0;/* Sampler C Negative = GND                    */
   ADC->ADCSOCCTL[2].bit.AVGCNT = 3;/* Averaging 8 times (2^3)                   */
   ADC->ADCSOCCTL[2].bit.SAMPCNT = 5;/* Sampling time = (5+1)*ADC_Clock          */
   ADC->ADCSOCCTL[2].bit.CONVCNT = 5;/* Conversion time = (5+1)*ADC_Clock          */
}
```

As Figure 12-9 shown, when the PWM0SOCA sends out a trigger, both ADC14 and ADC16 will be sampled simultaneously (assuming priority). Immediately after, the ADC14 channel will be converted and its value will be stored in the ADCRESULT[0] register. Then the ADC16 channel will be converted and its value will be stored in the ADCRESULT[1] register. The EOC0 pulse will either occur when the conversion of ADC16 completes. In addition to that, when PWM1SOCB sends out a trigger, ADC12 will be single sampled and its configuration comes from SOC2. Then its conversion result will be saved to ADCRESULT[2].

The rules of priority for the SOCx's remain the same as in sequential sampling mode.

Section 12.8 shows the timing of simultaneous sampling mode.

Note: In simultaneous mode, just channels in different samplers can be combined. For example, ADC2 can be simultaneously sampled with ADC4, but not ADC14. Because ADC2 and ADC14 are in the same sampler.

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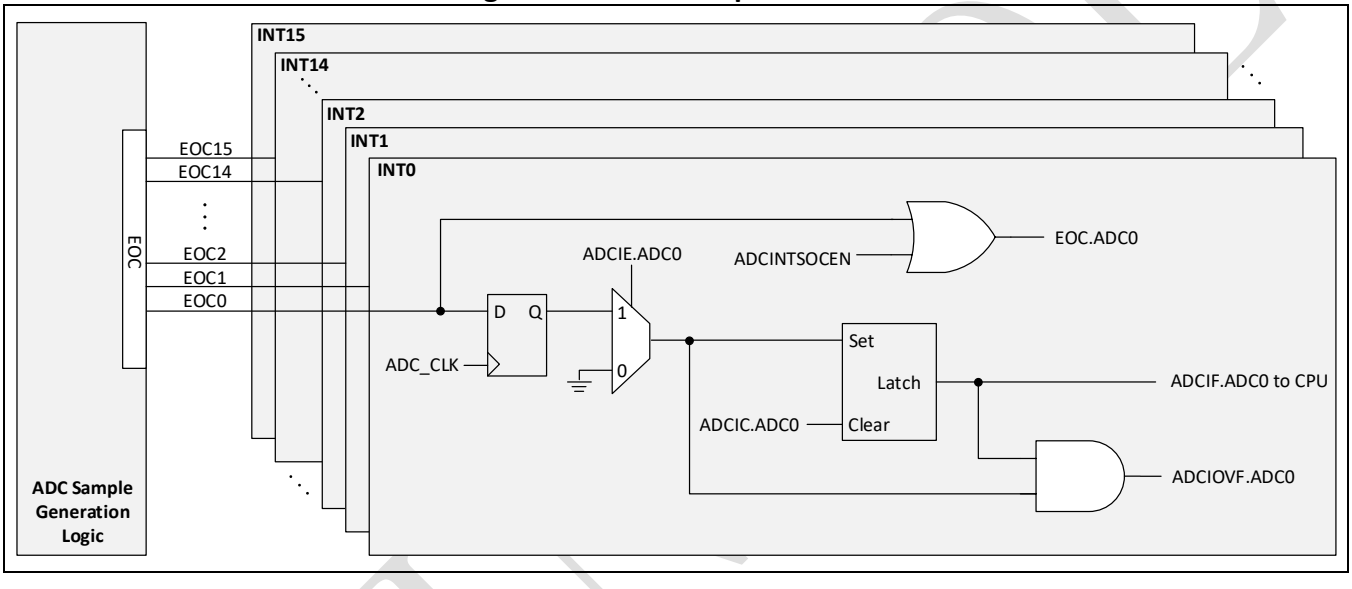
12.6 EOC and interrupt operation

Just as there are 16 independent SOC configuration sets, there are 16 EOCx pulses specifying corresponding end-of-conversion. In sequential sampling mode, the EOCx is associated directly with the SOCx. In simultaneous sampling mode, EOCx group are associated with SOCx group (x=0, 3, 6, 9, 12), as described in Section 12.5. The EOCx pulse will occur at the end of a conversion. See Figure 12-12 for exact timing sequence on the EOCx pulses. Each of EOCx signals can be configured as a trigger source to SOC. Also, this EOC signal can generate the ADC interrupts after 1 clock delay. There are 16 ADC interrupts from 16 EOC pulse. These interrupts can be passed on to the CPU.

Figure 12-10 shows the block diagram of the ADC interrupt structure.

Figure 12-10: Interrupt structure



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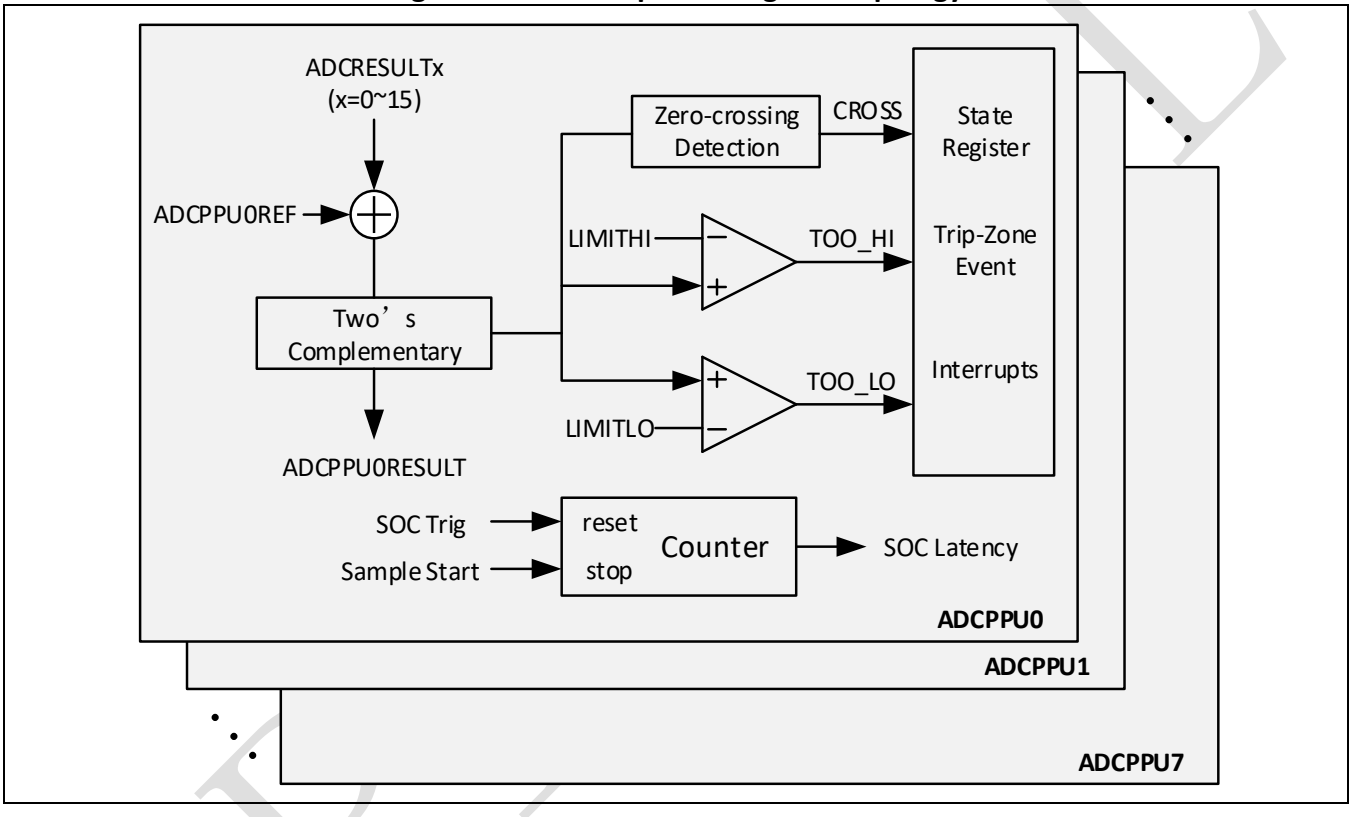
12.7 ADC post-processing units

There are 8 post-processing units (PPU) in ADC digital circuits. These blocks can be associated with any of the 16 RESULT registers using the ADCPPUCTLx.DATASEL bit field. Each PPU can simultaneously remove subtract out a reference value, flag a zero-crossing point, and flag a high or low compare limit. Furthermore, the zero-crossing can generate a trip-zone event to PWM and/or generate an interrupt.

A PPU is also capable of recording the delay between when the SOC associated with the PPU is triggered and when it actually begins to be sampled. Figure 12-11 presents the structure of each PPU. Subsequent sections explain the use of each sub-module.

Figure 12-11: Post-processing unit topology



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12.7.1 PPU reference error calculation

In many applications, ADC conversion result need to be subtracted from a reference value. The PPU can perform these function automatically, reducing the sample to output latency and software overhead.

First, configure the register ADCPPUCTLx.DATASEL pointing to the desired SOC result. That means PPU will operation after this SOC result come out. Then, writing a value to the ADCPPUREFx register as the reference value. The post-processing block will automatically subtract the value from the desired SOC result and store it in the ADCPPURESULTx register. This subtraction will produce a sign-extended 32-bit result. It is also possible to selectively invert the calculated value before storing in the ADCPPURESULTx register by setting the ADCPPUCTLx.POL field.

Example 12.7.1 Use PPU0 subtract a reference value from SOC0 result

It can be divided in to the followed lines:

Example 12.7.1

```
void   ADC_Example12_7_1(void)
{
   ADC->ADCPPUCTL[0].bit.EN        = 1;/* Enable ADC PPU0        */
   ADC->ADCPPUCTL[0].bit.DATASEL = 0;/*Select SOC0 result as post-processing data */
   ADC->ADCPPUREF[0].all = 100;/* Set the reference value of PPU0 is 100    */

   ADC->ADCIC.bit.INT0 = 1;/* Clear SOC0 interrupt flag */
   ADC->ADCSOCFRC.bit.SOC0 = 1;/*Trig SOC0 to convert and PPU0 to post-processing */
   while(ADC->ADCIF.bit.INT0 != 1){}; /* wait for SOC0 result ready*/
}
```

Configure that SOC0's result will subtract a reference value in PPU0, so PPU0 should enable firstly. Then select SOC0 conversion result for PPU to post-process. Set the fixed-point in PPU0. At last trig SOC0, PPU will post-process the result for SOC0 after conversion.

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12.7.2 PPU zero-crossing and threshold detection

Many applications perform a threshold detection against the ADC conversion results. The PPU can automatically perform a check against whenever ADCPPURESULTx changes sign or a high and low limit. Based on these comparisons, PPU can generate a trip to the PWM and/or an interrupt automatically, lowering the sample to PWM latency and reducing software overhead. This functionality also enables safety conscious applications to trip the PWM based on an out-of-range ADC conversion without any CPU intervention.

To enable this functionality, configure the register ADCPPUCTLx.DATASEL pointing to the desired SOC result. That means PPU will operation once the SOC is triggered. Then write a value to one or both of the registers ADCPPUTHHx and ADCPPUTHLx (Zero-crossing detection does not require further configuration).

Whenever the ADCPPURESULTx changes signs, the XZRO bit in the ADCPPUTZEx register will be only set when the corresponding EOC signal occurs. Whenever the threshold limits are exceeded, the TZHI and TZLO will be set when the corresponding EOC signal occurs.

These event can also generate the corresponding interrupt flag in the ADCPPUIFx register. The ADCPPUIEx register can enable this function. The corresponding bit in ADCPPUICx register can clear the related interrupt flag.

Example 12.7.2 Use PPU0 detect zero-crossing and high/low limit from SOC0 result

It can be divided in to the followed lines:

Example 12.7.2

```
void ADC_Example12_7_2(void)
{
   ADC->ADCPPUCTL[0].bit.EN          = 1;/* Enable ADC PPU0         */
   ADC->ADCPPUIE[0].bit.XZRO       = 1;/* Enable zero-crossing interrupt of ADC PPU0 */
   ADC->ADCPPUIE[0].bit.TZHI         = 1;/* Enable too high interrupt of ADC PPU0 */
   ADC->ADCPPUIE[0].bit.TZLO         = 1;/* Enable too low interrupt of ADC PPU0 */

   ADC->ADCPPUCTL[0].bit.DATASEL = 0;/*Select SOC0 result as post-processing data */
   ADC->ADCPPUTHH[0].all = 3000;/* Set PPU0 high threshold is 3000    */
   ADC->ADCPPUTHL[0].all = 1000;/* Set PPU0 low threshold is 1000    */

   ADC->ADCIC.bit.INT0 = 1;/* Clear SOC0 interrupt flag */
   ADC->ADCSOCFRC.bit.SOC0 = 1;/*Trig SOC0 to convert and PPU0 to post-processing */
   while(ADC->ADCIF.bit.INT0 != 1){}; /* wait for SOC0 result ready*/
}
```

Configure that SOC0's result will be detected by PPU0. So enable PPU0 and related interrupt. Set high and low limit threshold for PPU0 detection. At last, trig SOC0. Then PPU0 will make a detection after SOC0 conversion done.

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12.7.3 Sample delay capture

When multiple control loops are running asynchronously on the same ADC, there is a chance that an ADC request from two or more loops will collide, causing one of the samples to be delayed. This shows up as a measurement error in the system. By knowing when this delay occurs and the amount of delay that has occurred, software can employ extrapolation techniques to reduce the error.

To this effect, each PPU has the field SOCSEL in the ADCPPUCTLx register. This field contains the number of ADC clock cycles between the moment the associate SOC was triggered and that it began converting. This is achieved by having a global 32-bit free running counter based on ADC clock, which is in the ADCPPUSOCDLYx register. When the trigger for the associated SOC arrives, this counter value will reset and start to count. When the actual sample window for that SOC begins, the counter will stop and the current counter value will store in the ADCPPUSOCDLYx register.

Example 12.7.3 Use PPU0 to counter the sampling delay for SOC0

It can be divided in to the followed lines:

Example 12.7.3

```
void   ADC_Example12_7_3(void)
{
   ADC->ADCPPUCTL[0].bit.EN          = 1;/* Enable ADC PPU0        */
   ADC->ADCPPUCTL[0].bit.SOCSEL = 0;/* Select SOC0 to count sample delay */

   ADC->ADCIC.bit.INT0 = 1;        /* Clear SOC0 interrupt flag */
   ADC->ADCSOCFRC.bit.SOC0 = 1; /* Trig SOC0 and reset PPU0 delay capture counter */
   while(ADC->ADCIF.bit.INT0 != 1){}; /* wait for SOC0 result ready*/
}
```

Enable PPU0 for delay capture and configure SOC0 as tracking target. Then, trig SOC0. Then PPU0 will counter the delay from trigger time to SOC0 real sampling.

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12.8 ADC timing

Figure 12-12: Timing example for sequential mode interrupt

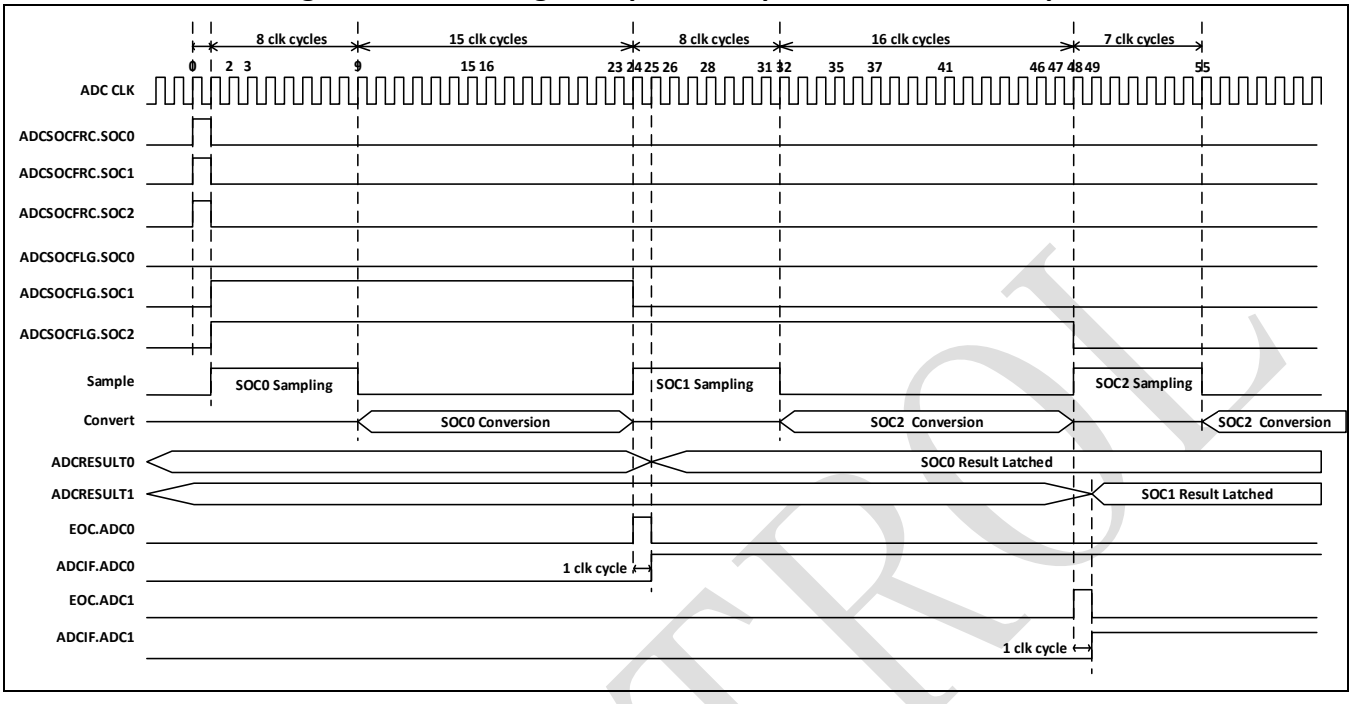
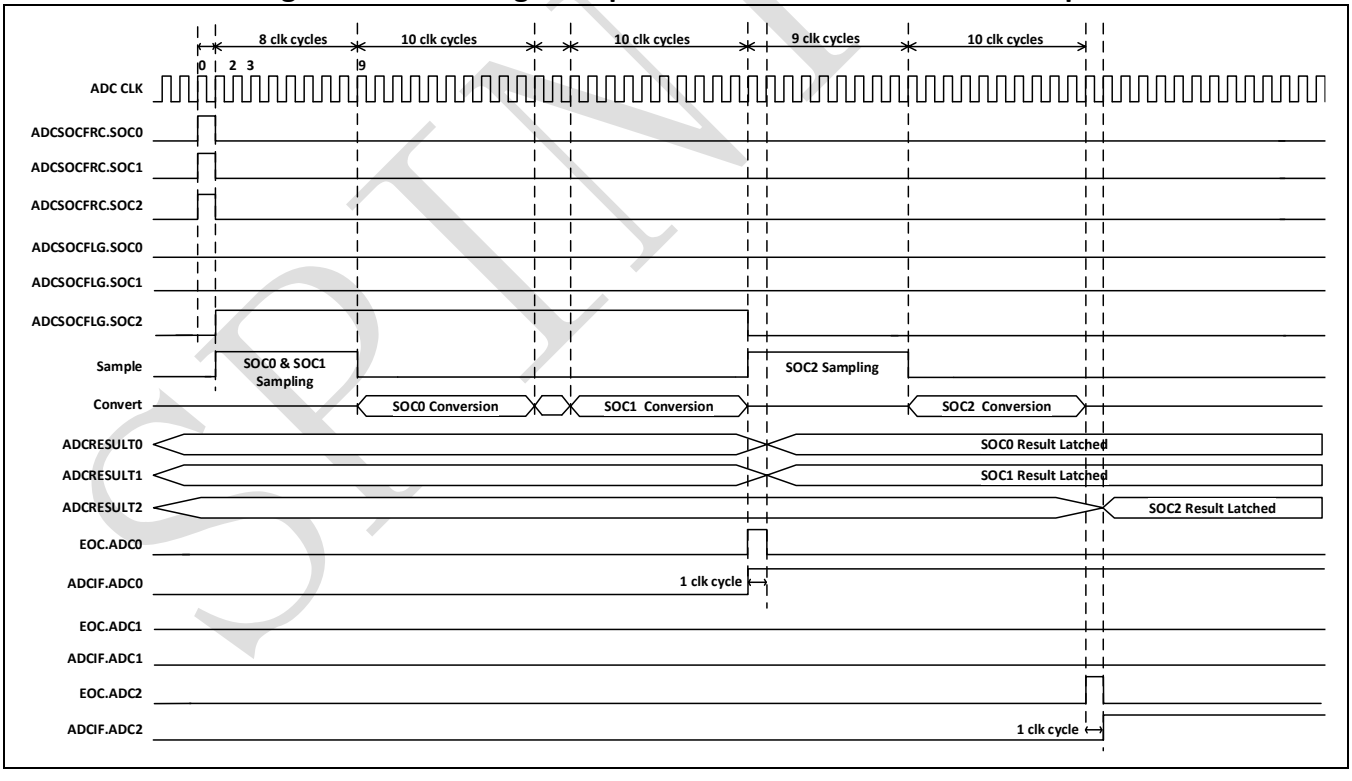


Figure 12-13: Timing example for simultaneous mode interrupt



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12.9 Power-up sequence

When powering up the ADC, the following sequence must be used:
Step 1: Power up ADC bandgap
Step 2: After 200us power up ADC reference buffer
Step 3: After 200us, power up the analog circuits of ADC

Example 12.9.1 Power up sequence

It can be divided in to the followed lines:

Example 12.9.1

```
void   ADC_Example12_9_1(void)
{
   ADC->ADCBGCTL.bit.EN = 1;    /* Enable on Bandgap                */
   Delay_ms(1);
   ADC->ADCREFCTL.bit.EN = 1; /* Enable Reference Buffer           */
   Delay_ms(1);
   ADC->ADCCTL.bit.EN = 1; /* Enable ADC                 */
   ADC->ADCCTL.bit.RST = 1; /* ADC logic state-machine reset, will be self-clear */
}
```

When powering down the ADC, all three bits in step 1~3 can be cleared simultaneously. The ADC power levels must be controlled via software and they are independent of the state of the device power modes.

When power-up, all ADC registers will be reset. After that, all ADC registers can be reset also when ADCCTL.RST is enabled. This reset will be self-clear.

12.10 ADC calibration

Inherent in any converter is an offset error and a full scale gain error. The ADC is factory calibrated at 25-degrees Celsius to correct both of these while allowing the user to modify the offset and gain correction register for any application environmental effects, such as the ambient temperature. Except under certain emulation conditions, or unless a modification from the factory settings is desired, the user is not required to perform any specific action. The ADC will be properly calibrated in every conversion, which is completed by hardware.

12.10.1 Factory settings and hardware calibration

During the fabrication and test process Spintrol calibrates several ADC settings which are stored in Flash memory. During the SPC2168 startup, boot code will write the factory settings into their respective active registers. When ADC in normal operation, the active registers will be used for hardware calibration.

12.10.2 Channel calibration

As Figure 12-1 shown, the respective active registers are OFFSET0~15 and GAIN0~15. They are correspond to SOC0~15. That allowed customer to modify the offset and gain parameter for special channel.

The channel calibration formula is:

$$ADC_RESULT[i] = (\mathrm{ADC_RAW_CODE[i]} - \mathrm{OFFSET[i]}) \times \mathrm{GAIN[i]}$$

In this formula, the parameter I is related to SOC and its range is from 0 to 15. This calibration function will be done in hardware automatically.

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12.11 ADC result

12.11.1 Quantization range

The quantization range of ADC is from -FS to +FS. (FS: full scale)

$$FS = 3.657\text{V}$$

However, for each channel, its voltage can't be over AVDD. If AVDD is 3.3V, that means the input voltage of each channel can't be over 3.3V.

12.11.2 ADC result calculation formula

As Figure 12-14 showed, ADC input is differential. Each end input range is 0~3.657V. As Figure 12-15 showed, its quantization range is -3.657V to 3.657V; digital code range is -8192~8191.

For differential mode,

$$ADC_RESULT = \frac{(AIP - AIN)}{3.657} \times 8192$$

All fractional values are truncated.

Figure 12-14: ADC core description

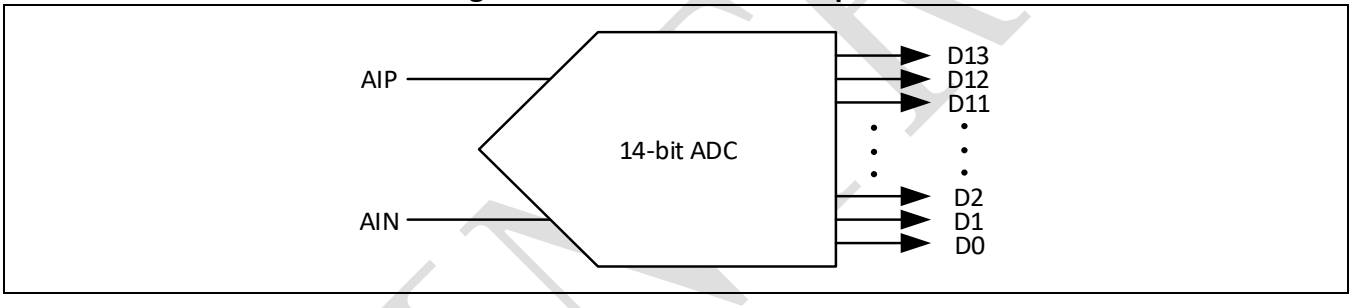
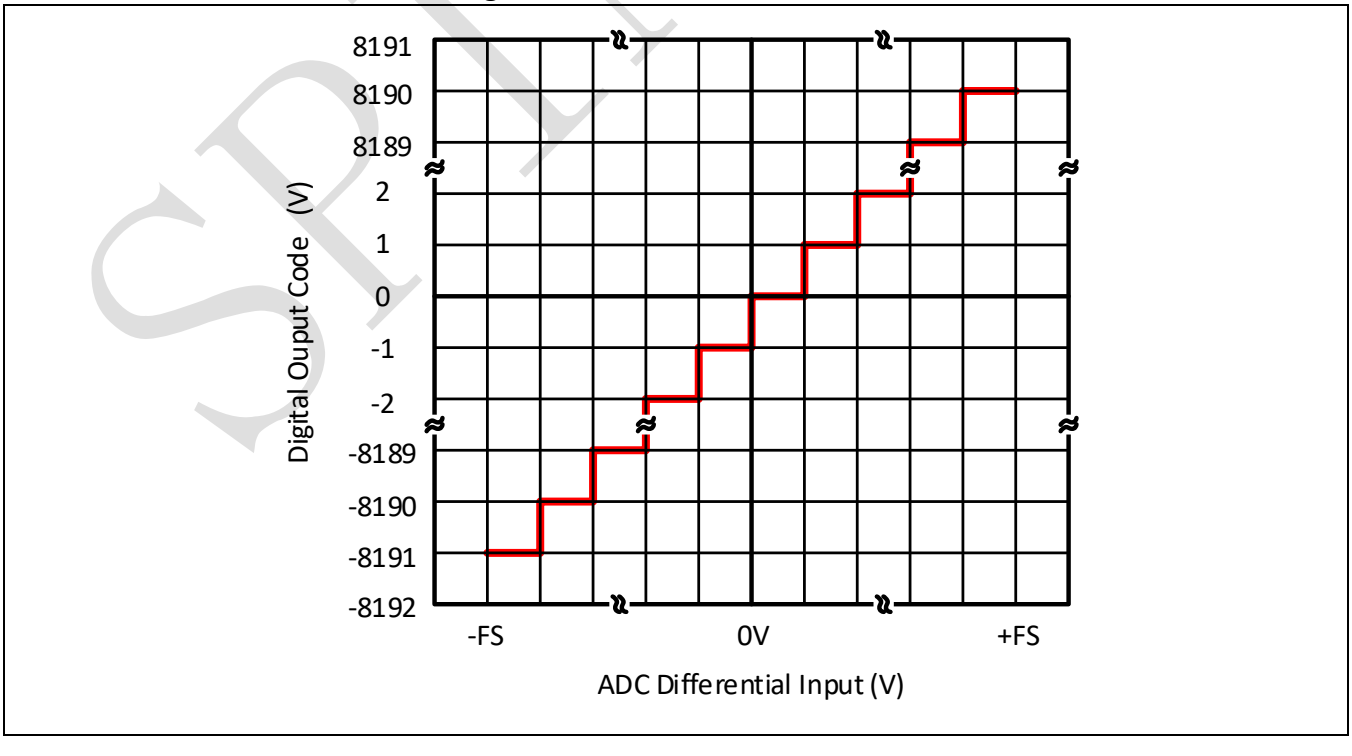


Figure 12-15: ADC transfer curve



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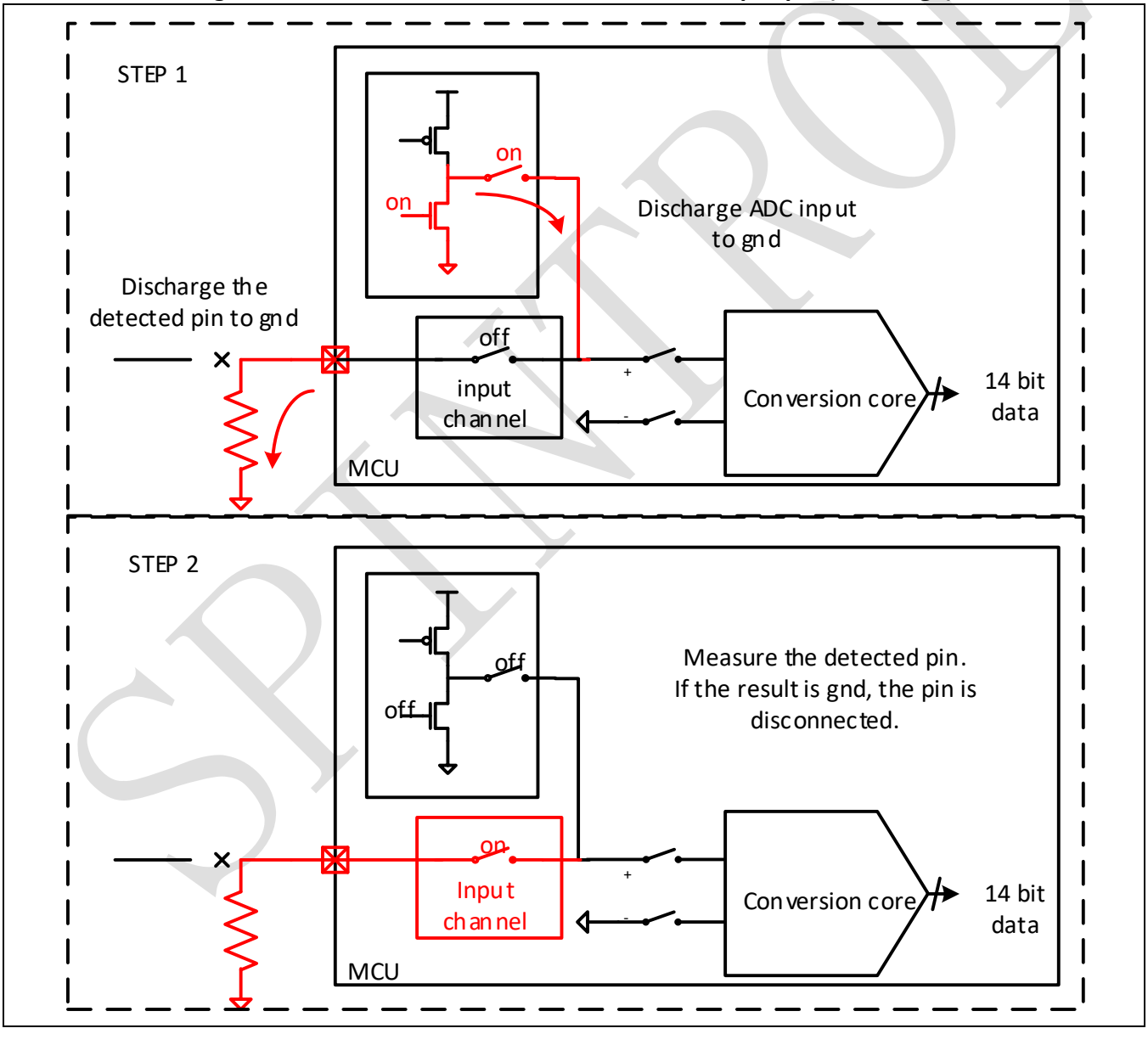
12.12 ADC safety feature

12.12.1 Analog disconnection detection

When the analog input from a sensor to the MCU is disconnected, the position of rotation, temperature and so on cannot be sensed correctly and depending on the application could cause serious damage. The ADC Input disconnection circuit detects an error under such circumstances which provides opportunity to activate fail-safe procedures.

The disconnection detection function can be enabled by configuring the ADCCTL register. In this ADC IP, it supports two optional scenarios to detect the disconnection. They are discharge and precharge cases.

Figure 12-16: Detect the disconnection of ADC input pin (Discharge)



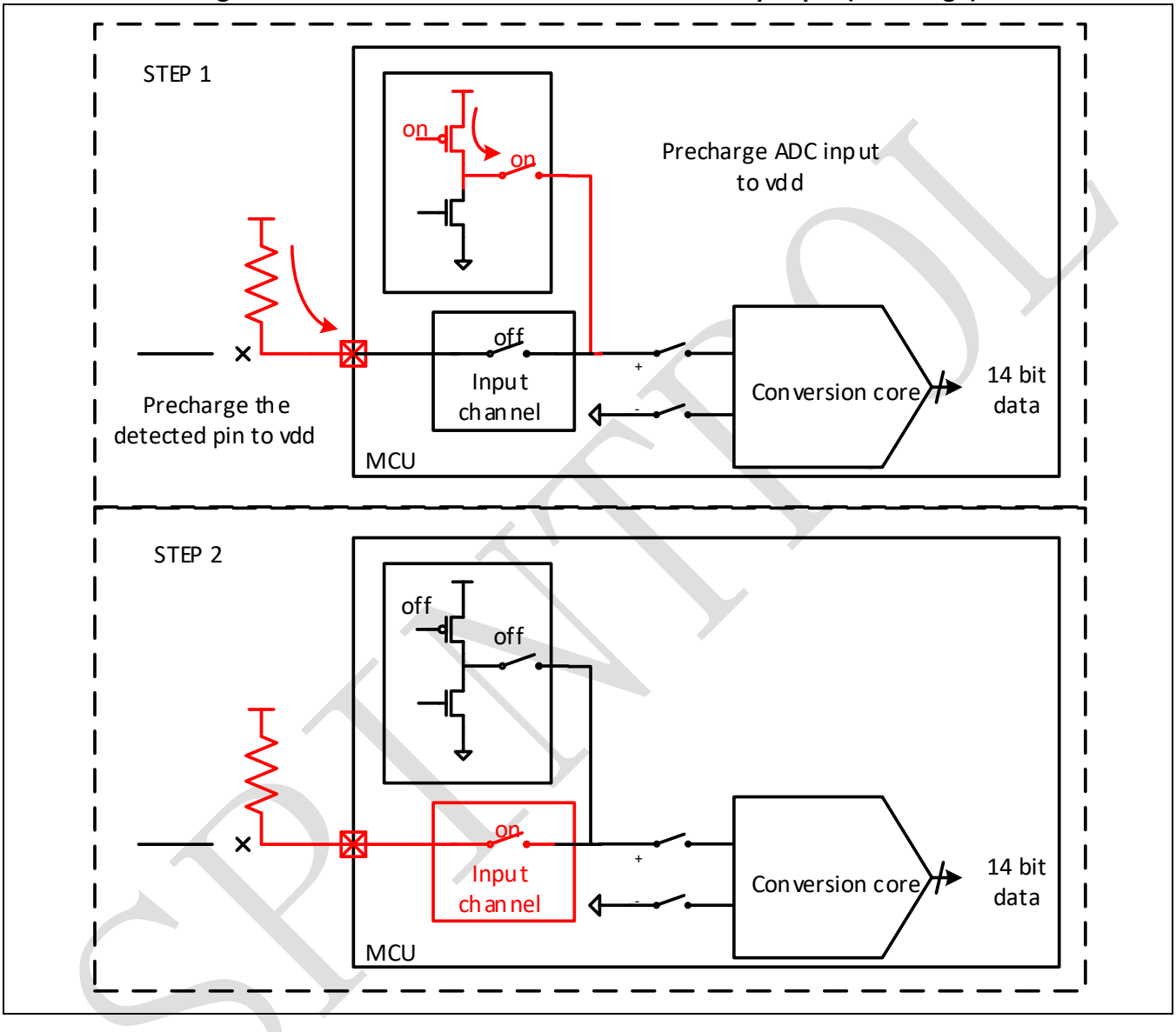
As Figure 12-16 shown the discharge case as below, two procedures are carried on the detection.

- Step1. Keep the input channel mux switch is disable. In the same time, discharge the input pin to gnd, and discharge internal ADC sampling node to gnd separately.

- Step2. Enable input channel mux switch. Use ADC to measure the input of pin. If the data show around 0x0000h, that means the input pin always keep around ground without external driven source.

In this case, we think the pin is disconnected.

Figure 12-17: Detect the disconnection of ADC input pin (Precharge)



As Figure 12-17 shown the precharge case as below, two procedures are carried on the detection.

- Step1. Keep the input channel mux switch is disable. In the same time, precharge the input pin to vdd, and precharge internal ADC sampling node to vdd separately.
- Step2. Enable input channel mux switch. Use ADC to measure the input of pin. If the data show around 0x1CE0h (VDD=3.3V), that means the input pin always keep around vdd without external driven source.

In this case, we think the pin is disconnected.

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12.12.2 Input short detection

When the analog input from a sensor to the MCU is anomalously shorted, the ADC Input disconnection circuit can detect a short, which provides opportunity to activate fail-safe procedures.

The input-short detection function can be enabled by configuring the ADCCTL register. The procedures of the detection are shown below:

Step1. ADC measures the input of pin. Save the result as DATA1.

Step2. Force this input pin to GND. ADC measures the input of pin. Save the result as DATA2.

Step3. Force this input pin to AVDD. ADC measures the input of pin. Save the result as DATA3.

Step4. If DATA1= DATA2=DATA3, the pin is shorted.

Note:	The short can only be determined if the driving impedance strength is high enough. Assume ADC resolves about 1mV voltage, and given pull-up and pull-down current of 8uA, maximum source impedance can be calculated as: Rsource,max = 1mV/8uA = 125Ω. If the ADC is driven by the source whose impedance is larger than this value, input short cannot be detected.

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12.13 Registers

12.13.1 ADC register map

Table 12-10: ADC Module Base Address

Peripheral Module	Base Address
ADC	0x4000 8C00

Table 12-11: ADC Register Map

Register	Offset	Description	Reset Value
ADCIF	0x00	ADC Interrupt Flag Register	0x00000000
ADCIC	0x04	ADC Interrupt Flag Clear Register	0x00000000
ADCIOVF	0x08	ADC Interrupt Overflow Flag Register	0x00000000
ADCIOVFC	0x0C	ADC Interrupt Overflow Flag Clear Register	0x00000000
ADCIE*	0x10	ADC Interrupt Enable Register	0x00000000
ADCSOCPRICTL*	0x14	ADC Start of Conversion Priority Control Register	0x00000000
ADCSOCFLG	0x18	ADC SOC Flag Register	0x00000000
ADCSOCFRC	0x1C	ADC SOC Force Register	0x00000000
ADCSOCOVF	0x20	ADC SOC Overflow Register	0x00000000
ADCSOCOVFC	0x24	ADC SOC Overflow Clear Register	0x00000000
ADCINTSOCEN*	0x28	ADC Interrupt Trigger SOC Enable Register	0x00000000
ADCINTSOCSEL0*	0x2C	ADC Interrupt Trigger SOC Select Register 0	0x00000000
ADCINTSOCSEL1*	0x30	ADC Interrupt Trigger SOC Select Register 1	0x00000000
ADCEXTSOCCTL*	0x34	ADC External SOC Input Control Register	0x0000007F
ADCSOCCTL0*	0x38	ADC SOC0 Control Register	0x00000000
ADCSOCCTL1*	0x3C	ADC SOC1 Control Register	0x00000000
ADCSOCCTL2*	0x40	ADC SOC2 Control Register	0x00000000
ADCSOCCTL3*	0x44	ADC SOC3 Control Register	0x00000000
ADCSOCCTL4*	0x48	ADC SOC4 Control Register	0x00000000
ADCSOCCTL5*	0x4C	ADC SOC5 Control Register	0x00000000
ADCSOCCTL6*	0x50	ADC SOC6 Control Register	0x00000000
ADCSOCCTL7*	0x54	ADC SOC7 Control Register	0x00000000
ADCSOCCTL8*	0x58	ADC SOC8 Control Register	0x00000000
ADCSOCCTL9*	0x5C	ADC SOC9 Control Register	0x00000000
ADCSOCCTL10*	0x60	ADC SOC10 Control Register	0x00000000
ADCSOCCTL11*	0x64	ADC SOC11 Control Register	0x00000000
ADCSOCCTL12*	0x68	ADC SOC12 Control Register	0x00000000
ADCSOCCTL13*	0x6C	ADC SOC13 Control Register	0x00000000
ADCSOCCTL14*	0x70	ADC SOC14 Control Register	0x00000000
ADCSOCCTL15*	0x74	ADC SOC15 Control Register	0x00000000
ADCOFFSET0*	0x78	ADC Offset Trim Register 0	0x00000000
ADCOFFSET1*	0x7C	ADC Offset Trim Register 1	0x00000000
ADCOFFSET2*	0x80	ADC Offset Trim Register 2	0x00000000
ADCOFFSET3*	0x84	ADC Offset Trim Register 3	0x00000000
ADCOFFSET4*	0x88	ADC Offset Trim Register 4	0x00000000
ADCOFFSET5*	0x8C	ADC Offset Trim Register 5	0x00000000

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Register	Offset	Description	Reset Value
ADCOFFSET6*	0x90	ADC Offset Trim Register 6	0x00000000
ADCOFFSET7*	0x94	ADC Offset Trim Register 7	0x00000000
ADCOFFSET8*	0x98	ADC Offset Trim Register 8	0x00000000
ADCOFFSET9*	0x9C	ADC Offset Trim Register 9	0x00000000
ADCOFFSET10*	0xA0	ADC Offset Trim Register 10	0x00000000
ADCOFFSET11*	0xA4	ADC Offset Trim Register 11	0x00000000
ADCOFFSET12*	0xA8	ADC Offset Trim Register 12	0x00000000
ADCOFFSET13*	0xAC	ADC Offset Trim Register 13	0x00000000
ADCOFFSET14*	0xB0	ADC Offset Trim Register 14	0x00000000
ADCOFFSET15*	0xB4	ADC Offset Trim Register 15	0x00000000
ADCGAIN0*	0xB8	ADC Gain Trim Register 0	0x00008000
ADCGAIN1*	0xBC	ADC Gain Trim Register 1	0x00008000
ADCGAIN2*	0xC0	ADC Gain Trim Register 2	0x00008000
ADCGAIN3*	0xC4	ADC Gain Trim Register 3	0x00008000
ADCGAIN4*	0xC8	ADC Gain Trim Register 4	0x00008000
ADCGAIN5*	0xCC	ADC Gain Trim Register 5	0x00008000
ADCGAIN6*	0xD0	ADC Gain Trim Register 6	0x00008000
ADCGAIN7*	0xD4	ADC Gain Trim Register 7	0x00008000
ADCGAIN8*	0xD8	ADC Gain Trim Register 8	0x00008000
ADCGAIN9*	0xDC	ADC Gain Trim Register 9	0x00008000
ADCGAIN10*	0xE0	ADC Gain Trim Register 10	0x00008000
ADCGAIN11*	0xE4	ADC Gain Trim Register 11	0x00008000
ADCGAIN12*	0xE8	ADC Gain Trim Register 12	0x00008000
ADCGAIN13*	0xEC	ADC Gain Trim Register 13	0x00008000
ADCGAIN14*	0xF0	ADC Gain Trim Register 14	0x00008000
ADCGAIN15*	0xF4	ADC Gain Trim Register 15	0x00008000
ADCOFFSETA*	0xF8	ADC SHA Offset Trim Register	0x00000000
ADCOFFSETB*	0xFC	ADC SHB Offset Trim Register	0x00000000
ADCOFFSETC*	0x100	ADC SHC Offset Trim Register	0x00000000
ADCGAINA*	0x104	ADC SHA Gain Trim Register	0x00008000
ADCGAINB*	0x108	ADC SHB Gain Trim Register	0x00008000
ADCGAINC*	0x10C	ADC SHC Gain Trim Register	0x00008000
ADCSTS	0x110	ADC Status Register	0x00000000
ADCSTSCLR	0x114	ADC Status Clear Register	0x00000000
ADCCTL*	0x118	ADC Control Register	0x00000008
ADCBGCTL*	0x11C	ADC Bandgap Control Register	0x00000000
ADCREFCTL*	0x120	ADC Reference Control Register	0x00003D3C
ADCRAWCODEA	0x124	ADC SHA Raw Code Register	0x00000000
ADCRAWCODEB	0x128	ADC SHB Raw Code Register	0x00000000
ADCRAWCODEC	0x12C	ADC SHC Raw Code Register	0x00000000
ADCRESULT0	0x130	ADC Result Register 0	0x00000000
ADCRESULT1	0x134	ADC Result Register 1	0x00000000
ADCRESULT2	0x138	ADC Result Register 2	0x00000000
ADCRESULT3	0x13C	ADC Result Register 3	0x00000000

SPINTROL

Register	Offset	Description	Reset Value
ADCRESULT4	0x140	ADC Result Register 4	0x00000000
ADCRESULT5	0x144	ADC Result Register 5	0x00000000
ADCRESULT6	0x148	ADC Result Register 6	0x00000000
ADCRESULT7	0x14C	ADC Result Register 7	0x00000000
ADCRESULT8	0x150	ADC Result Register 8	0x00000000
ADCRESULT9	0x154	ADC Result Register 9	0x00000000
ADCRESULT10	0x158	ADC Result Register 10	0x00000000
ADCRESULT11	0x15C	ADC Result Register 11	0x00000000
ADCRESULT12	0x160	ADC Result Register 12	0x00000000
ADCRESULT13	0x164	ADC Result Register 13	0x00000000
ADCRESULT14	0x168	ADC Result Register 14	0x00000000
ADCRESULT15	0x16C	ADC Result Register 15	0x00000000
ADCPPURESULT0	0x170	ADCPPU0 Comparison Result Register	0x00000000
ADCPPURESULT1	0x174	ADCPPU1 Comparison Result Register	0x00000000
ADCPPURESULT2	0x178	ADCPPU2 Comparison Result Register	0x00000000
ADCPPURESULT3	0x17C	ADCPPU3 Comparison Result Register	0x00000000
ADCPPURESULT4	0x180	ADCPPU4 Comparison Result Register	0x00000000
ADCPPURESULT5	0x184	ADCPPU5 Comparison Result Register	0x00000000
ADCPPURESULT6	0x188	ADCPPU6 Comparison Result Register	0x00000000
ADCPPURESULT7	0x18C	ADCPPU7 Comparison Result Register	0x00000000
ADCPPUSOCDLY0	0x190	ADCPPU0 SOC Delay Register	0x00000000
ADCPPUSOCDLY1	0x194	ADCPPU1 SOC Delay Register	0x00000000
ADCPPUSOCDLY2	0x198	ADCPPU2 SOC Delay Register	0x00000000
ADCPPUSOCDLY3	0x19C	ADCPPU3 SOC Delay Register	0x00000000
ADCPPUSOCDLY4	0x1A0	ADCPPU4 SOC Delay Register	0x00000000
ADCPPUSOCDLY5	0x1A4	ADCPPU5 SOC Delay Register	0x00000000
ADCPPUSOCDLY6	0x1A8	ADCPPU6 SOC Delay Register	0x00000000
ADCPPUSOCDLY7	0x1AC	ADCPPU7 SOC Delay Register	0x00000000
ADCPPUIF0	0x1B0	ADCPPU0 Interrupt Flag Register	0x00000000
ADCPPUIF1	0x1B4	ADCPPU1 Interrupt Flag Register	0x00000000
ADCPPUIF2	0x1B8	ADCPPU2 Interrupt Flag Register	0x00000000
ADCPPUIF3	0x1BC	ADCPPU3 Interrupt Flag Register	0x00000000
ADCPPUIF4	0x1C0	ADCPPU4 Interrupt Flag Register	0x00000000
ADCPPUIF5	0x1C4	ADCPPU5 Interrupt Flag Register	0x00000000
ADCPPUIF6	0x1C8	ADCPPU6 Interrupt Flag Register	0x00000000
ADCPPUIF7	0x1CC	ADCPPU7 Interrupt Flag Register	0x00000000
ADCPPUIC0	0x1D0	ADCPPU0 Interrupt Clear Register	0x00000000
ADCPPUIC1	0x1D4	ADCPPU1 Interrupt Clear Register	0x00000000
ADCPPUIC2	0x1D8	ADCPPU2 Interrupt Clear Register	0x00000000
ADCPPUIC3	0x1DC	ADCPPU3 Interrupt Clear Register	0x00000000
ADCPPUIC4	0x1E0	ADCPPU4 Interrupt Clear Register	0x00000000
ADCPPUIC5	0x1E4	ADCPPU5 Interrupt Clear Register	0x00000000
ADCPPUIC6	0x1E8	ADCPPU6 Interrupt Clear Register	0x00000000
ADCPPUIC7	0x1EC	ADCPPU7 Interrupt Clear Register	0x00000000

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Register	Offset	Description	Reset Value
ADCPPUIE0*	0x1F0	ADCPPU0 Interrupt Enable Register	0x00000000
ADCPPUIE1*	0x1F4	ADCPPU1 Interrupt Enable Register	0x00000000
ADCPPUIE2*	0x1F8	ADCPPU2 Interrupt Enable Register	0x00000000
ADCPPUIE3*	0x1FC	ADCPPU3 Interrupt Enable Register	0x00000000
ADCPPUIE4*	0x200	ADCPPU4 Interrupt Enable Register	0x00000000
ADCPPUIE5*	0x204	ADCPPU5 Interrupt Enable Register	0x00000000
ADCPPUIE6*	0x208	ADCPPU6 Interrupt Enable Register	0x00000000
ADCPPUIE7*	0x20C	ADCPPU7 Interrupt Enable Register	0x00000000
ADCPPUTZE0*	0x210	ADCPPU0 Trip-Zone Event Enable Register	0x00000000
ADCPPUTZE1*	0x214	ADCPPU1 Trip-Zone Event Enable Register	0x00000000
ADCPPUTZE2*	0x218	ADCPPU2 Trip-Zone Event Enable Register	0x00000000
ADCPPUTZE3*	0x21C	ADCPPU3 Trip-Zone Event Enable Register	0x00000000
ADCPPUTZE4*	0x220	ADCPPU4 Trip-Zone Event Enable Register	0x00000000
ADCPPUTZE5*	0x224	ADCPPU5 Trip-Zone Event Enable Register	0x00000000
ADCPPUTZE6*	0x228	ADCPPU6 Trip-Zone Event Enable Register	0x00000000
ADCPPUTZE7*	0x22C	ADCPPU7 Trip-Zone Event Enable Register	0x00000000
ADCPPUCTL0*	0x230	ADCPPU0 Control Register	0x00000400
ADCPPUCTL1*	0x234	ADCPPU1 Control Register	0x00000400
ADCPPUCTL2*	0x238	ADCPPU2 Control Register	0x00000400
ADCPPUCTL3*	0x23C	ADCPPU3 Control Register	0x00000400
ADCPPUCTL4*	0x240	ADCPPU4 Control Register	0x00000400
ADCPPUCTL5*	0x244	ADCPPU5 Control Register	0x00000400
ADCPPUCTL6*	0x248	ADCPPU6 Control Register	0x00000400
ADCPPUCTL7*	0x24C	ADCPPU7 Control Register	0x00000400
ADCPPUREF0*	0x250	ADCPPU0 Reference Register	0x00000000
ADCPPUREF1*	0x254	ADCPPU1 Reference Register	0x00000000
ADCPPUREF2*	0x258	ADCPPU2 Reference Register	0x00000000
ADCPPUREF3*	0x25C	ADCPPU3 Reference Register	0x00000000
ADCPPUREF4*	0x260	ADCPPU4 Reference Register	0x00000000
ADCPPUREF5*	0x264	ADCPPU5 Reference Register	0x00000000
ADCPPUREF6*	0x268	ADCPPU6 Reference Register	0x00000000
ADCPPUREF7*	0x26C	ADCPPU7 Reference Register	0x00000000
ADCPPUTHH0*	0x270	ADCPPU0 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHH1*	0x274	ADCPPU1 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHH2*	0x278	ADCPPU2 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHH3*	0x27C	ADCPPU3 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHH4*	0x280	ADCPPU4 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHH5*	0x284	ADCPPU5 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHH6*	0x288	ADCPPU6 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHH7*	0x28C	ADCPPU7 Trip-Zone High-Side Threshold Register	0x00000000
ADCPPUTHL0*	0x290	ADCPPU0 Trip-Zone Low-Side Threshold Register	0x00000000
ADCPPUTHL1*	0x294	ADCPPU1 Trip-Zone Low-Side Threshold Register	0x00000000
ADCPPUTHL2*	0x298	ADCPPU2 Trip-Zone Low-Side Threshold Register	0x00000000
ADCPPUTHL3*	0x29C	ADCPPU3 Trip-Zone Low-Side Threshold Register	0x00000000

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Register	Offset	Description	Reset Value
ADCPPUTHL4*	0x2A0	ADCPPU4 Trip-Zone Low-Side Threshold Register	0x00000000
ADCPPUTHL5*	0x2A4	ADCPPU5 Trip-Zone Low-Side Threshold Register	0x00000000
ADCPPUTHL6*	0x2A8	ADCPPU6 Trip-Zone Low-Side Threshold Register	0x00000000
ADCPPUTHL7*	0x2AC	ADCPPU7 Trip-Zone Low-Side Threshold Register	0x00000000
TSENSCTL*	0x2B0	Temperature Sensor Control Register	0x00000000
ADCREGKEY	0x2B4	ADC Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the ADCREGKEY=0x1ACCE551.

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12.13.2 ADC registers

12.13.2.1 ADC Interrupt Flag Register (ADCIF)

Table 12-12: ADC Interrupt Flag Register (ADCIF) Layout

ADCIF (ADC Interrupt Flag Register) Offset: 0x0 Default: 0x00000000 Access: ADC -> ADCIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 INT15	14 INT14	13 INT13	12 INT12	11 INT11	10 INT10	9 INT9	8 INT8
7 INT7	6 INT6	5 INT5	4 INT4	3 INT3	2 INT2	1 INT1	0 INT0

Table 12-13: ADC Interrupt Flag Register (ADCIF) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	INT15	RO	0x0	ADC interrupt 15 flag 0: ADC interrupt 15 does not happen 1: ADC interrupt 15 happened
14	INT14	RO	0x0	ADC interrupt 14 flag 0: ADC interrupt 14 does not happen 1: ADC interrupt 14 happened
13	INT13	RO	0x0	ADC interrupt 13 flag 0: ADC interrupt 13 does not happen 1: ADC interrupt 13 happened
12	INT12	RO	0x0	ADC interrupt 12 flag 0: ADC interrupt 12 does not happen 1: ADC interrupt 12 happened
11	INT11	RO	0x0	ADC interrupt 11 flag 0: ADC interrupt 11 does not happen 1: ADC interrupt 11 happened
10	INT10	RO	0x0	ADC interrupt 10 flag 0: ADC interrupt 10 does not happen 1: ADC interrupt 10 happened
9	INT9	RO	0x0	ADC interrupt 9 flag 0: ADC interrupt 9 does not happen 1: ADC interrupt 9 happened
8	INT8	RO	0x0	ADC interrupt 8 flag

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: ADC interrupt 8 does not happen 1: ADC interrupt 8 happened
7	INT7	RO	0x0	ADC interrupt 7 flag 0: ADC interrupt 7 does not happen 1: ADC interrupt 7 happened
6	INT6	RO	0x0	ADC interrupt 6 flag 0: ADC interrupt 6 does not happen 1: ADC interrupt 6 happened
5	INT5	RO	0x0	ADC interrupt 5 flag 0: ADC interrupt 5 does not happen 1: ADC interrupt 5 happened
4	INT4	RO	0x0	ADC interrupt 4 flag 0: ADC interrupt 4 does not happen 1: ADC interrupt 4 happened
3	INT3	RO	0x0	ADC interrupt 3 flag 0: ADC interrupt 3 does not happen 1: ADC interrupt 3 happened
2	INT2	RO	0x0	ADC interrupt 2 flag 0: ADC interrupt 2 does not happen 1: ADC interrupt 2 happened
1	INT1	RO	0x0	ADC interrupt 1 flag 0: ADC interrupt 1 does not happen 1: ADC interrupt 1 happened
0	INT0	RO	0x0	ADC interrupt 0 flag 0: ADC interrupt 0 does not happen 1: ADC interrupt 0 happened

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12.13.2.2 ADC Interrupt Flag Clear Register (ADCIC)

Table 12-14: ADC Interrupt Flag Clear Register (ADCIC) Layout

ADCIC (ADC Interrupt Flag Clear Register) Offset: 0x4 Default: 0x00000000 Access: ADC -> ADCIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 INT15	14 INT14	13 INT13	12 INT12	11 INT11	10 INT10	9 INT9	8 INT8
7 INT7	6 INT6	5 INT5	4 INT4	3 INT3	2 INT2	1 INT1	0 INT0

Table 12-15: ADC Interrupt Flag Clear Register (ADCIC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	INT15	W1C	0x0	ADC Interrupt 15 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT15. This bit is self-cleared.
14	INT14	W1C	0x0	ADC Interrupt 14 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT14. This bit is self-cleared.
13	INT13	W1C	0x0	ADC Interrupt 13 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT13. This bit is self-cleared.
12	INT12	W1C	0x0	ADC Interrupt 12 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT12. This bit is self-cleared.
11	INT11	W1C	0x0	ADC Interrupt 11 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT11. This bit is self-cleared.
10	INT10	W1C	0x0	ADC Interrupt 10 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT10. This bit is self-cleared.
9	INT9	W1C	0x0	ADC Interrupt 9 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT9. This bit is self-cleared.
8	INT8	W1C	0x0	ADC Interrupt 8 flag clear 0: Write a 0 has no effect and always reads back 0.

SPINTROL

Bits	Field Name	Type	Reset	Description
				1: Write a 1 clears ADCIF.INT8. This bit is self-cleared.
7	INT7	W1C	0x0	ADC Interrupt 7 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT7. This bit is self-cleared.
6	INT6	W1C	0x0	ADC Interrupt 6 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT6. This bit is self-cleared.
5	INT5	W1C	0x0	ADC Interrupt 5 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT5. This bit is self-cleared.
4	INT4	W1C	0x0	ADC Interrupt 4 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT4. This bit is self-cleared.
3	INT3	W1C	0x0	ADC Interrupt 3 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT3. This bit is self-cleared.
2	INT2	W1C	0x0	ADC Interrupt 2 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT2. This bit is self-cleared.
1	INT1	W1C	0x0	ADC Interrupt 1 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT1. This bit is self-cleared.
0	INT0	W1C	0x0	ADC Interrupt 0 flag clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears ADCIF.INT0. This bit is self-cleared.

SPINTROL

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12.13.2.3 ADC Interrupt Overflow Flag Register (ADCIOVF)

Table 12-16: ADC Interrupt Overflow Flag Register (ADCIOVF) Layout

ADCIOVF (ADC Interrupt Overflow Flag Register) Offset: 0x8 Default: 0x00000000 Access: ADC -> ADCIOVF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 INT15	14 INT14	13 INT13	12 INT12	11 INT11	10 INT10	9 INT9	8 INT8
7 INT7	6 INT6	5 INT5	4 INT4	3 INT3	2 INT2	1 INT1	0 INT0

Table 12-17: ADC Interrupt Overflow Flag Register (ADCIOVF) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	INT15	RO	0x0	ADC interrupt 15 overflow flag 0: No overflow 1: ADC interrupt 15 overflow
14	INT14	RO	0x0	ADC interrupt 14 overflow flag 0: No overflow 1: ADC interrupt 14 overflow
13	INT13	RO	0x0	ADC interrupt 13 overflow flag 0: No overflow 1: ADC interrupt 13 overflow
12	INT12	RO	0x0	ADC interrupt 12 overflow flag 0: No overflow 1: ADC interrupt 12 overflow
11	INT11	RO	0x0	ADC interrupt 11 overflow flag 0: No overflow 1: ADC interrupt 11 overflow
10	INT10	RO	0x0	ADC interrupt 10 overflow flag 0: No overflow 1: ADC interrupt 10 overflow
9	INT9	RO	0x0	ADC interrupt 9 overflow flag 0: No overflow 1: ADC interrupt 9 overflow
8	INT8	RO	0x0	ADC interrupt 8 overflow flag 0: No overflow 1: ADC interrupt 8 overflow

SPINTROL

Bits	Field Name	Type	Reset	Description
7	INT7	RO	0x0	ADC interrupt 7 overflow flag 0: No overflow 1: ADC interrupt 7 overflow
6	INT6	RO	0x0	ADC interrupt 6 overflow flag 0: No overflow 1: ADC interrupt 6 overflow
5	INT5	RO	0x0	ADC interrupt 5 overflow flag 0: No overflow 1: ADC interrupt 5 overflow
4	INT4	RO	0x0	ADC interrupt 4 overflow flag 0: No overflow 1: ADC interrupt 4 overflow
3	INT3	RO	0x0	ADC interrupt 3 overflow flag 0: No overflow 1: ADC interrupt 3 overflow
2	INT2	RO	0x0	ADC interrupt 2 overflow flag 0: No overflow 1: ADC interrupt 2 overflow
1	INT1	RO	0x0	ADC interrupt 1 overflow flag 0: No overflow 1: ADC interrupt 1 overflow
0	INT0	RO	0x0	ADC interrupt 0 overflow flag 0: No overflow 1: ADC interrupt 0 overflow

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12.13.2.4 ADC Interrupt Overflow Flag Clear Register (ADCIOVFC)

Table 12-18: ADC Interrupt Overflow Flag Clear Register (ADCIOVFC) Layout

ADCIOVFC (ADC Interrupt Overflow Flag Clear Register) Offset: 0xC Default: 0x00000000 Access: ADC -> ADCIOVFC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 INT15	14 INT14	13 INT13	12 INT12	11 INT11	10 INT10	9 INT9	8 INT8
7 INT7	6 INT6	5 INT5	4 INT4	3 INT3	2 INT2	1 INT1	0 INT0

Table 12-19: ADC Interrupt Overflow Flag Clear Register (ADCIOVFC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	INT15	W1C	0x0	ADC interrupt 15 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
14	INT14	W1C	0x0	ADC interrupt 14 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
13	INT13	W1C	0x0	ADC interrupt 13 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
12	INT12	W1C	0x0	ADC interrupt 12 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
11	INT11	W1C	0x0	ADC interrupt 11 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
10	INT10	W1C	0x0	ADC interrupt 10 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
9	INT9	W1C	0x0	ADC interrupt 9 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
8	INT8	W1C	0x0	ADC interrupt 8 overflow flag clear 0: Write a 0 has no effect and always reads back 0

SPINTROL

Bits	Field Name	Type	Reset	Description
				1: Write a 1 clears the flag. This bit is self-cleared.
7	INT7	W1C	0x0	ADC interrupt 7 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
6	INT6	W1C	0x0	ADC interrupt 6 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
5	INT5	W1C	0x0	ADC interrupt 5 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
4	INT4	W1C	0x0	ADC interrupt 4 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
3	INT3	W1C	0x0	ADC interrupt 3 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
2	INT2	W1C	0x0	ADC interrupt 2 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
1	INT1	W1C	0x0	ADC interrupt 1 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
0	INT0	W1C	0x0	ADC interrupt 0 overflow flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.

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12.13.2.5 ADC Interrupt Enable Register (ADCIE)

Table 12-20: ADC Interrupt Enable Register (ADCIE) Layout

ADCIE (ADC Interrupt Enable Register) Offset: 0x10 Default: 0x00000000 Access: ADC -> ADCIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 INT15	14 INT14	13 INT13	12 INT12	11 INT11	10 INT10	9 INT9	8 INT8
7 INT7	6 INT6	5 INT5	4 INT4	3 INT3	2 INT2	1 INT1	0 INT0

Table 12-21: ADC Interrupt Enable Register (ADCIE) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	INT15	RW	0x0	ADC interrupt 15 enable 0: Disable ADC interrupt 15 1: Enable ADC interrupt 15
14	INT14	RW	0x0	ADC interrupt 14 enable 0: Disable ADC interrupt 14 1: Enable ADC interrupt 14
13	INT13	RW	0x0	ADC interrupt 13 enable 0: Disable ADC interrupt 13 1: Enable ADC interrupt 13
12	INT12	RW	0x0	ADC interrupt 12 enable 0: Disable ADC interrupt 12 1: Enable ADC interrupt 12
11	INT11	RW	0x0	ADC interrupt 11 enable 0: Disable ADC interrupt 11 1: Enable ADC interrupt 11
10	INT10	RW	0x0	ADC interrupt 10 enable 0: Disable ADC interrupt 10 1: Enable ADC interrupt 10
9	INT9	RW	0x0	ADC interrupt 9 enable 0: Disable ADC interrupt 9 1: Enable ADC interrupt 9
8	INT8	RW	0x0	ADC interrupt 8 enable 0: Disable ADC interrupt 8 1: Enable ADC interrupt 8

SPINTROL

Bits	Field Name	Type	Reset	Description
7	INT7	RW	0x0	ADC interrupt 7 enable 0: Disable ADC interrupt 7 1: Enable ADC interrupt 7
6	INT6	RW	0x0	ADC interrupt 6 enable 0: Disable ADC interrupt 6 1: Enable ADC interrupt 6
5	INT5	RW	0x0	ADC interrupt 5 enable 0: Disable ADC interrupt 5 1: Enable ADC interrupt 5
4	INT4	RW	0x0	ADC interrupt 4 enable 0: Disable ADC interrupt 4 1: Enable ADC interrupt 4
3	INT3	RW	0x0	ADC interrupt 3 enable 0: Disable ADC interrupt 3 1: Enable ADC interrupt 3
2	INT2	RW	0x0	ADC interrupt 2 enable 0: Disable ADC interrupt 2 1: Enable ADC interrupt 2
1	INT1	RW	0x0	ADC interrupt 1 enable 0: Disable ADC interrupt 1 1: Enable ADC interrupt 1
0	INT0	RW	0x0	ADC interrupt 0 enable 0: Disable ADC interrupt 0 1: Enable ADC interrupt 0

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12.13.2.6 ADC Start of Conversion Priority Control Register (ADCSOCPRICTL)

Table 12-22: ADC Start of Conversion Priority Control Register (ADCSOCPRICTL) Layout

ADCSOCPRICTL (ADC Start of Conversion Priority Control Register) Offset: 0x14 Default: 0x00000000 Access: ADC -> ADCSOCPRICTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				PRIORITY			

Table 12-23: ADC Start of Conversion Priority Control Register (ADCSOCPRICTL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3:0	PRIORITY	RW	0x0	SOC (Start of Conversion) Priority Determineds the cutoff point for priority mode and round arbitration of SOCs 0000: All SOCs priority follow the rule of round mode 0001: SOC0 are high priority SOC1-SOC15 is in round mode 0010: SOC0-SOC1 are high priority SOC2-SOC15 is in round mode 0011: SOC0-SOC2 are high priority SOC3-SOC15 is in round mode 0100: SOC0-SOC3 are high priority SOC4-SOC15 is in round mode 0101: SOC0-SOC4 are high priority SOC5-SOC15 is in round mode 0110: SOC0-SOC5 are high priority SOC6-SOC15 is in round mode 0111: SOC0-SOC6 are high priority SOC7-SOC15 is in round mode 1000: SOC0-SOC7 are high priority SOC8-SOC15 is in round mode 1001: SOC0-SOC8 are high priority SOC9-SOC15 is in round mode 1010: SOC0-SOC9 are high priority SOC10-SOC15 is in round mode 1011: SOC0-SOC10 are high priority SOC11-SOC15 is in round mode

SPINTROL

Bits	Field Name	Type	Reset	Description
				1100: SOC0-SOC11 are high priority SOC12-SOC15 is in round mode 1101: SOC0-SOC12 are high priority SOC13-SOC15 is in round mode 1110: SOC0-SOC13 are high priority SOC14-SOC15 is in round mode 1111: SOC0-SOC14 are high priority SOC15 is in round mode

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12.13.2.7 ADC SOC Flag Register (ADCSOCFLG)

Table 12-24: ADC SOC Flag Register (ADCSOCFLG) Layout

ADCSOCFLG (ADC SOC Flag Register) Offset: 0x18 Default: 0x00000000 Access: ADC -> ADCSOCFLG.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 SOC15	14 SOC14	13 SOC13	12 SOC12	11 SOC11	10 SOC10	9 SOC9	8 SOC8
7 SOC7	6 SOC6	5 SOC5	4 SOC4	3 SOC3	2 SOC2	1 SOC1	0 SOC0

Table 12-25: ADC SOC Flag Register (ADCSOCFLG) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	SOC15	RO	0x0	SOC15 (Start of Conversion) flag 0: No sample pending for SOC15 1: Trigger received and pend sample for SOC15. This bit is self-cleared when sample starts.
14	SOC14	RO	0x0	SOC14 (Start of Conversion) flag 0: No sample pending for SOC14 1: Trigger received and pend sample for SOC14. This bit is self-cleared when sample starts.
13	SOC13	RO	0x0	SOC13 (Start of Conversion) flag 0: No sample pending for SOC13 1: Trigger received and pend sample for SOC13. This bit is self-cleared when sample starts.
12	SOC12	RO	0x0	SOC12 (Start of Conversion) flag 0: No sample pending for SOC12 1: Trigger received and pend sample for SOC12. This bit is self-cleared when sample starts.
11	SOC11	RO	0x0	SOC11 (Start of Conversion) flag 0: No sample pending for SOC11 1: Trigger received and pend sample for SOC11. This bit is self-cleared when sample starts.
10	SOC10	RO	0x0	SOC10 (Start of Conversion) flag 0: No sample pending for SOC10 1: Trigger received and pend sample for SOC10. This bit is self-cleared when sample starts.
9	SOC9	RO	0x0	SOC9 (Start of Conversion) flag 0: No sample pending for SOC9

SPINTROL

Bits	Field Name	Type	Reset	Description
				1: Trigger received and pend sample for SOC9. This bit is self-cleared when sample starts.
8	SOC8	RO	0x0	SOC8 (Start of Conversion) flag 0: No sample pending for SOC8 1: Trigger received and pend sample for SOC8. This bit is self-cleared when sample starts.
7	SOC7	RO	0x0	SOC7 (Start of Conversion) flag 0: No sample pending for SOC7 1: Trigger received and pend sample for SOC7. This bit is self-cleared when sample starts.
6	SOC6	RO	0x0	SOC6 (Start of Conversion) flag 0: No sample pending for SOC6 1: Trigger received and pend sample for SOC6. This bit is self-cleared when sample starts.
5	SOC5	RO	0x0	SOC5 (Start of Conversion) flag 0: No sample pending for SOC5 1: Trigger received and pend sample for SOC5. This bit is self-cleared when sample starts.
4	SOC4	RO	0x0	SOC4 (Start of Conversion) flag 0: No sample pending for SOC4 1: Trigger received and pend sample for SOC4. This bit is self-cleared when sample starts.
3	SOC3	RO	0x0	SOC3 (Start of Conversion) flag 0: No sample pending for SOC3 1: Trigger received and pend sample for SOC3. This bit is self-cleared when sample starts.
2	SOC2	RO	0x0	SOC2 (Start of Conversion) flag 0: No sample pending for SOC2 1: Trigger received and pend sample for SOC2. This bit is self-cleared when sample starts.
1	SOC1	RO	0x0	SOC1 (Start of Conversion) flag 0: No sample pending for SOC1 1: Trigger received and pend sample for SOC1. This bit is self-cleared when sample starts.
0	SOC0	RO	0x0	SOC0 (Start of Conversion) flag 0: No sample pending for SOC0 1: Trigger received and pend sample for SOC0. This bit is self-cleared when sample starts.

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12.13.2.8 ADC SOC Force Register (ADCSOCFRC)

Table 12-26: ADC SOC Force Register (ADCSOCFRC) Layout

ADCSOCFRC (ADC SOC Force Register) Offset: 0x1C Default: 0x00000000 Access: ADC -> ADCSOCFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 SOC15	14 SOC14	13 SOC13	12 SOC12	11 SOC11	10 SOC10	9 SOC9	8 SOC8
7 SOC7	6 SOC6	5 SOC5	4 SOC4	3 SOC3	2 SOC2	1 SOC1	0 SOC0

Table 12-27: ADC SOC Force Register (ADCSOCFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	SOC15	W1S	0x0	SOC15 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC15. This bit is self-cleared.
14	SOC14	W1S	0x0	SOC14 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC14. This bit is self-cleared.
13	SOC13	W1S	0x0	SOC13 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC13. This bit is self-cleared.
12	SOC12	W1S	0x0	SOC12 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC12. This bit is self-cleared.
11	SOC11	W1S	0x0	SOC11 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC11. This bit is self-cleared.
10	SOC10	W1S	0x0	SOC10 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC10. This bit is self-cleared.
9	SOC9	W1S	0x0	SOC9 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC9. This bit is self-cleared.
8	SOC8	W1S	0x0	SOC8 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC8. This bit is self-cleared.

SPINTROL

Bits	Field Name	Type	Reset	Description
7	SOC7	W1S	0x0	SOC7 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC7. This bit is self-cleared.
6	SOC6	W1S	0x0	SOC6 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC6. This bit is self-cleared.
5	SOC5	W1S	0x0	SOC5 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC5. This bit is self-cleared.
4	SOC4	W1S	0x0	SOC4 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC4. This bit is self-cleared.
3	SOC3	W1S	0x0	SOC3 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC3. This bit is self-cleared.
2	SOC2	W1S	0x0	SOC2 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC2. This bit is self-cleared.
1	SOC1	W1S	0x0	SOC1 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC1. This bit is self-cleared.
0	SOC0	W1S	0x0	SOC0 (Start of Conversion) flag force 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 forces SOC0. This bit is self-cleared.

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12.13.2.9 ADC SOC Overflow Register (ADCSOCOVF)

Table 12-28: ADC SOC Overflow Register (ADCSOCOVF) Layout

ADCSOCOVF (ADC SOC Overflow Register) Offset: 0x20 Default: 0x00000000 Access: ADC -> ADCSOCOVF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 SOC15	14 SOC14	13 SOC13	12 SOC12	11 SOC11	10 SOC10	9 SOC9	8 SOC8
7 SOC7	6 SOC6	5 SOC5	4 SOC4	3 SOC3	2 SOC2	1 SOC1	0 SOC0

Table 12-29: ADC SOC Overflow Register (ADCSOCOVF) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	SOC15	RO	0x0	SOC15 (Start of Conversion) overflow flag This indicates an SOC15 interrupt was generated while an existing SOC15 interrupt was already pending. This overflow flag can't stop SOC15 interrupts from being processing. It just show that a trigger was missed. 0: No SOC15 interrupt overflow 1: SOC15 interrupt overflow
14	SOC14	RO	0x0	SOC14 (Start of Conversion) overflow flag 0: No SOC14 interrupt overflow 1: SOC14 interrupt overflow
13	SOC13	RO	0x0	SOC13 (Start of Conversion) overflow flag 0: No SOC13 interrupt overflow 1: SOC13 interrupt overflow
12	SOC12	RO	0x0	SOC12 (Start of Conversion) overflow flag 0: No SOC12 interrupt overflow 1: SOC12 interrupt overflow
11	SOC11	RO	0x0	SOC11 (Start of Conversion) overflow flag 0: No SOC11 interrupt overflow 1: SOC11 interrupt overflow
10	SOC10	RO	0x0	SOC10 (Start of Conversion) overflow flag 0: No SOC10 interrupt overflow 1: SOC10 interrupt overflow
9	SOC9	RO	0x0	SOC9 (Start of Conversion) overflow flag 0: No SOC9 interrupt overflow 1: SOC9 interrupt overflow

SPINTROL

Bits	Field Name	Type	Reset	Description
8	SOC8	RO	0x0	SOC8 (Start of Conversion) overflow flag 0: No SOC8 interrupt overflow 1: SOC8 interrupt overflow
7	SOC7	RO	0x0	SOC7 (Start of Conversion) overflow flag 0: No SOC7 interrupt overflow 1: SOC7 interrupt overflow
6	SOC6	RO	0x0	SOC6 (Start of Conversion) overflow flag 0: No SOC6 interrupt overflow 1: SOC6 interrupt overflow
5	SOC5	RO	0x0	SOC5 (Start of Conversion) overflow flag 0: No SOC5 interrupt overflow 1: SOC5 interrupt overflow
4	SOC4	RO	0x0	SOC4 (Start of Conversion) overflow flag 0: No SOC4 interrupt overflow 1: SOC4 interrupt overflow
3	SOC3	RO	0x0	SOC3 (Start of Conversion) overflow flag 0: No SOC3 interrupt overflow 1: SOC3 interrupt overflow
2	SOC2	RO	0x0	SOC2 (Start of Conversion) overflow flag 0: No SOC2 interrupt overflow 1: SOC2 interrupt overflow
1	SOC1	RO	0x0	SOC1 (Start of Conversion) overflow flag 0: No SOC1 interrupt overflow 1: SOC1 interrupt overflow
0	SOC0	RO	0x0	SOC0 (Start of Conversion) overflow flag 0: No SOC0 interrupt overflow 1: SOC0 interrupt overflow

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12.13.2.10 ADC SOC Overflow Clear Register (ADCSOCOVFC)

Table 12-30: ADC SOC Overflow Clear Register (ADCSOCOVFC) Layout

ADCSOCOVFC (ADC SOC Overflow Clear Register) Offset: 0x24 Default: 0x00000000 Access: ADC -> ADCSOCOVFC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 SOC15	14 SOC14	13 SOC13	12 SOC12	11 SOC11	10 SOC10	9 SOC9	8 SOC8
7 SOC7	6 SOC6	5 SOC5	4 SOC4	3 SOC3	2 SOC2	1 SOC1	0 SOC0

Table 12-31: ADC SOC Overflow Clear Register (ADCSOCOVFC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	SOC15	W1C	0x0	Clear SOC15 overflow flag If this bit receive a request to set from software and hardware try to set respective SOC15 overflow bit in ADCSOCOVF register simultaneously, then software has priority and ADCSOCOVF register will be cleared. 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
14	SOC14	W1C	0x0	Clear SOC14 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
13	SOC13	W1C	0x0	Clear SOC13 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
12	SOC12	W1C	0x0	Clear SOC12 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
11	SOC11	W1C	0x0	Clear SOC11 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
10	SOC10	W1C	0x0	Clear SOC10 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
9	SOC9	W1C	0x0	Clear SOC9 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.

SPINTROL

Bits	Field Name	Type	Reset	Description
8	SOC8	W1C	0x0	Clear SOC8 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
7	SOC7	W1C	0x0	Clear SOC7 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
6	SOC6	W1C	0x0	Clear SOC6 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
5	SOC5	W1C	0x0	Clear SOC5 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
4	SOC4	W1C	0x0	Clear SOC4 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
3	SOC3	W1C	0x0	Clear SOC3 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
2	SOC2	W1C	0x0	Clear SOC2 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
1	SOC1	W1C	0x0	Clear SOC1 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.
0	SOC0	W1C	0x0	Clear SOC0 overflow flag 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the flag. This bit is self-cleared.

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12.13.2.11 ADC Interrupt Trigger SOC Enable Register (ADCINTSOCEN)

Table 12-32: ADC Interrupt Trigger SOC Enable Register (ADCINTSOCEN) Layout

ADCINTSOCEN (ADC Interrupt Trigger SOC Enable Register) Offset: 0x28 Default: 0x00000000 Access: ADC -> ADCINTSOCEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
SOC15	SOC14	SOC13	SOC12	SOC11	SOC10	SOC9	SOC8
7	6	5	4	3	2	1	0
SOC7	SOC6	SOC5	SOC4	SOC3	SOC2	SOC1	SOC0

Table 12-33: ADC Interrupt Trigger SOC Enable Register (ADCINTSOCEN) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved.
15	SOC15	RW	0x0	ADC interrupt trigger SOC15 enable 0: ADCINTSOCSEL1.SOC15 is ignored 1: ADCSOCCTL15.TRIGSEL is overriden by ADCINTSOCSEL1.SOC15
14	SOC14	RW	0x0	ADC interrupt trigger SOC14 enable 0: ADCINTSOCSEL1.SOC14 is ignored 1: ADCSOCCTL14.TRIGSEL is overriden by ADCINTSOCSEL1.SOC14
13	SOC13	RW	0x0	ADC interrupt trigger SOC13 enable 0: ADCINTSOCSEL1.SOC13 is ignored 1: ADCSOCCTL13.TRIGSEL is overriden by ADCINTSOCSEL1.SOC13
12	SOC12	RW	0x0	ADC interrupt trigger SOC12 enable 0: ADCINTSOCSEL1.SOC12 is ignored 1: ADCSOCCTL12.TRIGSEL is overriden by ADCINTSOCSEL1.SOC12
11	SOC11	RW	0x0	ADC interrupt trigger SOC11 enable 0: ADCINTSOCSEL1.SOC11 is ignored 1: ADCSOCCTL11.TRIGSEL is overriden by ADCINTSOCSEL1.SOC11
10	SOC10	RW	0x0	ADC interrupt trigger SOC10 enable 0: ADCINTSOCSEL1.SOC10 is ignored 1: ADCSOCCTL10.TRIGSEL is overriden by ADCINTSOCSEL1.SOC10
9	SOC9	RW	0x0	ADC interrupt trigger SOC9 enable 0: ADCINTSOCSEL1.SOC9 is ignored

SPINTROL

Bits	Field Name	Type	Reset	Description
				1: ADCSOCCTL9.TRIGSEL is overriden by ADCINTSOCSEL1.SOC9
8	SOC8	RW	0x0	ADC interrupt trigger SOC8 enable 0: ADCINTSOCSEL0.SOC8 is ignored 1: ADCSOCCTL8.TRIGSEL is overriden by ADCINTSOCSEL1.SOC8
7	SOC7	RW	0x0	ADC interrupt trigger SOC7 enable 0: ADCINTSOCSEL0.SOC7 is ignored 1: ADCSOCCTL7.TRIGSEL is overriden by ADCINTSOCSEL0.SOC7
6	SOC6	RW	0x0	ADC interrupt trigger SOC6 enable 0: ADCINTSOCSEL0.SOC6 is ignored 1: ADCSOCCTL6.TRIGSEL is overriden by ADCINTSOCSEL0.SOC6
5	SOC5	RW	0x0	ADC interrupt trigger SOC5 enable 0: ADCINTSOCSEL0.SOC5 is ignored 1: ADCSOCCTL5.TRIGSEL is overriden by ADCINTSOCSEL0.SOC5
4	SOC4	RW	0x0	ADC interrupt trigger SOC4 enable 0: ADCINTSOCSEL0.SOC4 is ignored 1: ADCSOCCTL4.TRIGSEL is overriden by ADCINTSOCSEL0.SOC4
3	SOC3	RW	0x0	ADC interrupt trigger SOC3 enable 0: ADCINTSOCSEL0.SOC3 is ignored 1: ADCSOCCTL3.TRIGSEL is overriden by ADCINTSOCSEL0.SOC3
2	SOC2	RW	0x0	ADC interrupt trigger SOC2 enable 0: ADCINTSOCSEL0.SOC2 is ignored 1: ADCSOCCTL2.TRIGSEL is overriden by ADCINTSOCSEL0.SOC2
1	SOC1	RW	0x0	ADC interrupt trigger SOC1 enable 0: ADCINTSOCSEL0.SOC1 is ignored 1: ADCSOCCTL1.TRIGSEL is overriden by ADCINTSOCSEL0.SOC1
0	SOC0	RW	0x0	ADC interrupt trigger SOC0 enable 0: ADCINTSOCSEL0.SOC0 is ignored 1: ADCSOCCTL0.TRIGSEL is overriden by ADCINTSOCSEL0.SOC0

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12.13.2.12 ADC Interrupt Trigger SOC Select Register 0 (ADCINTSOCSEL0)

Table 12-34: ADC Interrupt Trigger SOC Select Register 0 (ADCINTSOCSEL0) Layout

ADCINTSOCSEL0 (ADC Interrupt Trigger SOC Select Register 0) Offset: 0x2C Default: 0x00000000
Access: ADC -> ADCINTSOCSEL0.all

31	30	29	28	27	26	25	24
SOC7				SOC6			
23	22	21	20	19	18	17	16
SOC5				SOC4			
15	14	13	12	11	10	9	8
SOC3				SOC2			
7	6	5	4	3	2	1	0
SOC1				SOC0			

Table 12-35: ADC Interrupt Trigger SOC Select Register 0 (ADCINTSOCSEL0) Field Description

Bits	Field Name	Type	Reset	Description
31:28	SOC7	RW	0x0	ADC interrupt number for SOC7
27:24	SOC6	RW	0x0	ADC interrupt number for SOC6
23:20	SOC5	RW	0x0	ADC interrupt number for SOC5
19:16	SOC4	RW	0x0	ADC interrupt number for SOC4
15:12	SOC3	RW	0x0	ADC interrupt number for SOC3
11:8	SOC2	RW	0x0	ADC interrupt number for SOC2
7:4	SOC1	RW	0x0	ADC interrupt number for SOC1
3:0	SOC0	RW	0x0	ADC interrupt number for SOC0

SPINTROL

12.13.2.13 ADC Interrupt Trigger SOC Select Register 1 (ADCINTSOCSEL1)

Table 12-36: ADC Interrupt Trigger SOC Select Register 1 (ADCINTSOCSEL1) Layout

ADCINTSOCSEL1 (ADC Interrupt Trigger SOC Select Register 1) Offset: 0x30 Default: 0x00000000 Access: ADC -> ADCINTSOCSEL1.all							
31	30	29	28	27	26	25	24
SOC15				SOC14			
23	22	21	20	19	18	17	16
SOC13				SOC12			
15	14	13	12	11	10	9	8
SOC11				SOC10			
7	6	5	4	3	2	1	0
SOC9				SOC8			

Table 12-37: ADC Interrupt Trigger SOC Select Register 1 (ADCINTSOCSEL1) Field Description

Bits	Field Name	Type	Reset	Description
31:28	SOC15	RW	0x0	ADC interrupt number for SOC15
27:24	SOC14	RW	0x0	ADC interrupt number for SOC14
23:20	SOC13	RW	0x0	ADC interrupt number for SOC13
19:16	SOC12	RW	0x0	ADC interrupt number for SOC12
15:12	SOC11	RW	0x0	ADC interrupt number for SOC11
11:8	SOC10	RW	0x0	ADC interrupt number for SOC10
7:4	SOC9	RW	0x0	ADC interrupt number for SOC9
3:0	SOC8	RW	0x0	ADC interrupt number for SOC8

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12.13.2.14 ADC External SOC Input Control Register (ADCEXTSOCCTL)

Table 12-38: ADC External SOC Input Control Register (ADCEXTSOCCTL) Layout

ADCEXTSOCCTL (ADC External SOC Input Control Register) Offset: 0x34 Default: 0x0000007F Access: ADC -> ADCEXTSOCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	POL	IOSEL					

Table 12-39: ADC External SOC Input Control Register (ADCEXTSOCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	POL	RW	0x1	EXTSOC polarity 0: Active when low 1: Active when high
5:0	IOSEL	RW	0x3F	GPIO number for EXTSOC

SPINTROL

12.13.2.15 ADC SOC0 Control Register (ADCSOCCTL0)

Table 12-40: ADC SOC0 Control Register (ADCSOCCTL0) Layout

ADCSOCCTL0 (ADC SOC0 Control Register) Offset: 0x38 Default: 0x00000000
Access: ADC -> ADCSOCCTL0.all

31	30	29	28	27	26	25	24
SHEN			TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-41: ADC SOC0 Control Register (ADCSOCCTL0) Field Description

Bits	Field Name	Type	Reset	Description
31:29	SHEN	RW	0x0	SH enable 000: Disable all SHs 001: Enable SHA 010: Enable SHB 011: Enable SHC 100: Enable SHA and SHB simultaneously 101: Enable SHB and SHC simultaneously 110: Enable SHA and SHC simultaneously 111: Enable SHA, SHB, SHC simultaneously
28:24	TRIGSEL	RW	0x0	Select SOC0 trigger source It can be overridden by ADCINTSOCSEL0.SOC0. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA 10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC

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Bits	Field Name	Type	Reset	Description
				10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC0
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC0 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC0 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC0 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC0 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.16 ADC SOC1 Control Register (ADCSOCCTL1)

Table 12-42: ADC SOC1 Control Register (ADCSOCCTL1) Layout

ADCSOCCTL1 (ADC SOC1 Control Register) Offset: 0x3C Default: 0x00000000
Access: ADC -> ADCSOCCTL1.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-43: ADC SOC1 Control Register (ADCSOCCTL1) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL0.SHEN is set to 4, 5 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC1 trigger source It can be overridden by ADCINTSOCSEL0.SOC1. This field is not used when ADCSOCCTL0.SHEN is set to 4, 5 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC1
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC1 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL0.SHEN is set to 4, 5 or 7, SHB is controlled for SOC0 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC1 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL0.SHEN is set to 4, 5 or 7, SHB is controlled for SOC0 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC1 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC1 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.17 ADC SOC2 Control Register (ADCSOCCTL2)

Table 12-44: ADC SOC2 Control Register (ADCSOCCTL2) Layout

ADCSOCCTL2 (ADC SOC2 Control Register) Offset: 0x40 Default: 0x00000000
Access: ADC -> ADCSOCCTL2.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-45: ADC SOC2 Control Register (ADCSOCCTL2) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL0.SHEN is set to 5, 6 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC2 trigger source It can be overridden by ADCINTSOCSEL0.SOC2. This field is not used when ADCSOCCTL0.SHEN is set to 5, 6 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC2
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC2 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL0.SHEN is set to 5, 6 or 7, SHC is controlled for SOC0 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC2 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL0.SHEN is set to 5, 6 or 7, SHC is controlled for SOC0 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC2 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC2 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.18 ADC SOC3 Control Register (ADCSOCCTL3)

Table 12-46: ADC SOC3 Control Register (ADCSOCCTL3) Layout

ADCSOCCTL3 (ADC SOC3 Control Register) Offset: 0x44 Default: 0x00000000
Access: ADC -> ADCSOCCTL3.all

31	30	29	28	27	26	25	24
SHEN			TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-47: ADC SOC3 Control Register (ADCSOCCTL3) Field Description

Bits	Field Name	Type	Reset	Description
31:29	SHEN	RW	0x0	SH enable 000: Disable all SHs 001: Enable SHA 010: Enable SHB 011: Enable SHC 100: Enable SHA and SHB simultaneously 101: Enable SHB and SHC simultaneously 110: Enable SHA and SHC simultaneously 111: Enable SHA, SHB, SHC simultaneously
28:24	TRIGSEL	RW	0x0	Select SOC3 trigger source It can be overridden by ADCINTSOCSEL0.SOC3 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA 10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC

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Bits	Field Name	Type	Reset	Description
				10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC3
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC3 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC3 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC3 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC3 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.19 ADC SOC4 Control Register (ADCSOCCTL4)

Table 12-48: ADC SOC4 Control Register (ADCSOCCTL4) Layout

ADCSOCCTL4 (ADC SOC4 Control Register) Offset: 0x48 Default: 0x00000000
Access: ADC -> ADCSOCCTL4.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-49: ADC SOC4 Control Register (ADCSOCCTL4) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL3.SHEN is set to 4, 5 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC4 trigger source It can be overridden by the ADCINTSOCSEL0.SOC4 This field is not used when ADCSOCCTL3.SHEN is set to 4, 5 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC4
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC4 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL3.SHEN is set to 4, 5 or 7, SHB is controlled for SOC3 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC4 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL3.SHEN is set to 4, 5 or 7, SHB is controlled for SOC3 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC4 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC4 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.20 ADC SOC5 Control Register (ADCSOCCTL5)

Table 12-50: ADC SOC5 Control Register (ADCSOCCTL5) Layout

ADCSOCCTL5 (ADC SOC5 Control Register) Offset: 0x4C Default: 0x00000000
Access: ADC -> ADCSOCCTL5.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-51: ADC SOC5 Control Register (ADCSOCCTL5) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL3.SHEN is set to 5, 6 or 7 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC5 trigger source It can be overridden by ADCINTSOCSEL0.SOC5 This field is not used when ADCSOCCTL3.SHEN is set to 5, 6 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC5
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC5 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL3.SHEN is set to 5, 6 or 7, SHC is controlled for SOC3 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC5 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL3.SHEN is set to 5, 6 or 7, SHC is controlled for SOC3 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC0 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC0 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.21 ADC SOC6 Control Register (ADCSOCCTL6)

Table 12-52: ADC SOC6 Control Register (ADCSOCCTL6) Layout

ADCSOCCTL6 (ADC SOC6 Control Register) Offset: 0x50 Default: 0x00000000
Access: ADC -> ADCSOCCTL6.all

31	30	29	28	27	26	25	24
SHEN			TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-53: ADC SOC6 Control Register (ADCSOCCTL6) Field Description

Bits	Field Name	Type	Reset	Description
31:29	SHEN	RW	0x0	SH enable 000: Disable all SHs 001: Enable SHA 010: Enable SHB 011: Enable SHC 100: Enable SHA and SHB simultaneously 101: Enable SHB and SHC simultaneously 110: Enable SHA and SHC simultaneously 111: Enable SHA, SHB, SHC simultaneously
28:24	TRIGSEL	RW	0x0	Select SOC6 trigger source It can be overridden by ADCINTSOCSEL0.SOC6 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA 10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC

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Bits	Field Name	Type	Reset	Description
				10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC6
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC6 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC6 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC6 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC6 sample window is (SAMPCNT+1) ADC clocks

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12.13.2.22 ADC SOC7 Control Register (ADCSOCCTL7)

Table 12-54: ADC SOC7 Control Register (ADCSOCCTL7) Layout

ADCSOCCTL7 (ADC SOC7 Control Register) Offset: 0x54 Default: 0x00000000
Access: ADC -> ADCSOCCTL7.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-55: ADC SOC7 Control Register (ADCSOCCTL7) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL6.SHEN is set to 4, 5 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC7 trigger source It can be overridden by ADCINTSOCSEL0.SOC7. This field is not used when ADCSOCCTL6.SHEN is set to 4, 5 or 7 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC7
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC7 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL6.SHEN is set to 4, 5 or 7, SHB is controlled for SOC6 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC6 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL6.SHEN is set to 4, 5 or 7, SHB is controlled for SOC6 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC7 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC7 sample window is (SAMPCNT+1) ADC clocks

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12.13.2.23 ADC SOC8 Control Register (ADCSOCCTL8)

Table 12-56: ADC SOC8 Control Register (ADCSOCCTL8) Layout

ADCSOCCTL8 (ADC SOC8 Control Register) Offset: 0x58 Default: 0x00000000
Access: ADC -> ADCSOCCTL8.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-57: ADC SOC8 Control Register (ADCSOCCTL8) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL6.SHEN is set to 5, 6 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC8 trigger source It can be overridden by ADCINTSOCSEL1.SOC8 This field is not used when ADCSOCCTL6.SHEN is set to 5, 6 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC8
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC8 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL6.SHEN is set to 5, 6 or 7, SHC is controlled for SOC6 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC8 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL6.SHEN is set to 5, 6 or 7, SHC is controlled for SOC6 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC8 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC8 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.24 ADC SOC9 Control Register (ADCSOCCTL9)

Table 12-58: ADC SOC9 Control Register (ADCSOCCTL9) Layout

ADCSOCCTL9 (ADC SOC9 Control Register) Offset: 0x5C Default: 0x00000000
Access: ADC -> ADCSOCCTL9.all

31	30	29	28	27	26	25	24
SHEN			TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-59: ADC SOC9 Control Register (ADCSOCCTL9) Field Description

Bits	Field Name	Type	Reset	Description
31:29	SHEN	RW	0x0	SH enable 000: Disable all SHs 001: Enable SHA 010: Enable SHB 011: Enable SHC 100: Enable SHA and SHB simultaneously 101: Enable SHB and SHC simultaneously 110: Enable SHA and SHC simultaneously 111: Enable SHA, SHB, SHC simultaneously
28:24	TRIGSEL	RW	0x0	Select SOC9 trigger source It can be overridden by the ADCINTSOCSEL1.SOC9. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA 10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC

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Bits	Field Name	Type	Reset	Description
				10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC9
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC9 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC9 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC9 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC9 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.25 ADC SOC10 Control Register (ADCSOCCTL10)

Table 12-60: ADC SOC10 Control Register (ADCSOCCTL10) Layout

ADCSOCCTL10 (ADC SOC10 Control Register) Offset: 0x60 Default: 0x00000000
Access: ADC -> ADCSOCCTL10.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-61: ADC SOC10 Control Register (ADCSOCCTL10) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL9.SHEN is set to 4, 5 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC10 trigger source It can be overridden by ADCINTSOCSEL1.SOC10. This field is not used when ADCSOCCTL9.SHEN is set to 4, 5 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC others: Do not trigger SOC10
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH of SOC10 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL9.SHEN is set to 4, 5 or 7, SHB is controlled for SOC9 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC10 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL9.SHEN is set to 4, 5 or 7, SHB is controlled for SOC9 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC10 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC10 sample window is (SAMPCNT+1) ADC clocks

SPINTROL

12.13.2.26 ADC SOC11 Control Register (ADCSOCCTL11)

Table 12-62: ADC SOC11 Control Register (ADCSOCCTL11) Layout

ADCSOCCTL11 (ADC SOC11 Control Register) Offset: 0x64 Default: 0x00000000
Access: ADC -> ADCSOCCTL11.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-63: ADC SOC11 Control Register (ADCSOCCTL11) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL9.SHEN is set to 5, 6 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC11 trigger source It can be overridden by ADCINTSOCSEL1.SOC11. This field is not used when ADCSOCCTL9.SHEN is set to 5, 6 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC11
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH of SOC11 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL9.SHEN is set to 5, 6 or 7, SHC is controlled for SOC9 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC11 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL9.SHEN is set to 5, 6 or 7, SHC is controlled for SOC9 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC11 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC11 sample window is (SAMPCNT+1) ADC clocks

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12.13.2.27 ADC SOC12 Control Register (ADCSOCCTL12)

Table 12-64: ADC SOC12 Control Register (ADCSOCCTL12) Layout

ADCSOCCTL12 (ADC SOC12 Control Register) Offset: 0x68 Default: 0x00000000
Access: ADC -> ADCSOCCTL12.all

31	30	29	28	27	26	25	24
SHEN			TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-65: ADC SOC12 Control Register (ADCSOCCTL12) Field Description

Bits	Field Name	Type	Reset	Description
31:29	SHEN	RW	0x0	SH enable 000: Disable all SHs 001: Enable SHA 010: Enable SHB 011: Enable SHC 100: Enable SHA and SHB simultaneously 101: Enable SHB and SHC simultaneously 110: Enable SHA and SHC simultaneously 111: Enable SHA, SHB, SHC simultaneously
28:24	TRIGSEL	RW	0x0	Select SOC12 trigger source It can be overridden by the ADCINTSOCSEL1.SOC12. 0000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA 10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC

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Bits	Field Name	Type	Reset	Description
				10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC12
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC12 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC12 When SHEN=1, 4, 6 or 7, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When SHEN=5, this field is not used. Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC12 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC12 sample window is (SAMPCNT+1) ADC clocks

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12.13.2.28 ADC SOC13 Control Register (ADCSOCCTL13)

Table 12-66: ADC SOC13 Control Register (ADCSOCCTL13) Layout

ADCSOCCTL13 (ADC SOC13 Control Register) Offset: 0x6C Default: 0x00000000
Access: ADC -> ADCSOCCTL13.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-67: ADC SOC13 Control Register (ADCSOCCTL13) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL12.SHEN is set to 4, 5 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC13 trigger source It can be overridden by ADCINTSOCSEL1.SOC13. This field is not used when ADCSOCCTL12.SHEN is set to 4, 5 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC13
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH of SOC13 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL12.SHEN is set to 4, 5 or 7, SHB is controlled for SOC12 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC13 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL12.SHEN is set to 4, 5 or 7, SHB is controlled for SOC12 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC13 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC13 sample window is (SAMPCNT+1) ADC clocks

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12.13.2.29 ADC SOC14 Control Register (ADCSOCCTL14)

Table 12-68: ADC SOC14 Control Register (ADCSOCCTL14) Layout

ADCSOCCTL14 (ADC SOC14 Control Register) Offset: 0x70 Default: 0x00000000
Access: ADC -> ADCSOCCTL14.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-69: ADC SOC14 Control Register (ADCSOCCTL14) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable This field is not used when ADCSOCCTL12.SHEN is set to 5, 6 or 7. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC14 trigger source It can be overridden by ADCINTSOCSEL1.SOC14. This field is not used when ADCSOCCTL12.SHEN is set to 5, 6 or 7. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA

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Bits	Field Name	Type	Reset	Description
				10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC 10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC14
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH of SOC14 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL12.SHEN is set to 5, 6 or 7, SHC is controlled for SOC12 Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC14 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. When ADCSOCCTL12.SHEN is set to 5, 6 or 7, SHC is controlled for SOC12 Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC14 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC14 sample window is (SAMPCNT+1) ADC clocks

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12.13.2.30 ADC SOC15 Control Register (ADCSOCCTL15)

Table 12-70: ADC SOC15 Control Register (ADCSOCCTL15) Layout

ADCSOCCTL15 (ADC SOC15 Control Register) Offset: 0x74 Default: 0x00000000
Access: ADC -> ADCSOCCTL15.all

31	30	29	28	27	26	25	24
RESERVED	SHEN		TRIGSEL				
23	22	21	20	19	18	17	16
CHSELN			CHSELP			AVGCNT	
15	14	13	12	11	10	9	8
AVGCNT	CONVCNT						
7	6	5	4	3	2	1	0
SAMPCNT							

Table 12-71: ADC SOC15 Control Register (ADCSOCCTL15) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RO	0x0	Reserved
30:29	SHEN	RW	0x0	SH enable. 00: Disable all SHs 01: Enable SHA 10: Enable SHB 11: Enable SHC
28:24	TRIGSEL	RW	0x0	Select SOC15 trigger source It can be overridden by ADCINTSOCSEL1.SOC15. 00000: ADCTRIG0 – Software only 00001: ADCTRIG1 – CPU Timer 0 00010: ADCTRIG2 – CPU Timer 1 00011: ADCTRIG3 – CPU Timer 2 00100: ADCTRIG4 – EXTSOC 00101: ADCTRIG5 – PWM0SOCA 00110: ADCTRIG6 – PWM0SOCB 00111: ADCTRIG7 – PWM0SOCC 01000: ADCTRIG8 – PWM1SOCA 01001: ADCTRIG9 – PWM1SOCB 01010: ADCTRIG10 – PWM1SOCC 01011: ADCTRIG11 – PWM2SOCA 01100: ADCTRIG12 – PWM2SOCB 01101: ADCTRIG13 – PWM2SOCC 01110: ADCTRIG14 – PWM3SOCA 01111: ADCTRIG15 – PWM3SOCB 10000: ADCTRIG16 – PWM3SOCC 10001: ADCTRIG17 – PWM4SOCA 10010: ADCTRIG18 – PWM4SOCB 10011: ADCTRIG19 – PWM4SOCC 10100: ADCTRIG20 – PWM5SOCA 10101: ADCTRIG21 – PWM5SOCB 10110: ADCTRIG22 – PWM5SOCC

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Bits	Field Name	Type	Reset	Description
				10111: ADCTRIG23 – PWM6SOCA 11000: ADCTRIG24 – PWM6SOCB 11001: ADCTRIG25 – PWM6SOCC 11010: ADCTRIG26 – PWM7SOCA 11011: ADCTRIG27 – PWM7SOCB 11100: ADCTRIG28 – PWM7SOCC Others: Do not trigger SOC15
23:21	CHSELN	RW	0x0	Select channel to negative terminal of SH for SOC15 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. Please see Table 12-4 for channel selection.
20:18	CHSELP	RW	0x0	Select channel to positive terminal of SH for SOC15 When SHEN=1, SHA is controlled. When SHEN=2, SHB is controlled. When SHEN=3, SHC is controlled. Please see Table 12-4 for channel selection.
17:15	AVGCNT	RW	0x0	Select average counts for the ADC result 000: No average 001: Each SOC will trigger 2 consecutive ADC operations and then average 010: Each SOC will trigger 4 consecutive ADC operations and then average 011: Each SOC will trigger 8 consecutive ADC operations and then average 100: Each SOC will trigger 16 consecutive ADC operations and then average 101: Each SOC will trigger 32 consecutive ADC operations and then average 110: Each SOC will trigger 64 consecutive ADC operations and then average 111: Each SOC will trigger 128 consecutive ADC operations and then average
14:8	CONVCNT	RW	0x0	SOC15 convert window is (CONVCNT+1) ADC clocks
7:0	SAMPCNT	RW	0x0	SOC15 sample window is (SAMPCNT+1) ADC clocks

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12.13.2.31 ADC Offset Trim Register 0 (ADCOFFSET0)

Table 12-72: ADC Offset Trim Register 0 (ADCOFFSET0) Layout

ADCOFFSET0 (ADC Offset Trim Register 0) Offset: 0x78 Default: 0x00000000 Access: ADC -> ADCOFFSET0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-73: ADC Offset Trim Register 0 (ADCOFFSET0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT0 Should be within [-8192, 8191]

12.13.2.32 ADC Offset Trim Register 1 (ADCOFFSET1)

Table 12-74: ADC Offset Trim Register 1 (ADCOFFSET1) Layout

ADCOFFSET1 (ADC Offset Trim Register 1) Offset: 0x7C Default: 0x00000000 Access: ADC -> ADCOFFSET1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-75: ADC Offset Trim Register 1 (ADCOFFSET1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT1 Should be within [-8192, 8191]

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12.13.2.33 ADC Offset Trim Register 2 (ADCOFFSET2)

Table 12-76: ADC Offset Trim Register 2 (ADCOFFSET2) Layout

ADCOFFSET2 (ADC Offset Trim Register 2) Offset: 0x80 Default: 0x00000000 Access: ADC -> ADCOFFSET2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-77: ADC Offset Trim Register 2 (ADCOFFSET2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT2 Should be within [-8192, 8191]

12.13.2.34 ADC Offset Trim Register 3 (ADCOFFSET3)

Table 12-78: ADC Offset Trim Register 3 (ADCOFFSET3) Layout

ADCOFFSET3 (ADC Offset Trim Register 3) Offset: 0x84 Default: 0x00000000 Access: ADC -> ADCOFFSET3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-79: ADC Offset Trim Register 3 (ADCOFFSET3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT3 Should be within [-8192, 8191]

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12.13.2.35 ADC Offset Trim Register 4 (ADCOFFSET4)

Table 12-80: ADC Offset Trim Register 4 (ADCOFFSET4) Layout

ADCOFFSET4 (ADC Offset Trim Register 4) Offset: 0x88 Default: 0x00000000 Access: ADC -> ADCOFFSET4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-81: ADC Offset Trim Register 4 (ADCOFFSET4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT4 Should be within [-8192, 8191]

12.13.2.36 ADC Offset Trim Register 5 (ADCOFFSET5)

Table 12-82: ADC Offset Trim Register 5 (ADCOFFSET5) Layout

ADCOFFSET5 (ADC Offset Trim Register 5) Offset: 0x8C Default: 0x00000000 Access: ADC -> ADCOFFSET5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-83: ADC Offset Trim Register 5 (ADCOFFSET5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT5 Should be within [-8192, 8191]

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12.13.2.37 ADC Offset Trim Register 6 (ADCOFFSET6)

Table 12-84: ADC Offset Trim Register 6 (ADCOFFSET6) Layout

ADCOFFSET6 (ADC Offset Trim Register 6) Offset: 0x90 Default: 0x00000000 Access: ADC -> ADCOFFSET6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-85: ADC Offset Trim Register 6 (ADCOFFSET6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT6 Should be within [-8192, 8191]

12.13.2.38 ADC Offset Trim Register 7 (ADCOFFSET7)

Table 12-86: ADC Offset Trim Register 7 (ADCOFFSET7) Layout

ADCOFFSET7 (ADC Offset Trim Register 7) Offset: 0x94 Default: 0x00000000 Access: ADC -> ADCOFFSET7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-87: ADC Offset Trim Register 7 (ADCOFFSET7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT7 Should be within [-8192, 8191]

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12.13.2.39 ADC Offset Trim Register 8 (ADCOFFSET8)

Table 12-88: ADC Offset Trim Register 8 (ADCOFFSET8) Layout

ADCOFFSET8 (ADC Offset Trim Register 8) Offset: 0x98 Default: 0x00000000 Access: ADC -> ADCOFFSET8.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-89: ADC Offset Trim Register 8 (ADCOFFSET8) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT8 Should be within [-8192, 8191]

12.13.2.40 ADC Offset Trim Register 9 (ADCOFFSET9)

Table 12-90: ADC Offset Trim Register 9 (ADCOFFSET9) Layout

ADCOFFSET9 (ADC Offset Trim Register 9) Offset: 0x9C Default: 0x00000000 Access: ADC -> ADCOFFSET9.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-91: ADC Offset Trim Register 9 (ADCOFFSET9) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT9 Should be within [-8192, 8191]

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12.13.2.41 ADC Offset Trim Register 10 (ADCOFFSET10)

Table 12-92: ADC Offset Trim Register 10 (ADCOFFSET10) Layout

ADCOFFSET10 (ADC Offset Trim Register 10) Offset: 0xA0 Default: 0x00000000 Access: ADC -> ADCOFFSET10.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-93: ADC Offset Trim Register 10 (ADCOFFSET10) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT10 Should be within [-8192, 8191]

12.13.2.42 ADC Offset Trim Register 11 (ADCOFFSET11)

Table 12-94: ADC Offset Trim Register 11 (ADCOFFSET11) Layout

ADCOFFSET11 (ADC Offset Trim Register 11) Offset: 0xA4 Default: 0x00000000 Access: ADC -> ADCOFFSET11.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-95: ADC Offset Trim Register 11 (ADCOFFSET11) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT11 Should be within [-8192, 8191]

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12.13.2.43 ADC Offset Trim Register 12 (ADCOFFSET12)

Table 12-96: ADC Offset Trim Register 12 (ADCOFFSET12) Layout

ADCOFFSET12 (ADC Offset Trim Register 12) Offset: 0xA8 Default: 0x00000000 Access: ADC -> ADCOFFSET12.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-97: ADC Offset Trim Register 12 (ADCOFFSET12) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT12 Should be within [-8192, 8191]

12.13.2.44 ADC Offset Trim Register 13 (ADCOFFSET13)

Table 12-98: ADC Offset Trim Register 13 (ADCOFFSET13) Layout

ADCOFFSET13 (ADC Offset Trim Register 13) Offset: 0xAC Default: 0x00000000 Access: ADC -> ADCOFFSET13.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-99: ADC Offset Trim Register 13 (ADCOFFSET13) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT13 Should be within [-8192, 8191]

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12.13.2.45 ADC Offset Trim Register 14 (ADCOFFSET14)

Table 12-100: ADC Offset Trim Register 14 (ADCOFFSET14) Layout

ADCOFFSET14 (ADC Offset Trim Register 14) Offset: 0xB0 Default: 0x00000000 Access: ADC -> ADCOFFSET14.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-101: ADC Offset Trim Register 14 (ADCOFFSET14) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT14 Should be within [-8192, 8191]

12.13.2.46 ADC Offset Trim Register 15 (ADCOFFSET15)

Table 12-102: ADC Offset Trim Register 15 (ADCOFFSET15) Layout

ADCOFFSET15 (ADC Offset Trim Register 15) Offset: 0xB4 Default: 0x00000000 Access: ADC -> ADCOFFSET15.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-103: ADC Offset Trim Register 15 (ADCOFFSET15) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for ADCRESULT15 Should be within [-8192, 8191]

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12.13.2.47 ADC Gain Trim Register 0 (ADCGAIN0)

Table 12-104: ADC Gain Trim Register 0 (ADCGAIN0) Layout

ADCGAIN0 (ADC Gain Trim Register 0) Offset: 0xB8 Default: 0x00008000 Access: ADC -> ADCGAIN0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-105: ADC Gain Trim Register 0 (ADCGAIN0) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT0

12.13.2.48 ADC Gain Trim Register 1 (ADCGAIN1)

Table 12-106: ADC Gain Trim Register 1 (ADCGAIN1) Layout

ADCGAIN1 (ADC Gain Trim Register 1) Offset: 0xBC Default: 0x00008000 Access: ADC -> ADCGAIN1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-107: ADC Gain Trim Register 1 (ADCGAIN1) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT1

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12.13.2.49 ADC Gain Trim Register 2 (ADCGAIN2)

Table 12-108: ADC Gain Trim Register 2 (ADCGAIN2) Layout

ADCGAIN2 (ADC Gain Trim Register 2) Offset: 0xC0 Default: 0x00008000 Access: ADC -> ADCGAIN2.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-109: ADC Gain Trim Register 2 (ADCGAIN2) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT2

12.13.2.50 ADC Gain Trim Register 3 (ADCGAIN3)

Table 12-110: ADC Gain Trim Register 3 (ADCGAIN3) Layout

ADCGAIN3 (ADC Gain Trim Register 3) Offset: 0xC4 Default: 0x00008000 Access: ADC -> ADCGAIN3.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-111: ADC Gain Trim Register 3 (ADCGAIN3) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT3

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12.13.2.51 ADC Gain Trim Register 4 (ADCGAIN4)

Table 12-112: ADC Gain Trim Register 4 (ADCGAIN4) Layout

ADCGAIN4 (ADC Gain Trim Register 4) Offset: 0xC8 Default: 0x00008000 Access: ADC -> ADCGAIN4.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-113: ADC Gain Trim Register 4 (ADCGAIN4) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT4

12.13.2.52 ADC Gain Trim Register 5 (ADCGAIN5)

Table 12-114: ADC Gain Trim Register 5 (ADCGAIN5) Layout

ADCGAIN5 (ADC Gain Trim Register 5) Offset: 0xCC Default: 0x00008000 Access: ADC -> ADCGAIN5.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-115: ADC Gain Trim Register 5 (ADCGAIN5) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT5

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12.13.2.53 ADC Gain Trim Register 6 (ADCGAIN6)

Table 12-116: ADC Gain Trim Register 6 (ADCGAIN6) Layout

ADCGAIN6 (ADC Gain Trim Register 6) Offset: 0xD0 Default: 0x00008000 Access: ADC -> ADCGAIN6.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-117: ADC Gain Trim Register 6 (ADCGAIN6) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT6

12.13.2.54 ADC Gain Trim Register 7 (ADCGAIN7)

Table 12-118: ADC Gain Trim Register 7 (ADCGAIN7) Layout

ADCGAIN7 (ADC Gain Trim Register 7) Offset: 0xD4 Default: 0x00008000 Access: ADC -> ADCGAIN7.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-119: ADC Gain Trim Register 7 (ADCGAIN7) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT7

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12.13.2.55 ADC Gain Trim Register 8 (ADCGAIN8)

Table 12-120: ADC Gain Trim Register 8 (ADCGAIN8) Layout

ADCGAIN8 (ADC Gain Trim Register 8) Offset: 0xD8 Default: 0x00008000 Access: ADC -> ADCGAIN8.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-121: ADC Gain Trim Register 8 (ADCGAIN8) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT8

12.13.2.56 ADC Gain Trim Register 9 (ADCGAIN9)

Table 12-122: ADC Gain Trim Register 9 (ADCGAIN9) Layout

ADCGAIN9 (ADC Gain Trim Register 9) Offset: 0xDC Default: 0x00008000 Access: ADC -> ADCGAIN9.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-123: ADC Gain Trim Register 9 (ADCGAIN9) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT9

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12.13.2.57 ADC Gain Trim Register 10 (ADCGAIN10)

Table 12-124: ADC Gain Trim Register 10 (ADCGAIN10) Layout

ADCGAIN10 (ADC Gain Trim Register 10) Offset: 0xE0 Default: 0x00008000 Access: ADC -> ADCGAIN10.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-125: ADC Gain Trim Register 10 (ADCGAIN10) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT10

12.13.2.58 ADC Gain Trim Register 11 (ADCGAIN11)

Table 12-126: ADC Gain Trim Register 11 (ADCGAIN11) Layout

ADCGAIN11 (ADC Gain Trim Register 11) Offset: 0xE4 Default: 0x00008000 Access: ADC -> ADCGAIN11.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-127: ADC Gain Trim Register 11 (ADCGAIN11) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT11

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12.13.2.59 ADC Gain Trim Register 12 (ADCGAIN12)

Table 12-128: ADC Gain Trim Register 12 (ADCGAIN12) Layout

ADCGAIN12 (ADC Gain Trim Register 12) Offset: 0xE8 Default: 0x00008000 Access: ADC -> ADCGAIN12.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-129: ADC Gain Trim Register 12 (ADCGAIN12) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT12

12.13.2.60 ADC Gain Trim Register 13 (ADCGAIN13)

Table 12-130: ADC Gain Trim Register 13 (ADCGAIN13) Layout

ADCGAIN13 (ADC Gain Trim Register 13) Offset: 0xEC Default: 0x00008000 Access: ADC -> ADCGAIN13.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-131: ADC Gain Trim Register 13 (ADCGAIN13) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT13

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12.13.2.61 ADC Gain Trim Register 14 (ADCGAIN14)

Table 12-132: ADC Gain Trim Register 14 (ADCGAIN14) Layout

ADCGAIN14 (ADC Gain Trim Register 14) Offset: 0xF0 Default: 0x00008000 Access: ADC -> ADCGAIN14.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-133: ADC Gain Trim Register 14 (ADCGAIN14) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT14

12.13.2.62 ADC Gain Trim Register 15 (ADCGAIN15)

Table 12-134: ADC Gain Trim Register 15 (ADCGAIN15) Layout

ADCGAIN15 (ADC Gain Trim Register 15) Offset: 0xF4 Default: 0x00008000 Access: ADC -> ADCGAIN15.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-135: ADC Gain Trim Register 15 (ADCGAIN15) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for ADCRESULT15

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12.13.2.63 ADC SHA Offset Trim Register (ADCOFFSETA)

Table 12-136: ADC SHA Offset Trim Register (ADCOFFSETA) Layout

ADCOFFSETA (ADC SHA Offset Trim Register) Offset: 0xF8 Default: 0x00000000 Access: ADC -> ADCOFFSETA.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-137: ADC SHA Offset Trim Register (ADCOFFSETA) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for SHA Should be within [-8192, 8191]

12.13.2.64 ADC SHB Offset Trim Register (ADCOFFSETB)

Table 12-138: ADC SHB Offset Trim Register (ADCOFFSETB) Layout

ADCOFFSETB (ADC SHB Offset Trim Register) Offset: 0xFC Default: 0x00000000 Access: ADC -> ADCOFFSETB.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-139: ADC SHB Offset Trim Register (ADCOFFSETB) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for SHB Should be within [-8192, 8191]

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12.13.2.65 ADC SHC Offset Trim Register (ADCOFFSETC)

Table 12-140: ADC SHC Offset Trim Register (ADCOFFSETC) Layout

ADCOFFSETC (ADC SHC Offset Trim Register) Offset: 0x100 Default: 0x00000000 Access: ADC -> ADCOFFSETC.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-141: ADC SHC Offset Trim Register (ADCOFFSETC) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Offset trimming (signed number) for SHC Should be within [-8192, 8191]

12.13.2.66 ADC SHA Gain Trim Register (ADCGAINA)

Table 12-142: ADC SHA Gain Trim Register (ADCGAINA) Layout

ADCGAINA (ADC SHA Gain Trim Register) Offset: 0x104 Default: 0x00008000 Access: ADC -> ADCGAINA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-143: ADC SHA Gain Trim Register (ADCGAINA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for SHA

SPINTROL

12.13.2.67 ADC SHB Gain Trim Register (ADCGAINB)

Table 12-144: ADC SHB Gain Trim Register (ADCGAINB) Layout

ADCGAINB (ADC SHB Gain Trim Register) Offset: 0x108 Default: 0x00008000 Access: ADC -> ADCGAINB.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-145: ADC SHB Gain Trim Register (ADCGAINB) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for SHB

12.13.2.68 ADC SHC Gain Trim Register (ADCGAINC)

Table 12-146: ADC SHC Gain Trim Register (ADCGAINC) Layout

ADCGAINC (ADC SHC Gain Trim Register) Offset: 0x10C Default: 0x00008000 Access: ADC -> ADCGAINC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-147: ADC SHC Gain Trim Register (ADCGAINC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8000	Gain trimming (VAL/32768) for SHC

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12.13.2.69 ADC Status Register (ADCSTS)

Table 12-148: ADC Status Register (ADCSTS) Layout

ADCSTS (ADC Status Register) Offset: 0x110 Default: 0x00000000 Access: ADC -> ADCSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					CODECRDY	CODEBRDY	CODEARDY

Table 12-149: ADC Status Register (ADCSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	CODECRDY	RO	0x0	ADCRAWCODEC ready flag 0: ADCRAWCODEC is not ready 1: ADCRAWCODEC is ready
1	CODEBRDY	RO	0x0	ADCRAWCODEB ready flag 0: ADCRAWCODEB is not ready 1: ADCRAWCODEB is ready
0	CODEARDY	RO	0x0	ADCRAWCODEA ready flag 0: ADCRAWCODEA is not ready 1: ADCRAWCODEA is ready

SPINTROL

12.13.2.70 ADC Status Clear Register (ADCSTSCLR)

Table 12-150: ADC Status Clear Register (ADCSTSCLR) Layout

ADCSTSCLR (ADC Status Clear Register) Offset: 0x114 Default: 0x00000000 Access: ADC -> ADCSTSCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					CODECRDY	CODEBRDY	CODEARDY

Table 12-151: ADC Status Clear Register (ADCSTSCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	CODECRDY	W1C	0x0	ADCRAWCODEC ready clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
1	CODEBRDY	W1C	0x0	ADCRAWCODEB ready clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.
0	CODEARDY	W1C	0x0	ADCRAWCODEA ready clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the flag. This bit is self-cleared.

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12.13.2.71 ADC Control Register (ADCCTL)

Table 12-152: ADC Control Register (ADCCTL) Layout

ADCCTL (ADC Control Register) Offset: 0x118 Default: 0x00000008 Access: ADC -> ADCCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
TIECN		TIECP		TIEBN		TIEBP	
7	6	5	4	3	2	1	0
TIEAN		TIEAP		SYNCEDGE	SYNCEN	RST	EN

Table 12-153: ADC Control Register (ADCCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved.
15:14	TIECN	RW	0x0	Force SHC negative input connection 00: Disable 01: Disable 10: Force SHC negative input tied low 11: Force SHC negative input tied high
13:12	TIECP	RW	0x0	Force SHC positive input connection 00: Disable 01: Disable 10: Force SHC positive input tied low 11: Force SHC positive input tied high
11:10	TIEBN	RW	0x0	Force SHB negative input connection 00: Disable 01: Disable 10: Force SHB negative input tied low 11: Force SHB negative input tied high
9:8	TIEBP	RW	0x0	Force SHB positive input connection 00: Disable 01: Disable 10: Force SHB positive input tied low 11: Force SHB positive input tied high
7:6	TIEAN	RW	0x0	Force SHA negative input connection 00: Disable 01: Disable 10: Force SHA negative input tied low 11: Force SHA negative input tied high

SPINTROL

Bits	Field Name	Type	Reset	Description
5:4	TIEAP	RW	0x0	Force SHA positive input connection 00: Disable 01: Disable 10: Force SHA positive input tied low 11: Force SHA positive input tied high
3	SYNCEDGE	RW	0x1	Clock edge for sample/convert control re-synchronization 0: Negative edge 1: Positve edge
2	SYNCEN	RW	0x0	Enable sample/convert control re-synchronization with local clean clock 0: Disable 1: Enable
1	RST	W1S	0x0	ADC digital reset 0: Write a 0 has no effect and always read back 0 1: Write a 1 reset the ADC digital part. This bit is self-cleared
0	EN	RW	0x0	ADC enable 0: Disable ADC 1: Enable ADC

12.13.2.72 ADC Bandgap Control Register (ADCBGCTL)

Table 12-154: ADC Bandgap Control Register (ADCBGCTL) Layout

ADCBGCTL (ADC Bandgap Control Register) Offset: 0x11C Default: 0x00000000 Access: ADC -> ADCBGCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							EN

Table 12-155: ADC Bandgap Control Register (ADCBGCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	EN	RW	0x0	ADC bandgap enable 0: Disable ADC bandgap 1: Enable ADC bandgap

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12.13.2.73 ADC Reference Control Register (ADCREFCTL)

Table 12-156: ADC Reference Control Register (ADCREFCTL) Layout

ADCREFCTL (ADC Reference Control Register) Offset: 0x120 Default: 0x00003D3C Access: ADC -> ADCREFCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED	VDDTRIM				VANATRIM		VDIGTRIM
7	6	5	4	3	2	1	0
VDIGTRIM	VREFTRIM					EXTREF	EN

Table 12-157: ADC Reference Control Register (ADCREFCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:15	RESERVED_31_15	RO	0x0	Reserved
14:11	VDDTRIM	RW	0x7	VDD trimming
10:9	VANATRIM	RW	0x2	VANA trimming
8:7	VDIGTRIM	RW	0x2	VDIG trimming
6:2	VREFTRIM	RW	0xF	VREF trimming
1	EXTREF	RW	0x0	External reference enable 0: Disable 1: Enable
0	EN	RW	0x0	Reference enable 0: Disable 1: Enable

SPINTROL

12.13.2.74 ADC SHA Raw Code Register (ADCRAWCODEA)

Table 12-158: ADC SHA Raw Code Register (ADCRAWCODEA) Layout

ADCRAWCODEA (ADC SHA Raw Code Register) Offset: 0x124 Default: 0x00000000 Access: ADC -> ADCRAWCODEA.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-159: ADC SHA Raw Code Register (ADCRAWCODEA) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Raw code (Signed number from -8192 to 8191) for SHA.

12.13.2.75 ADC SHB Raw Code Register (ADCRAWCODEB)

Table 12-160: ADC SHB Raw Code Register (ADCRAWCODEB) Layout

ADCRAWCODEB (ADC SHB Raw Code Register) Offset: 0x128 Default: 0x00000000 Access: ADC -> ADCRAWCODEB.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-161: ADC SHB Raw Code Register (ADCRAWCODEB) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Raw code (Signed number from -8192 to 8191) for SHB.

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12.13.2.76 ADC SHC Raw Code Register (ADCRAWCODEC)

Table 12-162: ADC SHC Raw Code Register (ADCRAWCODEC) Layout

ADCRAWCODEC (ADC SHC Raw Code Register) Offset: 0x12C Default: 0x00000000 Access: ADC -> ADCRAWCODEC.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-163: ADC SHC Raw Code Register (ADCRAWCODEC) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Raw code (Signed number from -8192 to 8191) for SHC.

12.13.2.77 ADC Result Register 0 (ADCRESULT0)

Table 12-164: ADC Result Register 0 (ADCRESULT0) Layout

ADCRESULT0 (ADC Result Register 0) Offset: 0x130 Default: 0x00000000 Access: ADC -> ADCRESULT0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-165: ADC Result Register 0 (ADCRESULT0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit. In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL0. In simultaneous sampling mode enabled by ADCSOCCTL0.SHEN, it is the result of SHA configured in ADCSOCCTL0

SPINTROL

12.13.2.78 ADC Result Register 1 (ADCRESULT1)

Table 12-166: ADC Result Register 1 (ADCRESULT1) Layout

ADCRESULT1 (ADC Result Register 1) Offset: 0x134 Default: 0x00000000 Access: ADC -> ADCRESULT1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-167: ADC Result Register 1 (ADCRESULT1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL1. In simultaneous sampling mode enabled by ADCSOCCTL0.SHEN, it is the result of SHB configured in ADCSOCCTL1

12.13.2.79 ADC Result Register 2 (ADCRESULT2)

Table 12-168: ADC Result Register 2 (ADCRESULT2) Layout

ADCRESULT2 (ADC Result Register 2) Offset: 0x138 Default: 0x00000000 Access: ADC -> ADCRESULT2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-169: ADC Result Register 2 (ADCRESULT2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL2. In simultaneous sampling mode enabled by ADCSOCCTL0.SHEN, it is the result of SHC configured in ADCSOCCTL2

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12.13.2.80 ADC Result Register 3 (ADCRESULT3)

Table 12-170: ADC Result Register 3 (ADCRESULT3) Layout

ADCRESULT3 (ADC Result Register 3) Offset: 0x13C Default: 0x00000000 Access: ADC -> ADCRESULT3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-171: ADC Result Register 3 (ADCRESULT3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL3. In simultaneous sampling mode enabled by ADCSOCCTL3.SHEN, it is the result of SHA configured in ADCSOCCTL3

12.13.2.81 ADC Result Register 4 (ADCRESULT4)

Table 12-172: ADC Result Register 4 (ADCRESULT4) Layout

ADCRESULT4 (ADC Result Register 4) Offset: 0x140 Default: 0x00000000 Access: ADC -> ADCRESULT4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-173: ADC Result Register 4 (ADCRESULT4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL4. In simultaneous sampling mode enabled by ADCSOCCTL3.SHEN, it is the result of SHB configured in ADCSOCCTL4

SPINTROL

12.13.2.82 ADC Result Register 5 (ADCRESULT5)

Table 12-174: ADC Result Register 5 (ADCRESULT5) Layout

ADCRESULT5 (ADC Result Register 5) Offset: 0x144 Default: 0x00000000 Access: ADC -> ADCRESULT5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-175: ADC Result Register 5 (ADCRESULT5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL5. In simultaneous sampling mode enabled by ADCSOCCTL3.SHEN, it is the result of SHC configured in ADCSOCCTL5

12.13.2.83 ADC Result Register 6 (ADCRESULT6)

Table 12-176: ADC Result Register 6 (ADCRESULT6) Layout

ADCRESULT6 (ADC Result Register 6) Offset: 0x148 Default: 0x00000000 Access: ADC -> ADCRESULT6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-177: ADC Result Register 6 (ADCRESULT6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL6. In simultaneous sampling mode enabled by ADCSOCCTL6.SHEN, it is the result of SHA configured in ADCSOCCTL6

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12.13.2.84 ADC Result Register 7 (ADCRESULT7)

Table 12-178: ADC Result Register 7 (ADCRESULT7) Layout

ADCRESULT7 (ADC Result Register 7) Offset: 0x14C Default: 0x00000000 Access: ADC -> ADCRESULT7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-179: ADC Result Register 7 (ADCRESULT7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL7. In simultaneous sampling mode enabled by ADCSOCCTL6.SHEN, it is the result of SHB configured in ADCSOCCTL7

12.13.2.85 ADC Result Register 8 (ADCRESULT8)

Table 12-180: ADC Result Register 8 (ADCRESULT8) Layout

ADCRESULT8 (ADC Result Register 8) Offset: 0x150 Default: 0x00000000 Access: ADC -> ADCRESULT8.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-181: ADC Result Register 8 (ADCRESULT8) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL8. In simultaneous sampling mode enabled by ADCSOCCTL6.SHEN, it is the result of SHC configured in ADCSOCCTL8

SPINTROL

12.13.2.86 ADC Result Register 9 (ADCRESULT9)

Table 12-182: ADC Result Register 9 (ADCRESULT9) Layout

ADCRESULT9 (ADC Result Register 9) Offset: 0x154 Default: 0x00000000 Access: ADC -> ADCRESULT9.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-183: ADC Result Register 9 (ADCRESULT9) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL9. In simultaneous sampling mode enabled by ADCSOCCTL9.SHEN, it is the result of SHA configured in ADCSOCCTL9

12.13.2.87 ADC Result Register 10 (ADCRESULT10)

Table 12-184: ADC Result Register 10 (ADCRESULT10) Layout

ADCRESULT10 (ADC Result Register 10) Offset: 0x158 Default: 0x00000000 Access: ADC -> ADCRESULT10.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-185: ADC Result Register 10 (ADCRESULT10) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL10. In simultaneous sampling mode enabled by ADCSOCCTL9.SHEN, it is the result of SHB configured in ADCSOCCTL10

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12.13.2.88 ADC Result Register 11 (ADCRESULT11)

Table 12-186: ADC Result Register 11 (ADCRESULT11) Layout

ADCRESULT11 (ADC Result Register 11) Offset: 0x15C Default: 0x00000000 Access: ADC -> ADCRESULT11.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-187: ADC Result Register 11 (ADCRESULT11) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL11. In simultaneous sampling mode enabled by ADCSOCCTL9.SHEN, it is the result of SHC configured in ADCSOCCTL11

12.13.2.89 ADC Result Register 12 (ADCRESULT12)

Table 12-188: ADC Result Register 12 (ADCRESULT12) Layout

ADCRESULT12 (ADC Result Register 12) Offset: 0x160 Default: 0x00000000 Access: ADC -> ADCRESULT12.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-189: ADC Result Register 12 (ADCRESULT12) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL12. In simultaneous sampling mode enabled by ADCSOCCTL12.SHEN, it is the result of SHA configured in ADCSOCCTL12

SPINTROL

12.13.2.90 ADC Result Register 13 (ADCRESULT13)

Table 12-190: ADC Result Register 13 (ADCRESULT13) Layout

ADCRESULT13 (ADC Result Register 13) Offset: 0x164 Default: 0x00000000 Access: ADC -> ADCRESULT13.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-191: ADC Result Register 13 (ADCRESULT13) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL13. In simultaneous sampling mode enabled by ADCSOCCTL12.SHEN, it is the result of SHB configured in ADCSOCCTL13

12.13.2.91 ADC Result Register 14 (ADCRESULT14)

Table 12-192: ADC Result Register 14 (ADCRESULT14) Layout

ADCRESULT14 (ADC Result Register 14) Offset: 0x168 Default: 0x00000000 Access: ADC -> ADCRESULT14.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-193: ADC Result Register 14 (ADCRESULT14) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL14. In simultaneous sampling mode enabled by ADCSOCCTL12.SHEN, it is the result of SHC configured in ADCSOCCTL14

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12.13.2.92 ADC Result Register 15 (ADCRESULT15)

Table 12-194: ADC Result Register 15 (ADCRESULT15) Layout

ADCRESULT15 (ADC Result Register 15) Offset: 0x16C Default: 0x00000000 Access: ADC -> ADCRESULT15.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-195: ADC Result Register 15 (ADCRESULT15) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	14-bit ADC result with extended sign bit In sequential mode, it is the result of the corresponding SH enabled in ADCSOCCTL15. Simultaneous sample mode is not supported.

12.13.2.93 ADCPPU0 Comparison Result Register (ADCPPURESULT0)

Table 12-196: ADCPPU0 Comparison Result Register (ADCPPURESULT0) Layout

ADCPPURESULT0 (ADCPPU0 Comparison Result Register) Offset: 0x170 Default: 0x00000000 Access: ADC -> ADCPPURESULT0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-197: ADCPPU0 Comparison Result Register (ADCPPURESULT0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

SPINTROL

12.13.2.94 ADCPPU1 Comparison Result Register (ADCPPURESULT1)

Table 12-198: ADCPPU1 Comparison Result Register (ADCPPURESULT1) Layout

ADCPPURESULT1 (ADCPPU1 Comparison Result Register) Offset: 0x174 Default: 0x00000000 Access: ADC -> ADCPPURESULT1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-199: ADCPPU1 Comparison Result Register (ADCPPURESULT1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

12.13.2.95 ADCPPU2 Comparison Result Register (ADCPPURESULT2)

Table 12-200: ADCPPU2 Comparison Result Register (ADCPPURESULT2) Layout

ADCPPURESULT2 (ADCPPU2 Comparison Result Register) Offset: 0x178 Default: 0x00000000 Access: ADC -> ADCPPURESULT2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-201: ADCPPU2 Comparison Result Register (ADCPPURESULT2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

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12.13.2.96 ADCPPU3 Comparison Result Register (ADCPPURESULT3)

Table 12-202: ADCPPU3 Comparison Result Register (ADCPPURESULT3) Layout

ADCPPURESULT3 (ADCPPU3 Comparison Result Register) Offset: 0x17C Default: 0x00000000 Access: ADC -> ADCPPURESULT3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-203: ADCPPU3 Comparison Result Register (ADCPPURESULT3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

12.13.2.97 ADCPPU4 Comparison Result Register (ADCPPURESULT4)

Table 12-204: ADCPPU4 Comparison Result Register (ADCPPURESULT4) Layout

ADCPPURESULT4 (ADCPPU4 Comparison Result Register) Offset: 0x180 Default: 0x00000000 Access: ADC -> ADCPPURESULT4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-205: ADCPPU4 Comparison Result Register (ADCPPURESULT4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

SPINTROL

12.13.2.98 ADCPPU5 Comparison Result Register (ADCPPURESULT5)

Table 12-206: ADCPPU5 Comparison Result Register (ADCPPURESULT5) Layout

ADCPPURESULT5 (ADCPPU5 Comparison Result Register) Offset: 0x184 Default: 0x00000000 Access: ADC -> ADCPPURESULT5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-207: ADCPPU5 Comparison Result Register (ADCPPURESULT5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

12.13.2.99 ADCPPU6 Comparison Result Register (ADCPPURESULT6)

Table 12-208: ADCPPU6 Comparison Result Register (ADCPPURESULT6) Layout

ADCPPURESULT6 (ADCPPU6 Comparison Result Register) Offset: 0x188 Default: 0x00000000 Access: ADC -> ADCPPURESULT6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-209: ADCPPU6 Comparison Result Register (ADCPPURESULT6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

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12.13.2.100 ADCPPU7 Comparison Result Register (ADCPPURESULT7)

Table 12-210: ADCPPU7 Comparison Result Register (ADCPPURESULT7) Layout

ADCPPURESULT7 (ADCPPU7 Comparison Result Register) Offset: 0x18C Default: 0x00000000 Access: ADC -> ADCPPURESULT7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-211: ADCPPU7 Comparison Result Register (ADCPPURESULT7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Comparison result with extended sign bit

12.13.2.101 ADCPPU0 SOC Delay Register (ADCPPUSOCDLY0)

Table 12-212: ADCPPU0 SOC Delay Register (ADCPPUSOCDLY0) Layout

ADCPPUSOCDLY0 (ADCPPU0 SOC Delay Register) Offset: 0x190 Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-213: ADCPPU0 SOC Delay Register (ADCPPUSOCDLY0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU0CTL.SOCSEL

SPINTROL

12.13.2.102 ADCPPU1 SOC Delay Register (ADCPPUSOCDLY1)

Table 12-214: ADCPPU1 SOC Delay Register (ADCPPUSOCDLY1) Layout

ADCPPUSOCDLY1 (ADCPPU1 SOC Delay Register) Offset: 0x194 Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-215: ADCPPU1 SOC Delay Register (ADCPPUSOCDLY1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU1CTL.SOCSEL

12.13.2.103 ADCPPU2 SOC Delay Register (ADCPPUSOCDLY2)

Table 12-216: ADCPPU2 SOC Delay Register (ADCPPUSOCDLY2) Layout

ADCPPUSOCDLY2 (ADCPPU2 SOC Delay Register) Offset: 0x198 Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-217: ADCPPU2 SOC Delay Register (ADCPPUSOCDLY2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU2CTL.SOCSEL

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12.13.2.104 ADCPPU3 SOC Delay Register (ADCPPUSOCDLY3)

Table 12-218: ADCPPU3 SOC Delay Register (ADCPPUSOCDLY3) Layout

ADCPPUSOCDLY3 (ADCPPU3 SOC Delay Register) Offset: 0x19C Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-219: ADCPPU3 SOC Delay Register (ADCPPUSOCDLY3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU3CTL.SOCSEL

12.13.2.105 ADCPPU4 SOC Delay Register (ADCPPUSOCDLY4)

Table 12-220: ADCPPU4 SOC Delay Register (ADCPPUSOCDLY4) Layout

ADCPPUSOCDLY4 (ADCPPU4 SOC Delay Register) Offset: 0x1A0 Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-221: ADCPPU4 SOC Delay Register (ADCPPUSOCDLY4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU4CTL.SOCSEL

SPINTROL

12.13.2.106 ADCPPU5 SOC Delay Register (ADCPPUSOCDLY5)

Table 12-222: ADCPPU5 SOC Delay Register (ADCPPUSOCDLY5) Layout

ADCPPUSOCDLY5 (ADCPPU5 SOC Delay Register) Offset: 0x1A4 Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-223: ADCPPU5 SOC Delay Register (ADCPPUSOCDLY5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU5CTL.SOCSEL

12.13.2.107 ADCPPU6 SOC Delay Register (ADCPPUSOCDLY6)

Table 12-224: ADCPPU6 SOC Delay Register (ADCPPUSOCDLY6) Layout

ADCPPUSOCDLY6 (ADCPPU6 SOC Delay Register) Offset: 0x1A8 Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-225: ADCPPU6 SOC Delay Register (ADCPPUSOCDLY6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU6CTL.SOCSEL

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12.13.2.108 ADCPPU7 SOC Delay Register (ADCPPUSOCDLY7)

Table 12-226: ADCPPU7 SOC Delay Register (ADCPPUSOCDLY7) Layout

ADCPPUSOCDLY7 (ADCPPU7 SOC Delay Register) Offset: 0x1AC Default: 0x00000000 Access: ADC -> ADCPPUSOCDLY7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-227: ADCPPU7 SOC Delay Register (ADCPPUSOCDLY7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	Delay from trigger to execution for SOC selected by ADCPPU7CTL.SOCSEL

SPINTROL

12.13.2.109 ADCPPU0 Interrupt Flag Register (ADCPPUIF0)

Table 12-228: ADCPPU0 Interrupt Flag Register (ADCPPUIF0) Layout

ADCPPUIF0 (ADCPPU0 Interrupt Flag Register) Offset: 0x1B0 Default: 0x00000000 Access: ADC -> ADCPPUIF0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-229: ADCPPU0 Interrupt Flag Register (ADCPPUIF0) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU0 interrupt flag 0: ADCPPU0 interrupt does not happen 1: ADCPPU0 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU0 zero-cross status 0: ADCPPU0 zero-cross does not happen 1: ADCPPU0 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU0 too-high status 0: ADCPPU0 too-high does not happen 1: ADCPPU0 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU0 too-low status 0: ADCPPU0 too-low does not happen 1: ADCPPU0 too-low happened Further event will not generate interrupt until this bit is cleared.

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12.13.2.110 ADCPPU1 Interrupt Flag Register (ADCPPUIF1)

Table 12-230: ADCPPU1 Interrupt Flag Register (ADCPPUIF1) Layout

ADCPPUIF1 (ADCPPU1 Interrupt Flag Register) Offset: 0x1B4 Default: 0x00000000 Access: ADC -> ADCPPUIF1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-231: ADCPPU1 Interrupt Flag Register (ADCPPUIF1) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU1 interrupt flag 0: ADCPPU1 interrupt does not happen 1: ADCPPU1 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU1 zero-cross status 0: ADCPPU1 zero-cross does not happen 1: ADCPPU1 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU1 too-high status 0: ADCPPU1 too-high does not happen 1: ADCPPU1 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU1 too-low status 0: ADCPPU1 too-low does not happen 1: ADCPPU1 too-low happened Further event will not generate interrupt until this bit is cleared.

SPINTROL

12.13.2.111 ADCPPU2 Interrupt Flag Register (ADCPPUIF2)

Table 12-232: ADCPPU2 Interrupt Flag Register (ADCPPUIF2) Layout

ADCPPUIF2 (ADCPPU2 Interrupt Flag Register) Offset: 0x1B8 Default: 0x00000000 Access: ADC -> ADCPPUIF2.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-233: ADCPPU2 Interrupt Flag Register (ADCPPUIF2) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU2 interrupt flag 0: ADCPPU2 interrupt does not happen 1: ADCPPU2 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU2 zero-cross status 0: ADCPPU2 zero-cross does not happen 1: ADCPPU2 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU2 too-high status 0: ADCPPU2 too-high does not happen 1: ADCPPU2 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU2 too-low status 0: ADCPPU2 too-low does not happen 1: ADCPPU2 too-low happened Further event will not generate interrupt until this bit is cleared.

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12.13.2.112 ADCPPU3 Interrupt Flag Register (ADCPPUIF3)

Table 12-234: ADCPPU3 Interrupt Flag Register (ADCPPUIF3) Layout

ADCPPUIF3 (ADCPPU3 Interrupt Flag Register) Offset: 0x1BC Default: 0x00000000 Access: ADC -> ADCPPUIF3.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-235: ADCPPU3 Interrupt Flag Register (ADCPPUIF3) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU3 interrupt flag 0: ADCPPU3 interrupt does not happen 1: ADCPPU3 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU3 zero-cross status 0: ADCPPU3 zero-cross does not happen 1: ADCPPU3 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU3 too-high status 0: ADCPPU3 too-high does not happen 1: ADCPPU3 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU3 too-low status 0: ADCPPU3 too-low does not happen 1: ADCPPU3 too-low happened Further event will not generate interrupt until this bit is cleared.

SPINTROL

12.13.2.113 ADCPPU4 Interrupt Flag Register (ADCPPUIF4)

Table 12-236: ADCPPU4 Interrupt Flag Register (ADCPPUIF4) Layout

ADCPPUIF4 (ADCPPU4 Interrupt Flag Register) Offset: 0x1C0 Default: 0x00000000 Access: ADC -> ADCPPUIF4.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-237: ADCPPU4 Interrupt Flag Register (ADCPPUIF4) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU4 interrupt flag 0: ADCPPU4 interrupt does not happen 1: ADCPPU4 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU4 zero-cross status 0: ADCPPU4 zero-cross does not happen 1: ADCPPU4 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU4 too-high status 0: ADCPPU4 too-high does not happen 1: ADCPPU4 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU4 too-low status 0: ADCPPU4 too-low does not happen 1: ADCPPU4 too-low happened Further event will not generate interrupt until this bit is cleared.

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12.13.2.114 ADCPPU5 Interrupt Flag Register (ADCPPUIF5)

Table 12-238: ADCPPU5 Interrupt Flag Register (ADCPPUIF5) Layout

ADCPPUIF5 (ADCPPU5 Interrupt Flag Register) Offset: 0x1C4 Default: 0x00000000 Access: ADC -> ADCPPUIF5.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-239: ADCPPU5 Interrupt Flag Register (ADCPPUIF5) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU5 interrupt flag 0: ADCPPU5 interrupt does not happen 1: ADCPPU5 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU5 zero-cross status 0: ADCPPU5 zero-cross does not happen 1: ADCPPU5 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU5 too-high status 0: ADCPPU5 too-high does not happen 1: ADCPPU5 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU5 too-low status 0: ADCPPU5 too-low does not happen 1: ADCPPU5 too-low happened Further event will not generate interrupt until this bit is cleared.

SPINTROL

12.13.2.115 ADCPPU6 Interrupt Flag Register (ADCPPUIF6)

Table 12-240: ADCPPU6 Interrupt Flag Register (ADCPPUIF6) Layout

ADCPPUIF6 (ADCPPU6 Interrupt Flag Register) Offset: 0x1C8 Default: 0x00000000 Access: ADC -> ADCPPUIF6.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-241: ADCPPU6 Interrupt Flag Register (ADCPPUIF6) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU6 interrupt flag 0: ADCPPU6 interrupt does not happen 1: ADCPPU6 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU6 zero-cross status 0: ADCPPU6 zero-cross does not happen 1: ADCPPU6 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU6 too-high status 0: ADCPPU6 too-high does not happen 1: ADCPPU6 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU6 too-low status 0: ADCPPU6 too-low does not happen 1: ADCPPU6 too-low happened Further event will not generate interrupt until this bit is cleared.

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12.13.2.116 ADCPPU7 Interrupt Flag Register (ADCPPUIF7)

Table 12-242: ADCPPU7 Interrupt Flag Register (ADCPPUIF7) Layout

ADCPPUIF7 (ADCPPU7 Interrupt Flag Register) Offset: 0x1CC Default: 0x00000000 Access: ADC -> ADCPPUIF7.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-243: ADCPPU7 Interrupt Flag Register (ADCPPUIF7) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	RO	0x0	ADCPPU7 interrupt flag 0: ADCPPU7 interrupt does not happen 1: ADCPPU7 interrupt happened Further interrupt will not be generated until this bit is cleared.
2	XZRO	RO	0x0	Latched ADCPPU7 zero-cross status 0: ADCPPU7 zero-cross does not happen 1: ADCPPU7 zero-cross happened Further event will not generate interrupt until this bit is cleared.
1	TZHI	RO	0x0	Latched ADCPPU7 too-high status 0: ADCPPU7 too-high does not happen 1: ADCPPU7 too-high happened Further event will not generate interrupt until this bit is cleared.
0	TZLO	RO	0x0	Latched ADCPPU7 too-low status 0: ADCPPU7 too-low does not happen 1: ADCPPU7 too-low happened Further event will not generate interrupt until this bit is cleared.

SPINTROL

12.13.2.117 ADCPPU0 Interrupt Clear Register (ADCPPUIC0)

Table 12-244: ADCPPU0 Interrupt Clear Register (ADCPPUIC0) Layout

ADCPPUIC0 (ADCPPU0 Interrupt Clear Register) Offset: 0x1D0 Default: 0x00000000 Access: ADC -> ADCPPUIC0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-245: ADCPPU0 Interrupt Clear Register (ADCPPUIC0) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU0 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU0IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU0 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU0IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU0 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU0IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU0 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU0IF.TZLO. This bit is self-cleared.

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12.13.2.118 ADCPPU1 Interrupt Clear Register (ADCPPUIC1)

Table 12-246: ADCPPU1 Interrupt Clear Register (ADCPPUIC1) Layout

ADCPPUIC1 (ADCPPU1 Interrupt Clear Register) Offset: 0x1D4 Default: 0x00000000 Access: ADC -> ADCPPUIC1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-247: ADCPPU1 Interrupt Clear Register (ADCPPUIC1) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU1 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU1IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU1 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU1IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU1 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU1IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU1 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU1IF.TZLO. This bit is self-cleared.

SPINTROL

12.13.2.119 ADCPPU2 Interrupt Clear Register (ADCPPUIC2)

Table 12-248: ADCPPU2 Interrupt Clear Register (ADCPPUIC2) Layout

ADCPPUIC2 (ADCPPU2 Interrupt Clear Register) Offset: 0x1D8 Default: 0x00000000 Access: ADC -> ADCPPUIC2.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-249: ADCPPU2 Interrupt Clear Register (ADCPPUIC2) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU2 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU2IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU2 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU2IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU2 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU2IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU2 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU2IF.TZLO. This bit is self-cleared.

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12.13.2.120 ADCPPU3 Interrupt Clear Register (ADCPPUIC3)

Table 12-250: ADCPPU3 Interrupt Clear Register (ADCPPUIC3) Layout

ADCPPUIC3 (ADCPPU3 Interrupt Clear Register) Offset: 0x1DC Default: 0x00000000 Access: ADC -> ADCPPUIC3.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-251: ADCPPU3 Interrupt Clear Register (ADCPPUIC3) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU3 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU3IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU3 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU3IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU3 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU3IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU3 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU3IF.TZLO. This bit is self-cleared.

SPINTROL

12.13.2.121 ADCPPU4 Interrupt Clear Register (ADCPPUIC4)

Table 12-252: ADCPPU4 Interrupt Clear Register (ADCPPUIC4) Layout

ADCPPUIC4 (ADCPPU4 Interrupt Clear Register) Offset: 0x1E0 Default: 0x00000000 Access: ADC -> ADCPPUIC4.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-253: ADCPPU4 Interrupt Clear Register (ADCPPUIC4) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU4 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU4IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU4 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU4IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU4 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU4IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU4 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU4IF.TZLO. This bit is self-cleared.

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12.13.2.122 ADCPPU5 Interrupt Clear Register (ADCPPUIC5)

Table 12-254: ADCPPU5 Interrupt Clear Register (ADCPPUIC5) Layout

ADCPPUIC5 (ADCPPU5 Interrupt Clear Register) Offset: 0x1E4 Default: 0x00000000 Access: ADC -> ADCPPUIC5.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-255: ADCPPU5 Interrupt Clear Register (ADCPPUIC5) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU5 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU5IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU5 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU5IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU5 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU5IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU5 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU5IF.TZLO. This bit is self-cleared.

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12.13.2.123 ADCPPU6 Interrupt Clear Register (ADCPPUIC6)

Table 12-256: ADCPPU6 Interrupt Clear Register (ADCPPUIC6) Layout

ADCPPUIC6 (ADCPPU6 Interrupt Clear Register) Offset: 0x1E8 Default: 0x00000000 Access: ADC -> ADCPPUIC6.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-257: ADCPPU6 Interrupt Clear Register (ADCPPUIC6) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU6 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU6IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU6 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU6IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU6 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU6IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU6 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU6IF.TZLO. This bit is self-cleared.

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12.13.2.124 ADCPPU7 Interrupt Clear Register (ADCPPUIC7)

Table 12-258: ADCPPU7 Interrupt Clear Register (ADCPPUIC7) Layout

ADCPPUIC7 (ADCPPU7 Interrupt Clear Register) Offset: 0x1EC Default: 0x00000000 Access: ADC -> ADCPPUIC7.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				INT	XZRO	TZHI	TZLO

Table 12-259: ADCPPU7 Interrupt Clear Register (ADCPPUIC7) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	INT	W1C	0x0	ADCPPU7 interrupt flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU7IF.INT. This bit is self-cleared.
2	XZRO	W1C	0x0	Latched ADCPPU7 zero-cross status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU7IF.XZRO. This bit is self-cleared.
1	TZHI	W1C	0x0	Latched ADCPPU7 too-high status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU7IF.TZHI. This bit is self-cleared.
0	TZLO	W1C	0x0	Latched ADCPPU7 too-low status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears ADCPPU7IF.TZLO. This bit is self-cleared.

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12.13.2.125 ADCPPU0 Interrupt Enable Register (ADCPPUIE0)

Table 12-260: ADCPPU0 Interrupt Enable Register (ADCPPUIE0) Layout

ADCPPUIE0 (ADCPPU0 Interrupt Enable Register) Offset: 0x1F0 Default: 0x00000000 Access: ADC -> ADCPPUIE0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-261: ADCPPU0 Interrupt Enable Register (ADCPPUIE0) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU0 zero-cross as ADCPPU0 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU0 too-high as ADCPPU0 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU0 too-low as ADCPPU0 interrupt source 0: Disable 1: Enable

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12.13.2.126 ADCPPU1 Interrupt Enable Register (ADCPPUIE1)

Table 12-262: ADCPPU1 Interrupt Enable Register (ADCPPUIE1) Layout

ADCPPUIE1 (ADCPPU1 Interrupt Enable Register) Offset: 0x1F4 Default: 0x00000000 Access: ADC -> ADCPPUIE1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-263: ADCPPU1 Interrupt Enable Register (ADCPPUIE1) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU1 zero-cross as ADCPPU1 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU1 too-high as ADCPPU1 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU1 too-low as ADCPPU1 interrupt source 0: Disable 1: Enable

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12.13.2.127 ADCPPU2 Interrupt Enable Register (ADCPPUIE2)

Table 12-264: ADCPPU2 Interrupt Enable Register (ADCPPUIE2) Layout

ADCPPUIE2 (ADCPPU2 Interrupt Enable Register) Offset: 0x1F8 Default: 0x00000000 Access: ADC -> ADCPPUIE2.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-265: ADCPPU2 Interrupt Enable Register (ADCPPUIE2) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU2 zero-cross as ADCPPU2 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU2 too-high as ADCPPU2 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU2 too-low as ADCPPU2 interrupt source 0: Disable 1: Enable

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12.13.2.128 ADCPPU3 Interrupt Enable Register (ADCPPUIE3)

Table 12-266: ADCPPU3 Interrupt Enable Register (ADCPPUIE3) Layout

ADCPPUIE3 (ADCPPU3 Interrupt Enable Register) Offset: 0x1FC Default: 0x00000000 Access: ADC -> ADCPPUIE3.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-267: ADCPPU3 Interrupt Enable Register (ADCPPUIE3) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU3 zero-cross as ADCPPU3 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU3 too-high as ADCPPU3 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU3 too-low as ADCPPU3 interrupt source 0: Disable 1: Enable

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12.13.2.129 ADCPPU4 Interrupt Enable Register (ADCPPUIE4)

Table 12-268: ADCPPU4 Interrupt Enable Register (ADCPPUIE4) Layout

ADCPPUIE4 (ADCPPU4 Interrupt Enable Register) Offset: 0x200 Default: 0x00000000 Access: ADC -> ADCPPUIE4.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-269: ADCPPU4 Interrupt Enable Register (ADCPPUIE4) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU4 zero-cross as ADCPPU4 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU4 too-high as ADCPPU4 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU4 too-low as ADCPPU4 interrupt source 0: Disable 1: Enable

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12.13.2.130 ADCPPU5 Interrupt Enable Register (ADCPPUIE5)

Table 12-270: ADCPPU5 Interrupt Enable Register (ADCPPUIE5) Layout

ADCPPUIE5 (ADCPPU5 Interrupt Enable Register) Offset: 0x204 Default: 0x00000000 Access: ADC -> ADCPPUIE5.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-271: ADCPPU5 Interrupt Enable Register (ADCPPUIE5) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU5 zero-cross as ADCPPU5 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU5 too-high as ADCPPU5 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU5 too-low as ADCPPU5 interrupt source 0: Disable 1: Enable

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12.13.2.131 ADCPPU6 Interrupt Enable Register (ADCPPUIE6)

Table 12-272: ADCPPU6 Interrupt Enable Register (ADCPPUIE6) Layout

ADCPPUIE6 (ADCPPU6 Interrupt Enable Register) Offset: 0x208 Default: 0x00000000 Access: ADC -> ADCPPUIE6.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-273: ADCPPU6 Interrupt Enable Register (ADCPPUIE6) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU6 zero-cross as ADCPPU6 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU6 too-high as ADCPPU6 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU6 too-low as ADCPPU6 interrupt source 0: Disable 1: Enable

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12.13.2.132 ADCPPU7 Interrupt Enable Register (ADCPPUIE7)

Table 12-274: ADCPPU7 Interrupt Enable Register (ADCPPUIE7) Layout

ADCPPUIE7 (ADCPPU7 Interrupt Enable Register) Offset: 0x20C Default: 0x00000000 Access: ADC -> ADCPPUIE7.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-275: ADCPPU7 Interrupt Enable Register (ADCPPUIE7) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU7 zero-cross as ADCPPU7 interrupt source 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU7 too-high as ADCPPU7 interrupt source 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU7 too-low as ADCPPU7 interrupt source 0: Disable 1: Enable

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12.13.2.133 ADCPPU0 Trip-Zone Event Enable Register (ADCPPUTZE0)

Table 12-276: ADCPPU0 Trip-Zone Event Enable Register (ADCPPUTZE0) Layout

ADCPPUTZE0 (ADCPPU0 Trip-Zone Event Enable Register) Offset: 0x210 Default: 0x00000000 Access: ADC -> ADCPPUTZE0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-277: ADCPPU0 Trip-Zone Event Enable Register (ADCPPUTZE0) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU0 zero-cross as ADCPPU0 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU0 too-high as ADCPPU0 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU0 too-low as ADCPPU0 trip-zone event 0: Disable 1: Enable

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12.13.2.134 ADCPPU1 Trip-Zone Event Enable Register (ADCPPUTZE1)

Table 12-278: ADCPPU1 Trip-Zone Event Enable Register (ADCPPUTZE1) Layout

ADCPPUTZE1 (ADCPPU1 Trip-Zone Event Enable Register) Offset: 0x214 Default: 0x00000000 Access: ADC -> ADCPPUTZE1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-279: ADCPPU1 Trip-Zone Event Enable Register (ADCPPUTZE1) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU1 zero-cross as ADCPPU1 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU1 too-high as ADCPPU1 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU1 too-low as ADCPPU1 trip-zone event 0: Disable 1: Enable

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12.13.2.135 ADCPPU2 Trip-Zone Event Enable Register (ADCPPUTZE2)

Table 12-280: ADCPPU2 Trip-Zone Event Enable Register (ADCPPUTZE2) Layout

ADCPPUTZE2 (ADCPPU2 Trip-Zone Event Enable Register) Offset: 0x218 Default: 0x00000000 Access: ADC -> ADCPPUTZE2.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-281: ADCPPU2 Trip-Zone Event Enable Register (ADCPPUTZE2) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU2 zero-cross as ADCPPU2 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU2 too-high as ADCPPU2 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU2 too-low as ADCPPU2 trip-zone event 0: Disable 1: Enable

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12.13.2.136 ADCPPU3 Trip-Zone Event Enable Register (ADCPPUTZE3)

Table 12-282: ADCPPU3 Trip-Zone Event Enable Register (ADCPPUTZE3) Layout

ADCPPUTZE3 (ADCPPU3 Trip-Zone Event Enable Register) Offset: 0x21C Default: 0x00000000 Access: ADC -> ADCPPUTZE3.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-283: ADCPPU3 Trip-Zone Event Enable Register (ADCPPUTZE3) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU3 zero-cross as ADCPPU3 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU3 too-high as ADCPPU3 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU3 too-low as ADCPPU3 trip-zone event 0: Disable 1: Enable

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12.13.2.137 ADCPPU4 Trip-Zone Event Enable Register (ADCPPUTZE4)

Table 12-284: ADCPPU4 Trip-Zone Event Enable Register (ADCPPUTZE4) Layout

ADCPPUTZE4 (ADCPPU4 Trip-Zone Event Enable Register) Offset: 0x220 Default: 0x00000000 Access: ADC -> ADCPPUTZE4.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-285: ADCPPU4 Trip-Zone Event Enable Register (ADCPPUTZE4) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU4 zero-cross as ADCPPU4 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU4 too-high as ADCPPU4 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU4 too-low as ADCPPU4 trip-zone event 0: Disable 1: Enable

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12.13.2.138 ADCPPU5 Trip-Zone Event Enable Register (ADCPPUTZE5)

Table 12-286: ADCPPU5 Trip-Zone Event Enable Register (ADCPPUTZE5) Layout

ADCPPUTZE5 (ADCPPU5 Trip-Zone Event Enable Register) Offset: 0x224 Default: 0x00000000 Access: ADC -> ADCPPUTZE5.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-287: ADCPPU5 Trip-Zone Event Enable Register (ADCPPUTZE5) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU5 zero-cross as ADCPPU5 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU5 too-high as ADCPPU5 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU5 too-low as ADCPPU5 trip-zone event 0: Disable 1: Enable

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12.13.2.139 ADCPPU6 Trip-Zone Event Enable Register (ADCPPUTZE6)

Table 12-288: ADCPPU6 Trip-Zone Event Enable Register (ADCPPUTZE6) Layout

ADCPPUTZE6 (ADCPPU6 Trip-Zone Event Enable Register) Offset: 0x228 Default: 0x00000000 Access: ADC -> ADCPPUTZE6.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-289: ADCPPU6 Trip-Zone Event Enable Register (ADCPPUTZE6) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU6 zero-cross as ADCPPU6 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU6 too-high as ADCPPU6 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU6 too-low as ADCPPU6 trip-zone event 0: Disable 1: Enable

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12.13.2.140 ADCPPU7 Trip-Zone Event Enable Register (ADCPPUTZE7)

Table 12-290: ADCPPU7 Trip-Zone Event Enable Register (ADCPPUTZE7) Layout

ADCPPUTZE7 (ADCPPU7 Trip-Zone Event Enable Register) Offset: 0x22C Default: 0x00000000 Access: ADC -> ADCPPUTZE7.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					XZRO	TZHI	TZLO

Table 12-291: ADCPPU7 Trip-Zone Event Enable Register (ADCPPUTZE7) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	XZRO	RW	0x0	Enable ADCPPU7 zero-cross as ADCPPU7 trip-zone event 0: Disable 1: Enable
1	TZHI	RW	0x0	Enable ADCPPU7 too-high as ADCPPU7 trip-zone event 0: Disable 1: Enable
0	TZLO	RW	0x0	Enable ADCPPU7 too-low as ADCPPU7 trip-zone event 0: Disable 1: Enable

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12.13.2.141 ADCPPU0 Control Register (ADCPPUCTL0)

Table 12-292: ADCPPU0 Control Register (ADCPPUCTL0) Layout

ADCPPUCTL0 (ADCPPU0 Control Register) Offset: 0x230 Default: 0x00000400 Access: ADC -> ADCPPUCTL0.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-293: ADCPPU0 Control Register (ADCPPUCTL0) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU0 result is the reference minus the selected result 1: ADCPPU0 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU0SOCDLY
1	CBCEN	RW	0x0	ADCPPU0 cycle-by-cycle clear enable 0: Disable ADCPPU0 cycle-by-cycle clear 1: Enable ADCPPU0 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU0 enable 0: Disable ADCPPU0 1: Enable ADCPPU0

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12.13.2.142 ADCPPU1 Control Register (ADCPPUCTL1)

Table 12-294: ADCPPU1 Control Register (ADCPPUCTL1) Layout

ADCPPUCTL1 (ADCPPU1 Control Register) Offset: 0x234 Default: 0x00000400 Access: ADC -> ADCPPUCTL1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-295: ADCPPU1 Control Register (ADCPPUCTL1) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU1 result is the reference minus the selected result 1: ADCPPU1 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU1SOCDLY
1	CBCEN	RW	0x0	ADCPPU1 cycle-by-cycle clear enable 0: Disable ADCPPU1 cycle-by-cycle clear 1: Enable ADCPPU1 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU1 enable 0: Disable ADCPPU1 1: Enable ADCPPU1

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12.13.2.143 ADCPPU2 Control Register (ADCPPUCTL2)

Table 12-296: ADCPPU2 Control Register (ADCPPUCTL2) Layout

ADCPPUCTL2 (ADCPPU2 Control Register) Offset: 0x238 Default: 0x00000400 Access: ADC -> ADCPPUCTL2.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-297: ADCPPU2 Control Register (ADCPPUCTL2) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU2 result is the reference minus the selected result 1: ADCPPU2 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU2SOCDLY
1	CBCEN	RW	0x0	ADCPPU2 cycle-by-cycle clear enable 0: Disable ADCPPU2 cycle-by-cycle clear 1: Enable ADCPPU2 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU2 enable 0: Disable ADCPPU2 1: Enable ADCPPU2

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12.13.2.144 ADCPPU3 Control Register (ADCPPUCTL3)

Table 12-298: ADCPPU3 Control Register (ADCPPUCTL3) Layout

ADCPPUCTL3 (ADCPPU3 Control Register) Offset: 0x23C Default: 0x00000400 Access: ADC -> ADCPPUCTL3.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-299: ADCPPU3 Control Register (ADCPPUCTL3) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU3 result is the reference minus the selected result 1: ADCPPU3 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU3SOCDLY
1	CBCEN	RW	0x0	ADCPPU3 cycle-by-cycle clear enable 0: Disable ADCPPU3 cycle-by-cycle clear 1: Enable ADCPPU3 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU3 enable 0: Disable ADCPPU3 1: Enable ADCPPU3

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12.13.2.145 ADCPPU4 Control Register (ADCPPUCTL4)

Table 12-300: ADCPPU4 Control Register (ADCPPUCTL4) Layout

ADCPPUCTL4 (ADCPPU4 Control Register) Offset: 0x240 Default: 0x00000400 Access: ADC -> ADCPPUCTL4.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-301: ADCPPU4 Control Register (ADCPPUCTL4) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU4 result is the reference minus the selected result 1: ADCPPU4 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU4SOCDLY
1	CBCEN	RW	0x0	ADCPPU4 cycle-by-cycle clear enable 0: Disable ADCPPU4 cycle-by-cycle clear 1: Enable ADCPPU4 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU4 enable 0: Disable ADCPPU4 1: Enable ADCPPU4

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12.13.2.146 ADCPPU5 Control Register (ADCPPUCTL5)

Table 12-302: ADCPPU5 Control Register (ADCPPUCTL5) Layout

ADCPPUCTL5 (ADCPPU5 Control Register) Offset: 0x244 Default: 0x00000400 Access: ADC -> ADCPPUCTL5.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-303: ADCPPU5 Control Register (ADCPPUCTL5) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU5 result is the reference minus the selected result 1: ADCPPU5 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU5SOCDLY
1	CBCEN	RW	0x0	ADCPPU5 cycle-by-cycle clear enable 0: Disable ADCPPU5 cycle-by-cycle clear 1: Enable ADCPPU5 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU5 enable 0: Disable ADCPPU5 1: Enable ADCPPU5

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12.13.2.147 ADCPPU6 Control Register (ADCPPUCTL6)

Table 12-304: ADCPPU6 Control Register (ADCPPUCTL6) Layout

ADCPPUCTL6 (ADCPPU6 Control Register) Offset: 0x248 Default: 0x00000400 Access: ADC -> ADCPPUCTL6.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-305: ADCPPU6 Control Register (ADCPPUCTL6) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU6 result is the reference minus the selected result 1: ADCPPU6 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU6SOCDLY
1	CBCEN	RW	0x0	ADCPPU6 cycle-by-cycle clear enable 0: Disable ADCPPU6 cycle-by-cycle clear 1: Enable ADCPPU6 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU6 enable 0: Disable ADCPPU6 1: Enable ADCPPU6

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12.13.2.148 ADCPPU7 Control Register (ADCPPUCTL7)

Table 12-306: ADCPPU7 Control Register (ADCPPUCTL7) Layout

ADCPPUCTL7 (ADCPPU7 Control Register) Offset: 0x24C Default: 0x00000400 Access: ADC -> ADCPPUCTL7.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED					POL	DATASEL	
7	6	5	4	3	2	1	0
DATASEL		SOCSEL				CBCEN	EN

Table 12-307: ADCPPU7 Control Register (ADCPPUCTL7) Field Description

Bits	Field Name	Type	Reset	Description
31:11	RESERVED_31_11	RO	0x0	Reserved
10	POL	RW	0x1	Polarity for comparison 0: ADCPPU7 result is the reference minus the selected result 1: ADCPPU7 result is the selected result minus the reference
9:6	DATASEL	RW	0x0	Select the ADC result to compare with the reference
5:2	SOCSEL	RW	0x0	Select the SOC signal to derive the ADCPPU7SOCDLY
1	CBCEN	RW	0x0	ADCPPU7 cycle-by-cycle clear enable 0: Disable ADCPPU7 cycle-by-cycle clear 1: Enable ADCPPU7 cycle-by-cycle clear
0	EN	RW	0x0	ADCPPU7 enable 0: Disable ADCPPU7 1: Enable ADCPPU7

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12.13.2.149 ADCPPU0 Reference Register (ADCPPUREF0)

Table 12-308: ADCPPU0 Reference Register (ADCPPUREF0) Layout

ADCPPUREF0 (ADCPPU0 Reference Register) Offset: 0x250 Default: 0x00000000 Access: ADC -> ADCPPUREF0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-309: ADCPPU0 Reference Register (ADCPPUREF0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

12.13.2.150 ADCPPU1 Reference Register (ADCPPUREF1)

Table 12-310: ADCPPU1 Reference Register (ADCPPUREF1) Layout

ADCPPUREF1 (ADCPPU1 Reference Register) Offset: 0x254 Default: 0x00000000 Access: ADC -> ADCPPUREF1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-311: ADCPPU1 Reference Register (ADCPPUREF1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

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12.13.2.151 ADCPPU2 Reference Register (ADCPPUREF2)

Table 12-312: ADCPPU2 Reference Register (ADCPPUREF2) Layout

ADCPPUREF2 (ADCPPU2 Reference Register) Offset: 0x258 Default: 0x00000000 Access: ADC -> ADCPPUREF2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-313: ADCPPU2 Reference Register (ADCPPUREF2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

12.13.2.152 ADCPPU3 Reference Register (ADCPPUREF3)

Table 12-314: ADCPPU3 Reference Register (ADCPPUREF3) Layout

ADCPPUREF3 (ADCPPU3 Reference Register) Offset: 0x25C Default: 0x00000000 Access: ADC -> ADCPPUREF3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-315: ADCPPU3 Reference Register (ADCPPUREF3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

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12.13.2.153 ADCPPU4 Reference Register (ADCPPUREF4)

Table 12-316: ADCPPU4 Reference Register (ADCPPUREF4) Layout

ADCPPUREF4 (ADCPPU4 Reference Register) Offset: 0x260 Default: 0x00000000 Access: ADC -> ADCPPUREF4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-317: ADCPPU4 Reference Register (ADCPPUREF4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

12.13.2.154 ADCPPU5 Reference Register (ADCPPUREF5)

Table 12-318: ADCPPU5 Reference Register (ADCPPUREF5) Layout

ADCPPUREF5 (ADCPPU5 Reference Register) Offset: 0x264 Default: 0x00000000 Access: ADC -> ADCPPUREF5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-319: ADCPPU5 Reference Register (ADCPPUREF5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

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12.13.2.155 ADCPPU6 Reference Register (ADCPPUREF6)

Table 12-320: ADCPPU6 Reference Register (ADCPPUREF6) Layout

ADCPPUREF6 (ADCPPU6 Reference Register) Offset: 0x268 Default: 0x00000000 Access: ADC -> ADCPPUREF6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-321: ADCPPU6 Reference Register (ADCPPUREF6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

12.13.2.156 ADCPPU7 Reference Register (ADCPPUREF7)

Table 12-322: ADCPPU7 Reference Register (ADCPPUREF7) Layout

ADCPPUREF7 (ADCPPU7 Reference Register) Offset: 0x26C Default: 0x00000000 Access: ADC -> ADCPPUREF7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-323: ADCPPU7 Reference Register (ADCPPUREF7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Reference with extended sign bit Should be within [-8192, 8191]

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12.13.2.157 ADCPPU0 Trip-Zone High-Side Threshold Register (ADCPPUTHH0)

Table 12-324: ADCPPU0 Trip-Zone High-Side Threshold Register (ADCPPUTHH0) Layout

ADCPPUTHH0 (ADCPPU0 Trip-Zone High-Side Threshold Register) Offset: 0x270 Default: 0x00000000 Access: ADC -> ADCPPUTHH0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-325: ADCPPU0 Trip-Zone High-Side Threshold Register (ADCPPUTHH0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.158 ADCPPU1 Trip-Zone High-Side Threshold Register (ADCPPUTHH1)

Table 12-326: ADCPPU1 Trip-Zone High-Side Threshold Register (ADCPPUTHH1) Layout

ADCPPUTHH1 (ADCPPU1 Trip-Zone High-Side Threshold Register) Offset: 0x274 Default: 0x00000000 Access: ADC -> ADCPPUTHH1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-327: ADCPPU1 Trip-Zone High-Side Threshold Register (ADCPPUTHH1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.159 ADCPPU2 Trip-Zone High-Side Threshold Register (ADCPPUTHH2)

Table 12-328: ADCPPU2 Trip-Zone High-Side Threshold Register (ADCPPUTHH2) Layout

ADCPPUTHH2 (ADCPPU2 Trip-Zone High-Side Threshold Register) Offset: 0x278 Default: 0x00000000 Access: ADC -> ADCPPUTHH2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-329: ADCPPU2 Trip-Zone High-Side Threshold Register (ADCPPUTHH2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.160 ADCPPU3 Trip-Zone High-Side Threshold Register (ADCPPUTHH3)

Table 12-330: ADCPPU3 Trip-Zone High-Side Threshold Register (ADCPPUTHH3) Layout

ADCPPUTHH3 (ADCPPU3 Trip-Zone High-Side Threshold Register) Offset: 0x27C Default: 0x00000000 Access: ADC -> ADCPPUTHH3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-331: ADCPPU3 Trip-Zone High-Side Threshold Register (ADCPPUTHH3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.161 ADCPPU4 Trip-Zone High-Side Threshold Register (ADCPPUTHH4)

Table 12-332: ADCPPU4 Trip-Zone High-Side Threshold Register (ADCPPUTHH4) Layout

ADCPPUTHH4 (ADCPPU4 Trip-Zone High-Side Threshold Register) Offset: 0x280 Default: 0x00000000 Access: ADC -> ADCPPUTHH4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-333: ADCPPU4 Trip-Zone High-Side Threshold Register (ADCPPUTHH4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.162 ADCPPU5 Trip-Zone High-Side Threshold Register (ADCPPUTHH5)

Table 12-334: ADCPPU5 Trip-Zone High-Side Threshold Register (ADCPPUTHH5) Layout

ADCPPUTHH5 (ADCPPU5 Trip-Zone High-Side Threshold Register) Offset: 0x284 Default: 0x00000000 Access: ADC -> ADCPPUTHH5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-335: ADCPPU5 Trip-Zone High-Side Threshold Register (ADCPPUTHH5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.163 ADCPPU6 Trip-Zone High-Side Threshold Register (ADCPPUTHH6)

Table 12-336: ADCPPU6 Trip-Zone High-Side Threshold Register (ADCPPUTHH6) Layout

ADCPPUTHH6 (ADCPPU6 Trip-Zone High-Side Threshold Register) Offset: 0x288 Default: 0x00000000 Access: ADC -> ADCPPUTHH6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-337: ADCPPU6 Trip-Zone High-Side Threshold Register (ADCPPUTHH6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.164 ADCPPU7 Trip-Zone High-Side Threshold Register (ADCPPUTHH7)

Table 12-338: ADCPPU7 Trip-Zone High-Side Threshold Register (ADCPPUTHH7) Layout

ADCPPUTHH7 (ADCPPU7 Trip-Zone High-Side Threshold Register) Offset: 0x28C Default: 0x00000000 Access: ADC -> ADCPPUTHH7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-339: ADCPPU7 Trip-Zone High-Side Threshold Register (ADCPPUTHH7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.165 ADCPPU0 Trip-Zone Low-Side Threshold Register (ADCPPUTHL0)

Table 12-340: ADCPPU0 Trip-Zone Low-Side Threshold Register (ADCPPUTHL0) Layout

ADCPPUTHL0 (ADCPPU0 Trip-Zone Low-Side Threshold Register) Offset: 0x290 Default: 0x00000000 Access: ADC -> ADCPPUTHL0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-341: ADCPPU0 Trip-Zone Low-Side Threshold Register (ADCPPUTHL0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.166 ADCPPU1 Trip-Zone Low-Side Threshold Register (ADCPPUTHL1)

Table 12-342: ADCPPU1 Trip-Zone Low-Side Threshold Register (ADCPPUTHL1) Layout

ADCPPUTHL1 (ADCPPU1 Trip-Zone Low-Side Threshold Register) Offset: 0x294 Default: 0x00000000 Access: ADC -> ADCPPUTHL1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-343: ADCPPU1 Trip-Zone Low-Side Threshold Register (ADCPPUTHL1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.167 ADCPPU2 Trip-Zone Low-Side Threshold Register (ADCPPUTHL2)

Table 12-344: ADCPPU2 Trip-Zone Low-Side Threshold Register (ADCPPUTHL2) Layout

ADCPPUTHL2 (ADCPPU2 Trip-Zone Low-Side Threshold Register) Offset: 0x298 Default: 0x00000000 Access: ADC -> ADCPPUTHL2.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-345: ADCPPU2 Trip-Zone Low-Side Threshold Register (ADCPPUTHL2) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.168 ADCPPU3 Trip-Zone Low-Side Threshold Register (ADCPPUTHL3)

Table 12-346: ADCPPU3 Trip-Zone Low-Side Threshold Register (ADCPPUTHL3) Layout

ADCPPUTHL3 (ADCPPU3 Trip-Zone Low-Side Threshold Register) Offset: 0x29C Default: 0x00000000 Access: ADC -> ADCPPUTHL3.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-347: ADCPPU3 Trip-Zone Low-Side Threshold Register (ADCPPUTHL3) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.169 ADCPPU4 Trip-Zone Low-Side Threshold Register (ADCPPUTHL4)

Table 12-348: ADCPPU4 Trip-Zone Low-Side Threshold Register (ADCPPUTHL4) Layout

ADCPPUTHL4 (ADCPPU4 Trip-Zone Low-Side Threshold Register) Offset: 0x2A0 Default: 0x00000000 Access: ADC -> ADCPPUTHL4.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-349: ADCPPU4 Trip-Zone Low-Side Threshold Register (ADCPPUTHL4) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.170 ADCPPU5 Trip-Zone Low-Side Threshold Register (ADCPPUTHL5)

Table 12-350: ADCPPU5 Trip-Zone Low-Side Threshold Register (ADCPPUTHL5) Layout

ADCPPUTHL5 (ADCPPU5 Trip-Zone Low-Side Threshold Register) Offset: 0x2A4 Default: 0x00000000 Access: ADC -> ADCPPUTHL5.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-351: ADCPPU5 Trip-Zone Low-Side Threshold Register (ADCPPUTHL5) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.171 ADCPPU6 Trip-Zone Low-Side Threshold Register (ADCPPUTHL6)

Table 12-352: ADCPPU6 Trip-Zone Low-Side Threshold Register (ADCPPUTHL6) Layout

ADCPPUTHL6 (ADCPPU6 Trip-Zone Low-Side Threshold Register) Offset: 0x2A8 Default: 0x00000000 Access: ADC -> ADCPPUTHL6.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-353: ADCPPU6 Trip-Zone Low-Side Threshold Register (ADCPPUTHL6) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

12.13.2.172 ADCPPU7 Trip-Zone Low-Side Threshold Register (ADCPPUTHL7)

Table 12-354: ADCPPU7 Trip-Zone Low-Side Threshold Register (ADCPPUTHL7) Layout

ADCPPUTHL7 (ADCPPU7 Trip-Zone Low-Side Threshold Register) Offset: 0x2AC Default: 0x00000000 Access: ADC -> ADCPPUTHL7.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 12-355: ADCPPU7 Trip-Zone Low-Side Threshold Register (ADCPPUTHL7) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Signed trip-zone threshold within [-16384, 16383]

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12.13.2.173 Temperature Sensor Control Register (TSENSCTL)

Table 12-356: Temperature Sensor Control Register (TSENSCTL) Layout

TSENSCTL (Temperature Sensor Control Register) Offset: 0x2B0 Default: 0x00000000 Access: ADC -> TSENSCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	DEMSEL				SWAPBJT	OUTINV	EN

Table 12-357: Temperature Sensor Control Register (TSENSCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6:3	DEMSEL	RW	0x0	Current branch select for dynamic element match
2	SWAPBJT	RW	0x0	Swap BJT 0: Not swap BJT 1: Swap BJT
1	OUTINV	RW	0x0	Invert T-Sensor output 0 and output 1 0: Normal connect 1: Invert T-Sensor output 0 and output 1
0	EN	RW	0x0	Temperature sensor enable 0: Disable 1: Enable

12.13.2.174 ADC Register Write-Allow Key Register (ADCREGKEY)

Table 12-358: ADC Register Write-Allow Key Register (ADCREGKEY) Layout

ADCREGKEY (ADC Register Write-Allow Key Register) Offset: 0x2B4 Default: 0x1ACCE551 Access: ADC -> ADCREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 12-359: ADC Register Write-Allow Key Register (ADCREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected ADC registers

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13 PGA

13.1 PGA overview

The SPC2168 implements six Programmable-Gain Amplifiers (PGA), which supports 6-channel amplifying simultaneously. Each PGA supports two mode: one is differential mode with gain up to 64, the other is single ended mode with gain up to 32. In single ended mode, one PGA can act like two single-ended PGA.

13.2 PGA architecture

The six PGAs are numbered 0 to 5. As shown in Figure 13-1 and Figure 13-2, there is an 8:1 MUX (called PGA MUX) on each positive and negative input of PGA. Each PGA can be powered down and bypassed.

Figure 13-1: Block architecture for PGA0 ~ PGA2

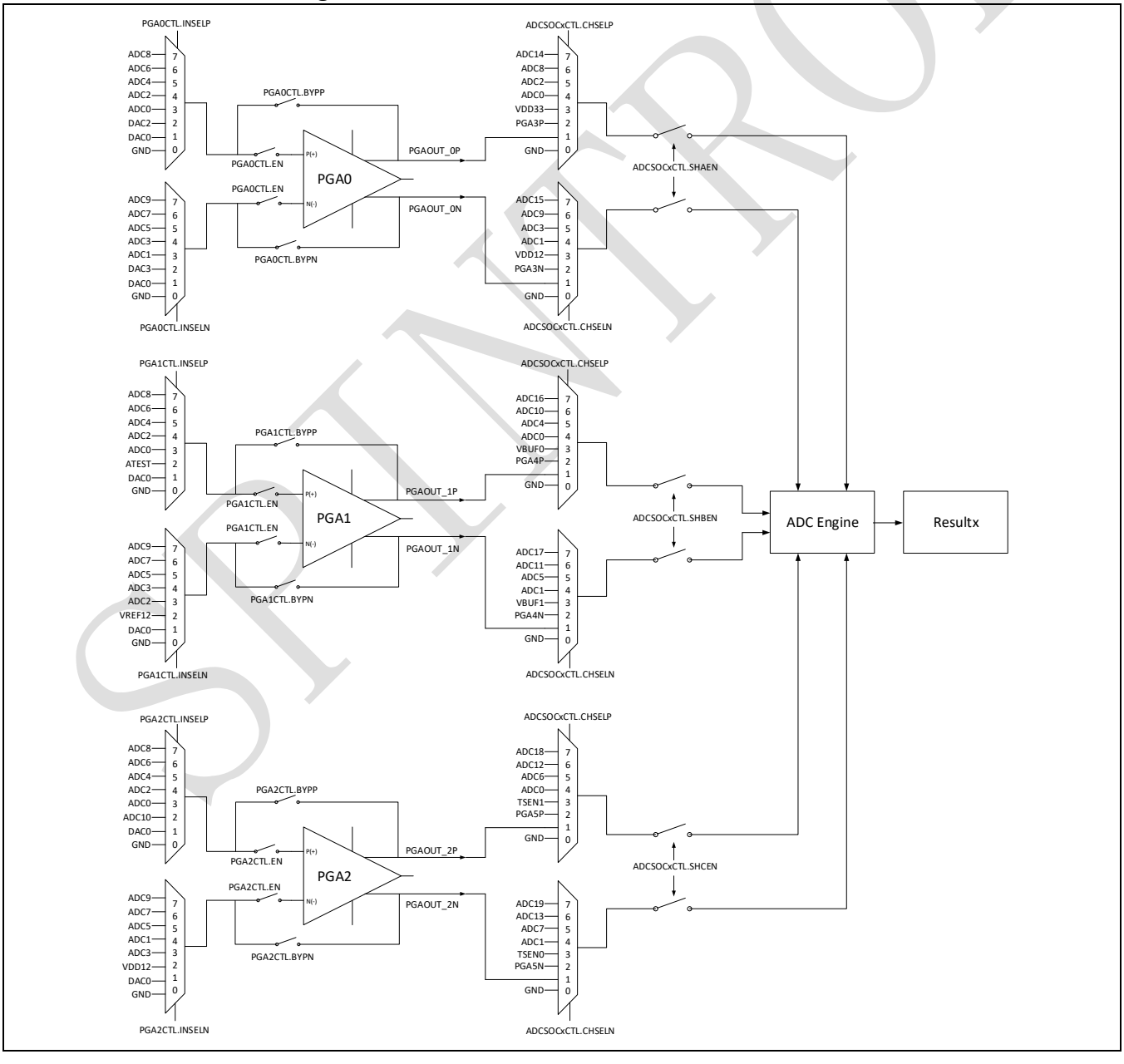

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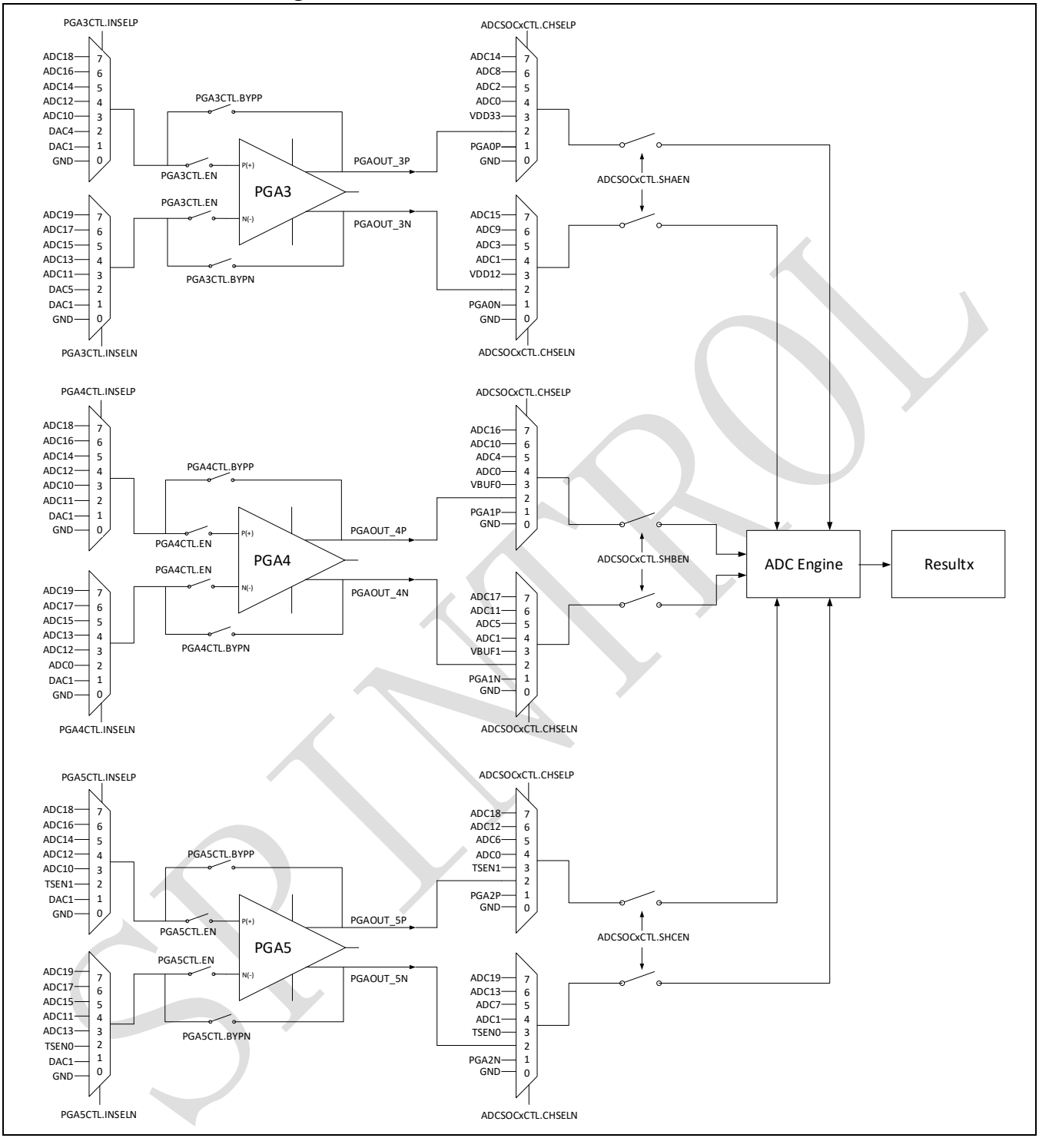
Figure 13-2: Block architecture for PGA3 ~ PGA5



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13.3 PGA channel selection

For each PGA, there are 3 different options groups to control 8 to 1 channel MUX. In one group, the selection contain positive and negative (PGAxCTL.INSELP/N, x = 0, 1, 2, 3, 4, 5 for PGA0/1/2/3/4/5). The channel selection table is shown as below.

Table 13-1: MUX selection for PGA0/1/2

PGAxCTL.INSELP & PGAxCTL.INSELN	in_p to PGA0	in_n to PGA0	in_p to PGA1	in_n to PGA1	in_p to PGA2	in_n to PGA2
7	ADC8	ADC9	ADC8	ADC9	ADC8	ADC9
6	ADC6	ADC7	ADC6	ADC7	ADC6	ADC7
5	ADC4	ADC5	ADC4	ADC5	ADC4	ADC5
4	ADC2	ADC3	ADC2	ADC3	ADC2	ADC1
3	ADC0	ADC1	ADC0	ADC2	ADC0	ADC3
2	DAC2	DAC3	ATEST	VREF12	ADC10	VDD12
1	DAC0	DAC0	DAC0	DAC0	DAC0	DAC0
0	GND	GND	GND	GND	GND	GND

Table 13-2: MUX selection for PGA3/4/5

PGAxCTL.INSELP & PGAxCTL.INSELN	in_p to PGA3	in_n to PGA3	in_p to PGA4	in_n to PGA4	in_p to PGA5	in_n to PGA5
7	ADC18	ADC19	ADC18	ADC19	ADC18	ADC19
6	ADC16	ADC17	ADC16	ADC17	ADC16	ADC17
5	ADC14	ADC15	ADC14	ADC15	ADC14	ADC15
4	ADC12	ADC13	ADC12	ADC13	ADC12	ADC11
3	ADC10	ADC11	ADC10	ADC12	ADC10	ADC13
2	DAC4	DAC5	ADC11	ADC0	TSEN1	TSEN0
1	DAC1	DAC1	DAC1	DAC1	DAC1	DAC1
0	GND	GND	GND	GND	GND	GND

Example 13.3.1 Examples of PGA MUX usage

- Connect temperature sensor differential output to PGA5
- Connect input ADC10 voltage (referred to ground) into PGA3
- Connect difference between ADC8 and DAC0 into PGA0

Example 13.3.1

```
void PGA_Example13_3_1(void)
{
   PGA->PGA5CTL.bit.INSELP=2;/* Select TSENS1 to PGA5_INP    */
   PGA->PGA5CTL.bit.INSELN=2;/* Select TSENS0 to PGA5_INN    */
   PGA->PGA3CTL.bit.INSELP=3;/* Select ADC10 to PGA3_INP     */
   PGA->PGA3CTL.bit.INSELN=0;/* Select GND to PGA3_INN        */
   PGA->PGA0CTL.bit.INSELP=7;/* Select ADC8 to PGA0_INP      */
   PGA->PGA0CTL.bit.INSELN=1;/* Select DAC0 to PGA0_INN       */
}
```

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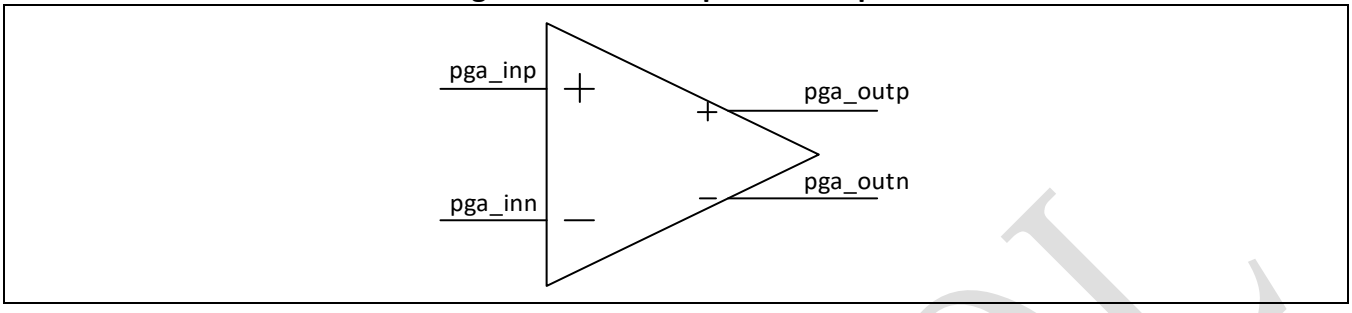
13.4 PGA mode and gain

Each PGA can be configured to work in single-ended mode or differential-mode.

Figure 13-3: PGA input and output



In single-ended mode, for each PGA, either inp or inn can be selected as input. The corresponding output is outp or outn. And inp and inn can be simultaneously used in single-ended mode for same PGA. It depends on PGAxCTL.MODE settings shown as below:

Table 13-3: PGA mode selection

PGAxCTL.MODE	Description
0	Differential mode
1	Single-ended mode with positive path only
2	Single-ended mode with negative path only
3	Single-ended mode with both negative path and positive path

The gain selection for single-ended mode and differential mode is shown as below:

Table 13-4: PGA gain selection

PGAxCTL.GAINP & PGAxCTL.GAINN	Single-ended mode gain	Differential mode gain
0	1	2
1	2	4
2	4	8
3	8	16
4	12	24
5	16	32
6	24	48
7	32	64

For single-ended mode, positive path gain is set by GAINP, and negative path gain is set by GAINN, shown as the following equations:

$$\mathrm{OUTP} = \mathrm{GAINP} \times \mathrm{INP}$$
$$\mathrm{OUTN} = \mathrm{GAINN} \times \mathrm{INN}$$

For each PGA, both inp and inn are rail to rail input range. Output range in each-end is 0.3V ~ AVDD-0.3V, to avoid saturation in PGA, different gain is corresponding to different input range. Assume AVDD is 3.3V, input range in different gain for single-ended mode is shown as below:

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Table 13-5: PGA input range in different gain for single-ended mode

PGAxCTL.GAINP(N)	Gain	Input range (V)	Output range (V)
0	1	0.3~3	0.3~3
1	2	0.15~1.5	0.3~3
2	4	0.075~0.75	0.3~3
3	8	0.0375~0.375	0.3~3
4	12	0.025~0.25	0.3~3
5	16	0.01875~0.1875	0.3~3
6	24	0.0125~0.125	0.3~3
7	32	0.009375~0.09375	0.3~3

The GAINP and GAINN need to be set as the same value for differential mode. For example, GAINP = GAINN = GAIN, then the differential output is shown as below:

$$\mathrm{OUTP} - \mathrm{OUTN} = \mathrm{GAIN} \times (INP - INN)$$

Common mode voltage of output can be set by either inp or inn, depends on the PGAxCTL.CMSEL setting. By default, PGAxCTL.CMSEL = 1, and inp is set as output common voltage. If PGAxCTL.CMSEL = 0, inn is set as output common mode voltage. For example, if PGAxCTL.CMSEL = 0,

$$\mathrm{OUT_CM} = \mathrm{INN}$$

$$\mathrm{OUTP} = \mathrm{INN} + (INP - INN) \times \frac{Gain}{2}$$

$$\mathrm{OUTN} = \mathrm{INN} - (INP - INN) \times \frac{Gain}{2}$$

If PGAxCTL.CMSEL = 1,

$$\mathrm{OUT_CM} = \mathrm{INP}$$

$$\mathrm{OUTP} = \mathrm{INP} + (INP - INN) \times \frac{Gain}{2}$$

$$\mathrm{OUTN} = \mathrm{INP} - (INP - INN) \times \frac{Gain}{2}$$

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Example 13.4.1 PGA in single-ended mode with positive path and set gain

Only use PGA2 positive path, inp = 0.5V, and expected outp = 1V

- Set PGA2 positive path in single-ended mode
- Set single mode gain = 2

Example 13.4.1

```
void PGA_Example13_4_1(void)
{
  PGA->PGA2CTL.bit.MODE=1;/* Set single mode with positive path only      */
  PGA->PGA2CTL.bit.GAINP=1;/* Set single mode gain =2 */
}
```

Example 13.4.2 PGA in single-ended mode with positive and negative path and set gain

Use PGA1 both positive and negative path in single-ended mode, if inp range is 0.3V to 0.5V, and inn range is 0.06V to 0.14V, set positive path gain to 4, so outp range is from 1.2V to 2V; and set negative path gain to 16, so outn range is from 0.96V to 2.24V.

- Set PGA1 positive path and negative path in single mode
- Set PGA1 positive path gain is 4
- Set PGA1 negative path gain is 16

Example 13.4.2

```
void PGA_Example13_4_2(void)
{
PGA->PGA1CTL.bit.MODE=3;/* Set single mode with positive path and negative path    */
PGA->PGA1CTL.bit.GAINP=2;/* Set single mode positive path gain = 4 */
PGA->PGA1CTL.bit.GAINN=5;/* Set single mode negative path gain = 16 */
}
```

Example 13.4.3 PGA in differential mode and gain set

If AVDD=3.3V, gain=4X, inp=2.05V, inn=1.65V, use inn as output common voltage:

outp = 1.65 + (2.05-1.65) * 4/2 = 2.45V
outn = 1.65 – (2.05-1.65) * 4/2 = 0.85V

- Set PGA1 in differential mode
- Set INN as output common mode voltage
- Set gain = 4

Example 13.4.3

```
void PGA_Example13_4_3(void)
{
PGA->PGA2CTL.bit.MODE=0;/* Set differential mode      */
PGA->PGA2CTL.bit.CMSEL=1;/* Use INN as output common mode voltage    */
PGA->PGA2CTL.bit.GAINP=1;/* Set differential mode gain = 4 */
PGA->PGA2CTL.bit.GAINN=1;/* Set differential mode gain = 4 */
}
```


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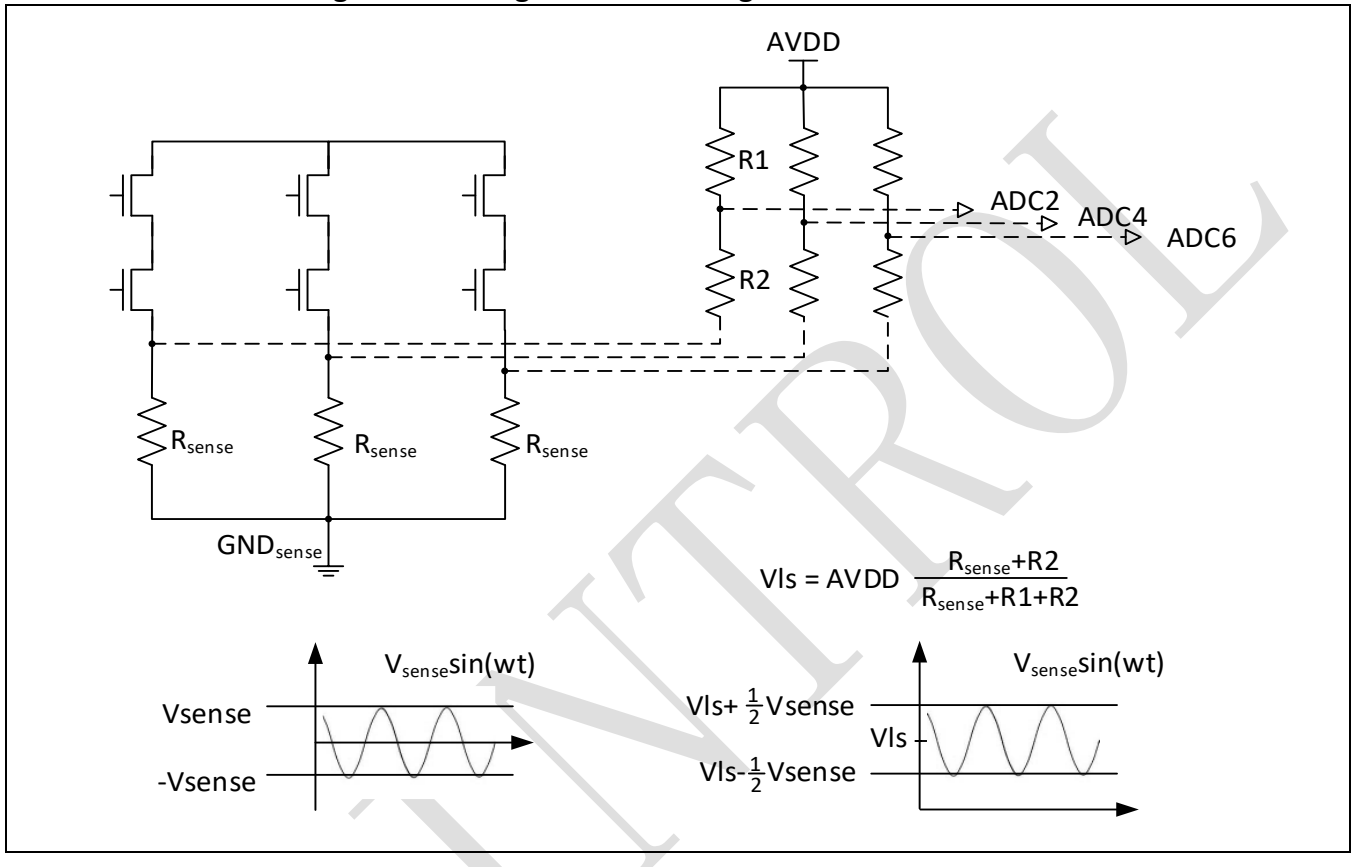
13.5 PGA single-ended application in current sensing

For driver FET current sensing, as Figure 13-4 shows, assume use ADC2, ADC4, ADC6 to sample. PGA configuration is described in Table 13-1. It is important to level-shift V_{sense} signal just enough to guarantee V_{sense} does not go below ground, so that the level-shifted signal could be brought up on-chip to PGA.

Figure 13-4: Single-ended sensing of driver FET currents



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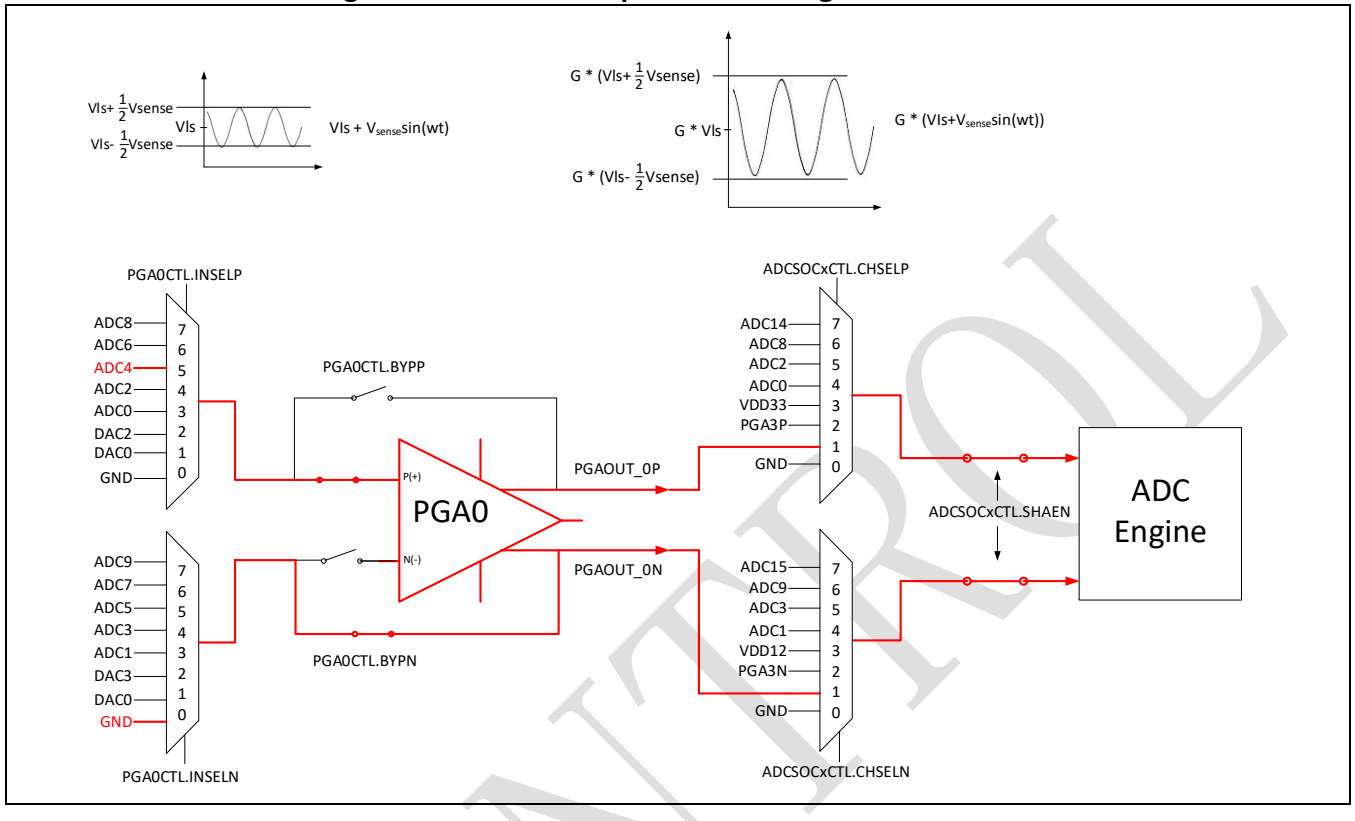
As Figure 13-5 shows, PGA0 amplifies ADC4 and its outputs are brought to ADC for conversion via ADC MUX. Input signal Vls+Vsense*sin(wt) is multiplied by G.

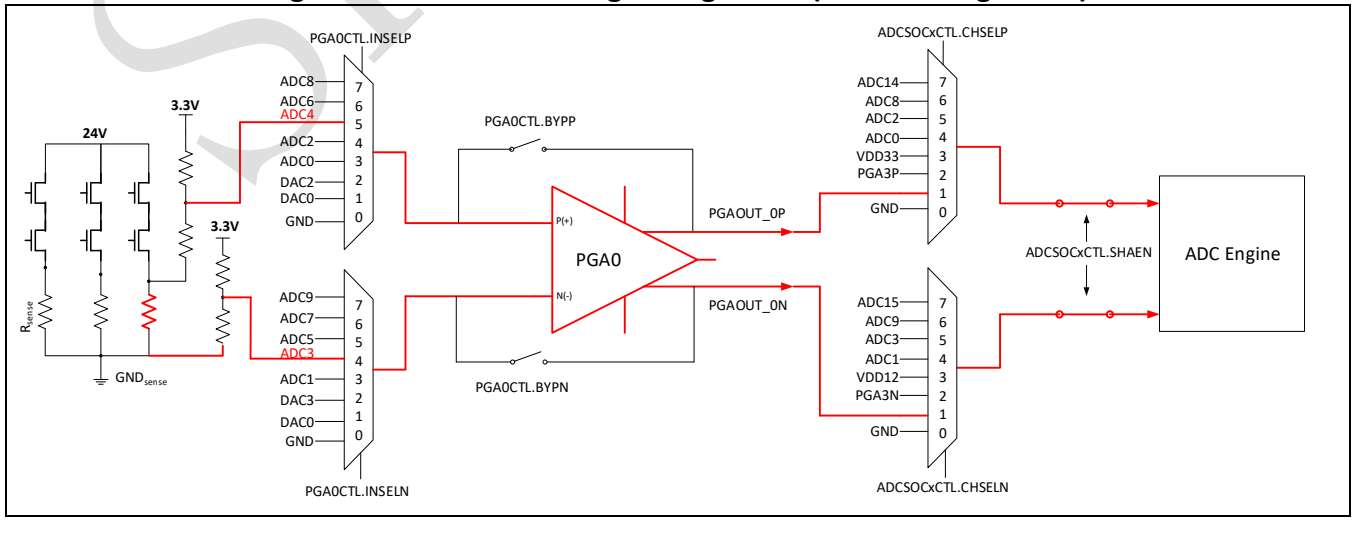
Figure 13-5: PGA0 sample ADC4 in single-ended mode



13.6 PGA differential application in current sensing

Motor control is achieved usually by sensing current through a driver FET as depicted in Figure 13-6. The current is usually measured by measuring voltage in the sense resistor. The resulting voltage is a sinusoid with average 0V. The negative voltage on the sensing resistor Rsense cannot be fed into the chip and is level-shifted up by using resistor divider consisting of two resistors R. The most optimal design has the two resistors equal and top resistor connected to the voltage level equal to high-voltage power of the chip AVDD, as will be seen from further discussion.

Figure 13-6: Motor sensing arrangement (differential gain = 8)



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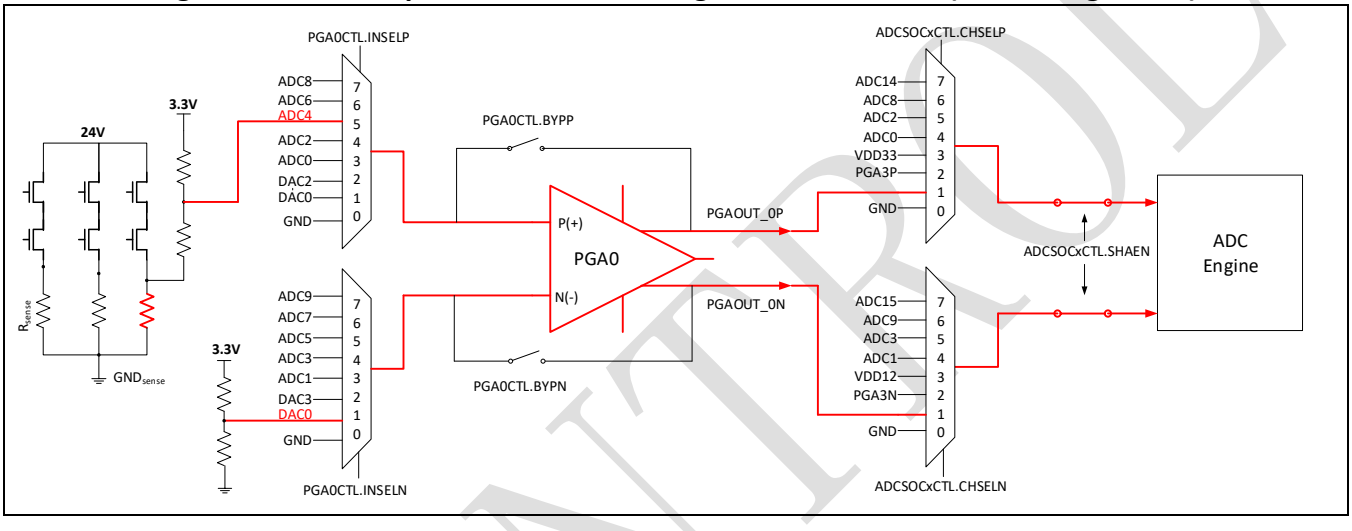
The level-shifted signal has average of AVDD/2 and amplitude equal to half of the amplitude of voltage on the sense resistor. In addition to the level-shifted motor current signals, a level-shifted sensing ground is also set up for conversion.

Arrange PGA0 in differential mode with top branch receiving level-shifted sensed signal ADC4, and bottom branch receiving ADC3 (level-shifted ground, optimally AVDD/2). The output common mode of PGA0 is equal to the input of the bottom branch, i.e. equal to AVDD/2. This creates the optimal range for PGA0 output signal differential swing, because it places common mode voltage directly in the middle of 0 to AVDD output range of PGA0. The PGA0 output differential signal is equal to the input differential signal multiplied by gain, as shown in Figure 13-6.

Figure 13-7: Three-pin differential sensing of three currents (diffential gain = 8)

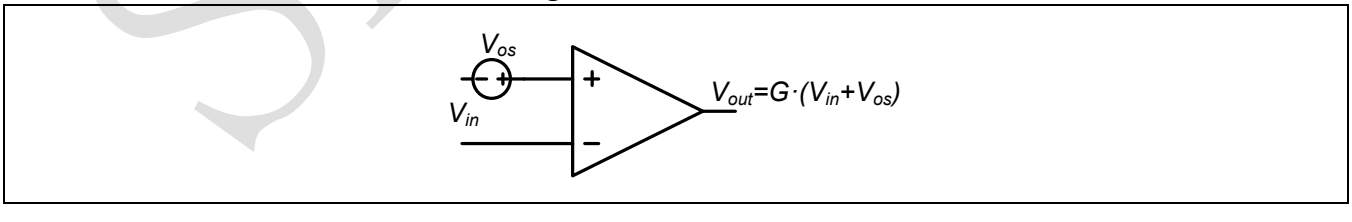


Instead of using outside resistor divider to generate AVDD/2, we can choose an internal 10-bit DAC as common mode, as shown in Figure 13-7. The advantage of this method is to save a pin of feeding level-shifting ground.

13.7 PGA offset calibration

Due to natural mismatch of transistors on the chip, every amplifier has a natural input-referred offset which distorts output. This concept is shown in Figure 13-8. Here PGA output is equal to gain multiplying input plus an extra voltage Vos, called input-referred offset or simply offset of PGA.

Figure 13-8: PGA offset



In order to calibrate for offset, the offset must be independent of input, i.e. Vos cannot depend on Vin, both its differential and common mode component. The offset dynamics of SPC2168 amplifiers is shown in Figure 13-9. For input common mode voltage less than 2.1V, the offset has one value, for the input common mode range high enough (larger than 2.4V), the offset has another value, and a transition region between 2.1 and 2.4V. Note that for AVDD>3V, the input is centered on 1.5V or more, as long as input common mode voltage is less than 2.1V, the constant-Vos scenario holds and offset can be calibrated.

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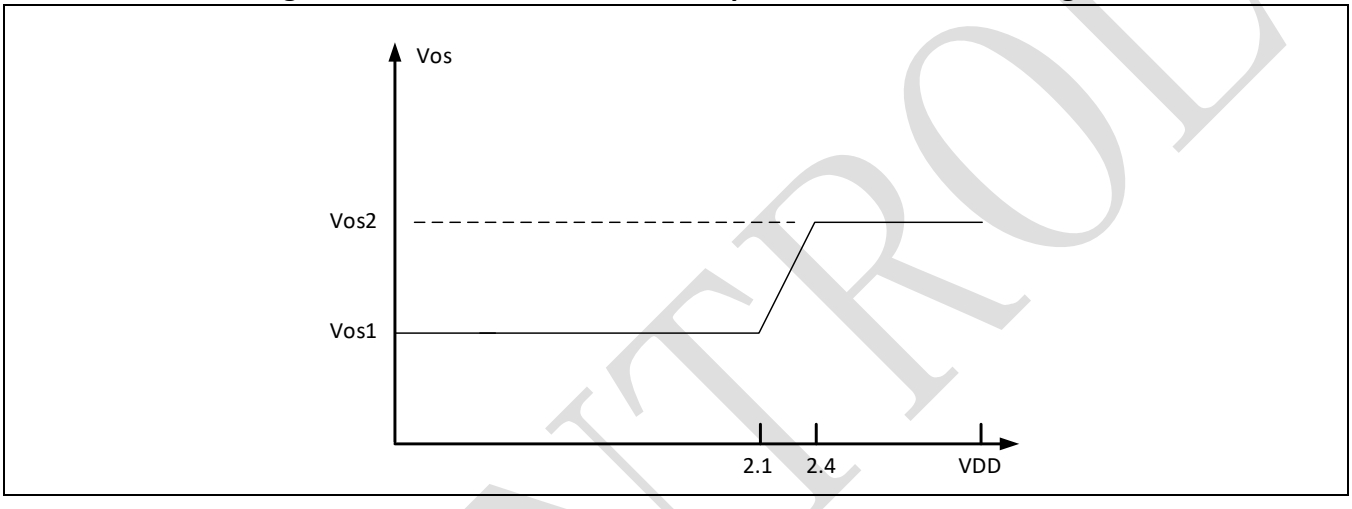
If the offset is determined, the software can account for it, by subtracting from measured signal offset multiplied by gain, to get ideally-amplified signal information. Therefore, calibrating for offset is an integral part of accurate signal amplification and measurement.

In order to calibrate for offset, equal signal must apply to both inputs of PGA (Vin=0 in Figure 13-9). Then the measured output, divided by gain, is the desired offset value Vos. It is recommended to apply equal 10bit DAC value to PGAn (use DAC1 see Table 13-1 and related discussion), with DAC1 output being equal to value less than 2.1V. The PGA will output Vos1 times gain. Since Vos1 is small to begin with (<2mV), within largest gain of 64 the PGA differential output is less than 200mV and the PGA output will not saturate.

Figure 13-9: Offset behavior with input common-mode voltage



It is not recommended to apply external level shifters on board because level shifters mismatch probably more than any on-chip elements. Moreover, since the same DAC1 voltage point is applied to both p and n inputs of PGA, even if internal DAC resistors have minor mismatch, differential input signal is exactly zero.

There are three different offsets for three different modes of PGA operation: PGA operating in differential mode, PGA operating with single-ended mode for p-branch (n-branch disabled and bypassed), PGA operating with single-ended mode for n-branch (p-branch disabled and bypassed) has different offset which should be independently determined and accounted for by post-ADC processing.

There are three different offsets for three different modes of PGA operation: PGA operating in differential mode, PGA operating with single-ended mode for p-branch (n-branch disabled and bypassed), PGA operating with single-ended mode for n-branch (p-branch disabled and bypassed). Each mode has different offset which should be independently determined and handled for post-ADC processing.

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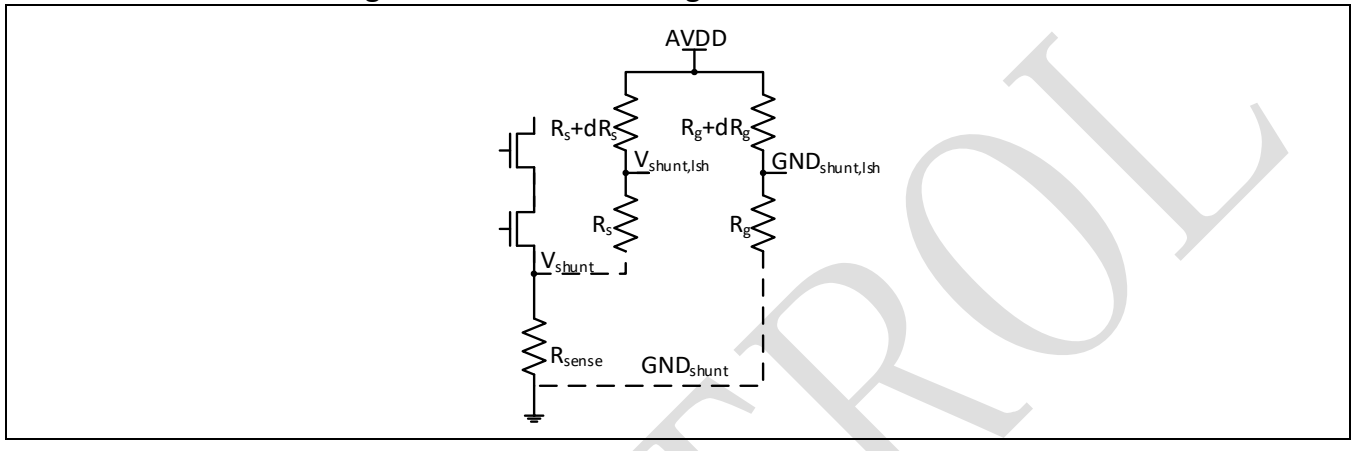
13.8 Resistive level shifter offset calibration

As can be seen from Figure 13-6, each on-board resistive level shifter consists of two resistors. For conventional differential mode operation, both resistors should be equal, in order to level shift signal to come out differentially centered on mid-rail AVDD/2 level. The two resistors usually mismatch and this mismatch also has to be calibrated, in order to correctly determine voltage across current-sensing shunt resistor.

Figure 13-10: Level-shifting with resistor mismatch



For simplicity, but without reducing discussion generality, assume the case of Figure 13-10. There the voltages are level-shifted to the mid-rail AVDD/2 level, and nominally each two level-shifting resistors are equal. Then we can write for the level-shifted outputs:

$$V_{shunt,lsh} = V_{ddx}\frac{R_s}{2\cdot R_s + \delta R_s} + V_{shunt}\frac{R_s + \delta R_s}{2\cdot R_s + \delta R_s} = \frac{V_{ddx}}{2}\left[1 - \frac{\delta_s}{2}\right] + \frac{V_{shunt}}{2}\left[1 + \frac{\delta_s}{2}\right]$$

$$GND_{shunt,lsh} = V_{ddx}\frac{R_g}{2\cdot R_g + \delta R_g} + GND_{shunt}\frac{R_g + \delta R_g}{2\cdot R_g + \delta R_g} = \frac{V_{ddx}}{2}\left[1 - \frac{\delta_g}{2}\right] + \frac{GND_{shunt}}{2}\left[1 + \frac{\delta_g}{2}\right]$$

Here Rs/Rs=δ_s and Rg/Rg=δ_g. The differential signal can be written:

$$V_{ind} = V_{shunt,lsh} - GND_{shunt,lsh} = \frac{V_{ddx}}{2}\cdot\frac{\delta_g - \delta_s}{2} + \frac{V_{shunt} - GND_{shunt}}{2} + \frac{V_{shunt}}{2}\cdot\frac{\delta_s}{2}$$

Here we neglect term $GND_{shunt}\delta_g/4$ because both GND_{shunt} and δ_g are small. We see that mismatch is separated in gain error (V_{shunt}-multiplying term δ_s /2) and offset (V_{ind} at V_{shunt}=0 term). Gain error term is equivalent to effective difference in R_{sense} resistor, because $V_{shunt}=I_{FET}xR_{sense}$. Both terms can be determined from measuring signal when the motor is not operating, i.e. when V_{shunt}=0. The following procedure can be observed:

- Measure AVDD. It can be routed to ADC via ADC MUX, as can be seen from Table 13-1.
- With zero current, when Vshunt=0, measure Vshunt,lsh and determine δs (remember, AVDD is known already) using the first equation of this chapter.

Finally, with zero current, measure V_{ind} and determine $\delta_g - \delta_s$ term, thereby deriving δ_g using the third equation of this chapter.

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13.9 Power-up sequence

When powering up the PGA, the following sequence must be used:

Step 1: Power up ADC bandgap

Step 2: Power up the analog circuits of PGA

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13.10 Registers

13.10.1 PGA register map

Table 13-6: PGA Module Base Address

Peripheral Module	Base Address
PGA	0x4000 8C00

Table 13-7: PGA Register Map

Register	Offset	Description	Reset Value
PGA0CTL*	0x2C0	PGA0 Control Register	0x00000008
PGA1CTL*	0x2C4	PGA1 Control Register	0x00000008
PGA2CTL*	0x2C8	PGA2 Control Register	0x00000008
PGA3CTL*	0x2CC	PGA3 Control Register	0x00000008
PGA4CTL*	0x2D0	PGA4 Control Register	0x00000008
PGA5CTL*	0x2D4	PGA5 Control Register	0x00000008
PGAREGKEY	0x2E0	PGA Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the PGAREGKEY=0x1ACCE551.

SPINTROL

13.10.2 PGA registers

13.10.2.1 PGA0 Control Register (PGA0CTL)

Table 13-8: PGA0 Control Register (PGA0CTL) Layout

PGA0CTL (PGA0 Control Register) Offset: 0x2C0 Default: 0x00000008 Access: PGA -> PGA0CTL.all							
31	30	29	28	27	26	25	24
RESERVED_31_18							
23	22	21	20	19	18	17	16
RESERVED_31_18						BYPN	BYPP
15	14	13	12	11	10	9	8
GAINN			GAINP			INSELN	
7	6	5	4	3	2	1	0
INSELN	INSELP			CMSEL	MODE		EN

Table 13-9: PGA0 Control Register (PGA0CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	BYPN	RW	0x0	PGA0 negative path bypass 0: Not bypass 1: Bypass
16	BYPP	RW	0x0	PGA0 positive path bypass 0: Not bypass 1: Bypass
15:13	GAINN	RW	0x0	PGA0 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode 010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
12:10	GAINP	RW	0x0	PGA0 negative path gain 000: 1x for single-ended mode 2x for differential mode

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Bits	Field Name	Type	Reset	Description
				001: 2x for single-ended mode 4x for differential mode 010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
9:7	INSELN	RW	0x0	PGA0 negative input select 000: Analog ground 001: DAC0 for common input 010: DAC3 output 011: ADC1 input from GPIO1 100: ADC3 input from GPIO3 101: ADC5 input from GPIO5 110: ADC7 input from GPIO7 111: ADC9 input from GPIO9
6:4	INSELP	RW	0x0	PGA0 positive input select 000: Analog ground 001: DAC0 for common input 010: DAC2 output 011: ADC0 input from GPIO0 100: ADC2 input from GPIO2 101: ADC4 input from GPIO4 110: ADC6 input from GPIO6 111: ADC8 input from GPIO8
3	CMSEL	RW	0x1	PGA0 output common voltage select This bit is active only in differential mode 0: Select negative input as output common voltage 1: Select positive input as output common voltage
2:1	MODE	RW	0x0	PGA0 mode 00: Differential mode 01: Single-ended mode with positive path only 10: Single-ended mode with negative path only 11: Single-ended mode with both paths
0	EN	RW	0x0	PGA0 enable 0: Disable PGA0 1: Enable PGA0

SPINTROL

13.10.2.2 PGA1 Control Register (PGA1CTL)

Table 13-10: PGA1 Control Register (PGA1CTL) Layout

PGA1CTL (PGA1 Control Register) Offset: 0x2C4 Default: 0x00000008 Access: PGA -> PGA1CTL.all							
31	30	29	28	27	26	25	24
RESERVED_31_18							
23	22	21	20	19	18	17	16
RESERVED_31_18						BYPN	BYPP
15	14	13	12	11	10	9	8
GAINN			GAINP			INSELN	
7	6	5	4	3	2	1	0
INSELN	INSELP			CMSEL	MODE		EN

Table 13-11: PGA1 Control Register (PGA1CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	BYPN	RW	0x0	PGA1 negative path bypass 0: Not bypass 1: Bypass
16	BYPP	RW	0x0	PGA1 positive path bypass 0: Not bypass 1: Bypass
15:13	GAINN	RW	0x0	PGA1 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode 010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
12:10	GAINP	RW	0x0	PGA1 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode

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Bits	Field Name	Type	Reset	Description
				010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
9:7	INSELN	RW	0x0	PGA1 negative input select 000: Analog ground 001: DAC0 for common input 010: 1.2V reference from ADC 011: ADC2 input from GPIO2 100: ADC3 input from GPIO3 101: ADC5 input from GPIO5 110: ADC7 input from GPIO7 111: ADC9 input from GPIO9
6:4	INSELP	RW	0x0	PGA1 positive input select 000: Analog ground 001: DAC0 for common input 010: ATEST output voltage 011: ADC0 input from GPIO0 100: ADC2 input from GPIO2 101: ADC4 input from GPIO4 110: ADC6 input from GPIO6 111: ADC8 input from GPIO8
3	CMSEL	RW	0x1	PGA1 output common voltage select This bit is active only in differential mode 0: Select negative input as output common voltage 1: Select positive input as output common voltage
2:1	MODE	RW	0x0	PGA1 mode 00: Differential mode 01: Single-ended mode with positive path only 10: Single-ended mode with negative path only 11: Single-ended mode with both paths
0	EN	RW	0x0	PGA1 enable 0: Disable PGA1 1: Enable PGA1

SPINTROL

13.10.2.3 PGA2 Control Register (PGA2CTL)

Table 13-12: PGA2 Control Register (PGA2CTL) Layout

PGA2CTL (PGA2 Control Register) Offset: 0x2C8 Default: 0x00000008
Access: PGA -> PGA2CTL.all

31	30	29	28	27	26	25	24
RESERVED_31_18							
23	22	21	20	19	18	17	16
RESERVED_31_18						BYPN	BYPP
15	14	13	12	11	10	9	8
GAINN			GAINP			INSELN	
7	6	5	4	3	2	1	0
INSELN	INSELP			CMSEL	MODE		EN

Table 13-13: PGA2 Control Register (PGA2CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	BYPN	RW	0x0	PGA2 negative path bypass 0: Not bypass 1: Bypass
16	BYPP	RW	0x0	PGA2 positive path bypass 0: Not bypass 1: Bypass
15:13	GAINN	RW	0x0	PGA2 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode 010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
12:10	GAINP	RW	0x0	PGA2 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode

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Bits	Field Name	Type	Reset	Description
				010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
9:7	INSELN	RW	0x0	PGA2 negative input select 000: Analog ground 001: DAC0 for common input 010: Digital 1.2V power 011: ADC3 input from GPIO3 100: ADC1 input from GPIO1 101: ADC5 input from GPIO5 110: ADC7 input from GPIO7 111: ADC9 input from GPIO9
6:4	INSELP	RW	0x0	PGA2 positive input select 000: Analog ground 001: DAC0 for common input 010: ADC10 input from GPIO10 011: ADC0 input from GPIO0 100: ADC2 input from GPIO2 101: ADC4 input from GPIO4 110: ADC6 input from GPIO6 111: ADC8 input from GPIO8
3	CMSEL	RW	0x1	PGA2 output common voltage select This bit is active only in differential mode 0: Select negative input as output common voltage 1: Select positive input as output common voltage
2:1	MODE	RW	0x0	PGA2 mode 00: Differential mode 01: Single-ended mode with positive path only 10: Single-ended mode with negative path only 11: Single-ended mode with both paths
0	EN	RW	0x0	PGA2 enable 0: Disable PGA2 1: Enable PGA2

SPINTROL

13.10.2.4 PGA3 Control Register (PGA3CTL)

Table 13-14: PGA3 Control Register (PGA3CTL) Layout

PGA3CTL (PGA3 Control Register) Offset: 0x2CC Default: 0x00000008
Access: PGA -> PGA3CTL.all

31	30	29	28	27	26	25	24
RESERVED_31_18							
23	22	21	20	19	18	17	16
RESERVED_31_18						BYPN	BYPP
15	14	13	12	11	10	9	8
GAINN			GAINP			INSELN	
7	6	5	4	3	2	1	0
INSELN	INSELP			CMSEL	MODE		EN

Table 13-15: PGA3 Control Register (PGA3CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	BYPN	RW	0x0	PGA3 negative path bypass 0: Not bypass 1: Bypass
16	BYPP	RW	0x0	PGA3 positive path bypass 0: Not bypass 1: Bypass
15:13	GAINN	RW	0x0	PGA3 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode 010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
12:10	GAINP	RW	0x0	PGA3 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode

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Bits	Field Name	Type	Reset	Description
				010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
9:7	INSELN	RW	0x0	PGA3 negative input select 000: Analog ground 001: DAC1 for common input 010: DAC5 output 011: ADC11 input from GPIO11 100: ADC13 input from GPIO13 101: ADC15 input from GPIO15 110: ADC17 input from GPIO17 111: ADC19 input from GPIO19
6:4	INSELP	RW	0x0	PGA3 positive input select 000: Analog ground 001: DAC1 for common input 010: DAC4 output 011: ADC10 input from GPIO10 100: ADC12 input from GPIO12 101: ADC14 input from GPIO14 110: ADC16 input from GPIO16 111: ADC18 input from GPIO18
3	CMSEL	RW	0x1	PGA3 output common voltage select This bit is active only in differential mode 0: Select negative input as output common voltage 1: Select positive input as output common voltage
2:1	MODE	RW	0x0	PGA3 mode 00: Differential mode 01: Single-ended mode with positive path only 10: Single-ended mode with negative path only 11: Single-ended mode with both paths
0	EN	RW	0x0	PGA3 enable 0: Disable PGA3 1: Enable PGA3

SPINTROL

13.10.2.5 PGA4 Control Register (PGA4CTL)

Table 13-16: PGA4 Control Register (PGA4CTL) Layout

PGA4CTL (PGA4 Control Register) Offset: 0x2D0 Default: 0x00000008 Access: PGA -> PGA4CTL.all							
31	30	29	28	27	26	25	24
RESERVED_31_18							
23	22	21	20	19	18	17	16
RESERVED_31_18						BYPN	BYPP
15	14	13	12	11	10	9	8
GAINN			GAINP			INSELN	
7	6	5	4	3	2	1	0
INSELN	INSELP			CMSEL	MODE		EN

Table 13-17: PGA4 Control Register (PGA4CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	BYPN	RW	0x0	PGA4 negative path bypass 0: Not bypass 1: Bypass
16	BYPP	RW	0x0	PGA4 positive path bypass 0: Not bypass 1: Bypass
15:13	GAINN	RW	0x0	PGA4 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode 010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
12:10	GAINP	RW	0x0	PGA4 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode

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Bits	Field Name	Type	Reset	Description
				010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
9:7	INSELN	RW	0x0	PGA4 negative input select 000: Analog ground 001: DAC1 for common input 010: ADC0 input from GPIO0 011: ADC12 input from GPIO12 100: ADC13 input from GPIO13 101: ADC15 input from GPIO15 110: ADC17 input from GPIO17 111: ADC19 input from GPIO19
6:4	INSELP	RW	0x0	PGA4 positive input select 000: Analog ground 001: DAC1 for common input 010: ADC11 input from GPIO11 011: ADC10 input from GPIO10 100: ADC12 input from GPIO12 101: ADC14 input from GPIO14 110: ADC16 input from GPIO16 111: ADC18 input from GPIO18
3	CMSEL	RW	0x1	PGA4 output common voltage select This bit is active only in differential mode 0: Select negative input as output common voltage 1: Select positive input as output common voltage
2:1	MODE	RW	0x0	PGA4 mode 00: Differential mode 01: Single-ended mode with positive path only 10: Single-ended mode with negative path only 11: Single-ended mode with both paths
0	EN	RW	0x0	PGA4 enable 0: Disable PGA4 1: Enable PGA4

SPINTROL

13.10.2.6 PGA5 Control Register (PGA5CTL)

Table 13-18: PGA5 Control Register (PGA5CTL) Layout

PGA5CTL (PGA5 Control Register) Offset: 0x2D4 Default: 0x00000008 Access: PGA -> PGA5CTL.all							
31	30	29	28	27	26	25	24
RESERVED_31_18							
23	22	21	20	19	18	17	16
RESERVED_31_18						BYPN	BYPP
15	14	13	12	11	10	9	8
GAINN			GAINP			INSELN	
7	6	5	4	3	2	1	0
INSELN	INSELP			CMSEL	MODE		EN

Table 13-19: PGA5 Control Register (PGA5CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:18	RESERVED_31_18	RO	0x0	Reserved
17	BYPN	RW	0x0	PGA5 negative path bypass 0: Not bypass 1: Bypass
16	BYPP	RW	0x0	PGA5 positive path bypass 0: Not bypass 1: Bypass
15:13	GAINN	RW	0x0	PGA5 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode 010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
12:10	GAINP	RW	0x0	PGA5 negative path gain 000: 1x for single-ended mode 2x for differential mode 001: 2x for single-ended mode 4x for differential mode

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Bits	Field Name	Type	Reset	Description
				010: 4x for single-ended mode 8x for differential mode 011: 8x for single-ended mode 16x for differential mode 100: 12x for single-ended mode 24x for differential mode 101: 16x for single-ended mode 32x for differential mode 110: 24x for single-ended mode 48x for differential mode 111: 32x for single-ended mode 64x for differential mode
9:7	INSELN	RW	0x0	PGA5 negative input select 000: Analog ground 001: DAC1 for common input 010: T-sensor output 0 011: ADC13 input from GPIO13 100: ADC11 input from GPIO11 101: ADC15 input from GPIO15 110: ADC17 input from GPIO17 111: ADC19 input from GPIO19
6:4	INSELP	RW	0x0	PGA5 positive input select 000: Analog ground 001: DAC1 for common input 010: T-sensor output 1 011: ADC10 input from GPIO10 100: ADC12 input from GPIO12 101: ADC14 input from GPIO14 110: ADC16 input from GPIO16 111: ADC18 input from GPIO18
3	CMSEL	RW	0x1	PGA5 output common voltage select This bit is active only in differential mode 0: Select negative input as output common voltage 1: Select positive input as output common voltage
2:1	MODE	RW	0x0	PGA5 mode 00: Differential mode 01: Single-ended mode with positive path only 10: Single-ended mode with negative path only 11: Single-ended mode with both paths
0	EN	RW	0x0	PGA5 enable 0: Disable PGA3 1: Enable PGA3

SPINTROL

13.10.2.7 PGA Register Write-Allow Key Register (PGAREGKEY)

Table 13-20: PGA Register Write-Allow Key Register (PGAREGKEY) Layout

PGAREGKEY (PGA Register Write-Allow Key Register) Offset: 0x2E0 Default: 0x1ACCE551 Access: PGA -> PGAREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 13-21: PGA Register Write-Allow Key Register (PGAREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected PGA registers

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14 Comparator

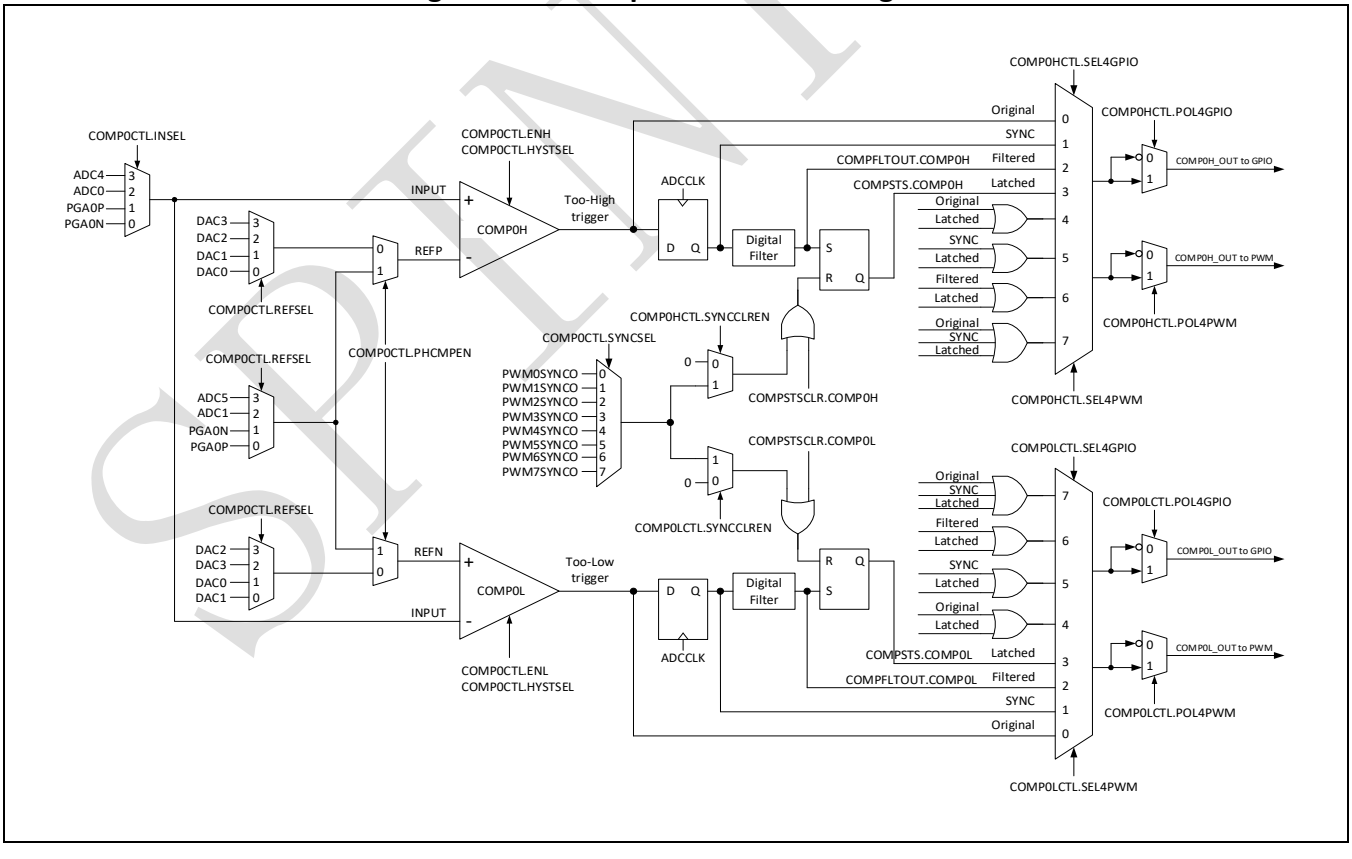
14.1 Comparator overview

For each PGA in SPC2168, there are 2 high speed rail-to-rail input comparators, check whether the voltage is too high or too low for over-current detection resulting in overall 12 comparators. There are two more pairs of comparators reserved for additional applications, such as two motor control support or PFC. Totally, SPC2168 has 16 comparators.

14.2 Comparator architecture

Figure 14-1 shows comparator0 block diagram, which includes two comparators, one is for monitoring voltage is too high, the other is to check voltage too low, and also includes input MUX to the comparators. SPC2168 has phase comparator feature, when COMP0CTL.PHCMPEN = 1, this feature is enabled, for example, if INSEL=1, REFSEL=1, PGA0P will be sent to positive input of the too high comparator and negative input of the too low comparator, PGA0N will be sent to negative input of the too high comparator and positive input of the too low comparator. When COMP0CTL.PHCMPEN = 0, the comparator references are from one of the four 10-bit DACs. Hysteresis can be enabled for each comparator with a typical value of 30 mV. The output of each comparator can be used as the PWM trip-zone event and has a typical delay of 50 ns.

Figure 14-1: Comparator 0 block diagram



SPINTROL

14.3 Comparator MUX selection

The input selections for 8 comparator pairs (comparator0~7) are shown in Table 14-1.

Table 14-1: Comparator MUX selection

Comparator0 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC4	1	3	ADC5	0	3	DAC3	DAC2
2	ADC0	1	2	ADC1	0	2	DAC2	DAC3
1	PGA0P	1	1	PGA0N	0	1	DAC1	DAC0
0	PGA0N	1	0	PGA0P	0	0	DAC0	DAC1
Comparator1 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC6	1	3	ADC7	0	3	DAC3	DAC2
2	ADC0	1	2	ADC2	0	2	DAC2	DAC3
1	PGA1P	1	1	PGA1N	0	1	DAC1	DAC0
0	PGA1N	1	0	PGA1P	0	0	DAC0	DAC1
Comparator2 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC8	1	3	ADC9	0	3	DAC3	DAC2
2	ADC0	1	2	ADC3	0	2	DAC2	DAC3
1	PGA2P	1	1	PGA2N	0	1	DAC1	DAC0
0	PGA2N	1	0	PGA2P	0	0	DAC0	DAC1
Comparator3 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC14	1	3	ADC15	0	3	DAC5	DAC4
2	ADC10	1	2	ADC11	0	2	DAC4	DAC5
1	PGA3P	1	1	PGA3N	0	1	DAC1	DAC0
0	PGA3N	1	0	PGA3P	0	0	DAC0	DAC1
Comparator4 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC16	1	3	ADC17	0	3	DAC5	DAC4
2	ADC10	1	2	ADC12	0	2	DAC4	DAC5
1	PGA4P	1	1	PGA4N	0	1	DAC1	DAC0
0	PGA4N	1	0	PGA4P	0	0	DAC0	DAC1
Comparator5 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC18	1	3	ADC19	0	3	DAC5	DAC4
2	ADC10	1	2	ADC13	0	2	DAC4	DAC5
1	PGA5P	1	1	PGA5N	0	1	DAC1	DAC0
0	PGA5N	1	0	PGA5P	0	0	DAC0	DAC1
Comparator6 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC16	1	3	ADC17	0	3	DAC3	DAC2
2	ADC12	1	2	ADC13	0	2	DAC2	DAC3
1	ADC6	1	1	ADC7	0	1	DAC1	DAC0

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0	ADC2	1	0	ADC3	0	0	DAC0	DAC1
Comparator7 MUX								
INSEL	**INPUT**	**PHCOMPEN**	**REFSEL**	**REFP/N**	**PHCOMPEN**	**REFSEL**	**REFP**	**REFN**
3	ADC18	1	3	ADC19	0	3	DAC5	DAC4
2	ADC14	1	2	ADC15	0	2	DAC4	DAC5
1	ADC8	1	1	ADC9	0	1	DAC1	DAC0
0	ADC4	1	0	ADC5	0	0	DAC0	DAC1

Example 14.3.1 Example of comparator MUX selection

- Set PGA2 positive output to comparator
- Set DAC1 output as too high threshold value
- Set DAC0 output as too low threshold value

Example 14.3.1

```
void COMP_Example14_3_1(void)
{
COMP->COMP2CTL.bit.INSEL=1;       /* Set PGA2P as input to comparator */
COMP->COMP2CTL.bit.PHCMPEN=0; /* disable phase comparator function */
COMP->COMP2CTL.bit.REFSEL=1;    /* Set DAC1 as REFP, and DAC0 as REFN */
COMP->COMP2CTL.bit.ENH=1;         /* Enable too high comparator */
COMP->COMP2CTL.bit.ENL=1;         /* Enable too low comparator */
}
```

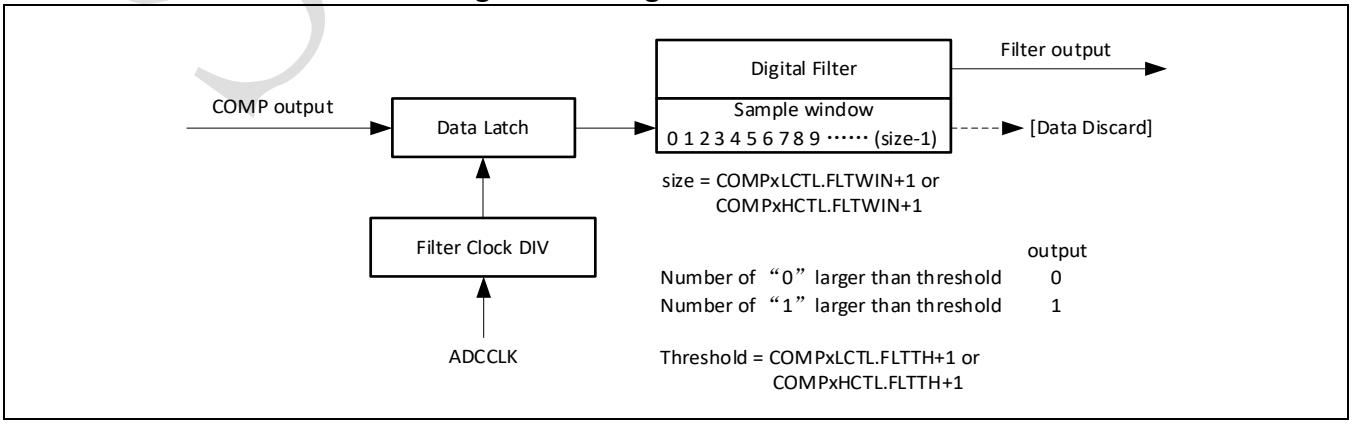
14.4 Digital filter

The comparator's output is sent to the sample window of the digital filter. The sampled clock is from ADCCLK, and can be divided by COMPxLCTL.FLTDIV/COMPxHCTL.FLTDIV, the window size is defined by COMPxLCTL.FLTWIN/COMPxHCTL.FLTWIN. The digital filter can count the number of majority value of the sample window. If the number is larger than the pre-defined threshold value COMPxLCTL.FLTTH/COMPxHCTL.FLTTH, the filter output will change to the majority value; otherwise, the filter output will not be changed.

For proper operation, the threshold values should be greater than COMPxLCTL.FLTWIN/2 and COMPxHCTL.FLTWIN/2 respectively.

A conceptual model of the digital filter is shown in Figure 14-2.

Figure 14-2: Digital filter behavior



14.5 Power-up sequence

When powering up the COMP, the following sequence must be used:

Step 1: Power up ADC bandgap

Step 2: Power up the analog circuits of COMP

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14.6 Registers

14.6.1 Comparator register map

Table 14-2: Comparator Module Base Address

Peripheral Module	Base Address
COMP	0x4000 8C00

Table 14-3: Comparator Register Map

Register	Offset	Description	Reset Value
COMPFLTOUT	0x2F0	Comparator Filter Output Register	0x00000000
COMPSTS	0x2F4	Comparator Status Register	0x00000000
COMPSTSCLR	0x2F8	Comparator Status Clear Register	0x00000000
COMP0CTL*	0x2FC	Comparator 0 Control Register	0x00000000
COMP0LCTL*	0x300	COMP0L Control Register	0x00000088
COMP0HCTL*	0x304	COMP0H Control Register	0x00000088
COMP1CTL*	0x308	Comparator 1 Control Register	0x00000000
COMP1LCTL*	0x30C	COMP1L Control Register	0x00000088
COMP1HCTL*	0x310	COMP1H Control Register	0x00000088
COMP2CTL*	0x314	Comparator 2 Control Register	0x00000000
COMP2LCTL*	0x318	COMP2L Control Register	0x00000088
COMP2HCTL*	0x31C	COMP2H Control Register	0x00000088
COMP3CTL*	0x320	Comparator 3 Control Register	0x00000000
COMP3LCTL*	0x324	COMP3L Control Register	0x00000088
COMP3HCTL*	0x328	COMP3H Control Register	0x00000088
COMP4CTL*	0x32C	Comparator 4 Control Register	0x00000000
COMP4LCTL*	0x330	COMP4L Control Register	0x00000088
COMP4HCTL*	0x334	COMP4H Control Register	0x00000088
COMP5CTL*	0x338	Comparator 5 Control Register	0x00000000
COMP5LCTL*	0x33C	COMP5L Control Register	0x00000088
COMP5HCTL*	0x340	COMP5H Control Register	0x00000088
COMP6CTL*	0x344	Comparator 6 Control Register	0x00000000
COMP6LCTL*	0x348	COMP6L Control Register	0x00000088
COMP6HCTL*	0x34C	COMP6H Control Register	0x00000088
COMP7CTL*	0x350	Comparator 7 Control Register	0x00000000
COMP7LCTL*	0x354	COMP7L Control Register	0x00000088
COMP7HCTL*	0x358	COMP7H Control Register	0x00000088
DAC0CTL*	0x35C	DAC0 Control Register	0x00000002
DAC0CODE	0x360	DAC0 Code Register	0x00000000
DAC0CODEA	0x364	DAC0 Active Code Register	0x00000000
RAMP0DLY*	0x368	RAMP0 Delay Shadow Register	0x00000000
RAMP0DLYA	0x36C	RAMP0 Delay Active Register	0x00000000
RAMP0DEC*	0x370	RAMP0 Decrement Shadow Register	0x00000000

SPINTROL

Register	Offset	Description	Reset Value
RAMP0DECA	0x374	RAMP0 Decrement Active Register	0x00000000
RAMP0MAX*	0x378	RAMP0 Maximum Value Shadow Register	0x00000000
RAMP0MAXA	0x37C	RAMP0 Maximum Value Active Register	0x00000000
RAMP0CNT	0x380	RAMP0 Count Register	0x00000000
DAC1CTL*	0x384	DAC1 Control Register	0x00000002
DAC1CODE	0x388	DAC1 Code Register	0x00000000
DAC1CODEA	0x38C	DAC1 Active Code Register	0x00000000
RAMP1DLY*	0x390	RAMP1 Delay Shadow Register	0x00000000
RAMP1DLYA	0x394	RAMP1 Delay Active Register	0x00000000
RAMP1DEC*	0x398	RAMP1 Decrement Shadow Register	0x00000000
RAMP1DECA	0x39C	RAMP1 Decrement Active Register	0x00000000
RAMP1MAX	0x3A0	RAMP1 Maximum Value Shadow Register	0x00000000
RAMP1MAXA	0x3A4	RAMP1 Maximum Value Active Register	0x00000000
RAMP1CNT	0x3A8	RAMP1 Count Register	0x00000000
DAC2CTL*	0x3AC	DAC2 Control Register	0x00000002
DAC2CODE	0x3B0	DAC2 Code Register	0x00000000
DAC2CODEA	0x3B4	DAC2 Active Code Register	0x00000000
DAC3CTL*	0x3B8	DAC3 Control Register	0x00000002
DAC3CODE	0x3BC	DAC3 Code Register	0x00000000
DAC3CODEA	0x3C0	DAC3 Active Code Register	0x00000000
DAC4CTL*	0x3C4	DAC4 Control Register	0x00000002
DAC4CODE	0x3C8	DAC4 Code Register	0x00000000
DAC4CODEA	0x3CC	DAC4 Active Code Register	0x00000000
DAC5CTL*	0x3D0	DAC5 Control Register	0x00000002
DAC5CODE	0x3D4	DAC5 Code Register	0x00000000
DAC5CODEA	0x3D8	DAC5 Active Code Register	0x00000000
DACBUF0CTL*	0x3F4	DAC Buffer 0 Control Register	0x00000000
DACBUF1CTL*	0x3F8	DAC Buffer 1 Control Register	0x00000000
COMPREGKEY	0x3FC	COMP Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the COMPREGKEY=0x1ACCE551.

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14.6.2 Comparator registers

14.6.2.1 Comparator Filter Output Register (COMPFLTOUT)

Table 14-4: Comparator Filter Output Register (COMPFLTOUT) Layout

COMPFLTOUT (Comparator Filter Output Register) Offset: 0x2F0 Default: 0x00000000 Access: COMP -> COMPFLTOUT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 COMP7H	14 COMP7L	13 COMP6H	12 COMP6L	11 COMP5H	10 COMP5L	9 COMP4H	8 COMP4L
7 COMP3H	6 COMP3L	5 COMP2H	4 COMP2L	3 COMP1H	2 COMP1L	1 COMP0H	0 COMP0L

Table 14-5: Comparator Filter Output Register (COMPFLTOUT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	COMP7H	RO	0x0	COMP7H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
14	COMP7L	RO	0x0	COMP7L filtered status without latch 0: Input is higher than the low-boundary 1: Input is lower than the low-boundary
13	COMP6H	RO	0x0	COMP6H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
12	COMP6L	RO	0x0	COMP6L filtered status without latch 0: Input is higher than the low-boundary 1: Input is lower than the low-boundary
11	COMP5H	RO	0x0	COMP5H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
10	COMP5L	RO	0x0	COMP5L filtered status without latch 0: Input is higher than the low-boundary 1: Input is lower than the low-boundary
9	COMP4H	RO	0x0	COMP4H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
8	COMP4L	RO	0x0	COMP4L filtered status without latch

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Input is higher than the low-boundary 1: Input is lower than the low-boundary
7	COMP3H	RO	0x0	COMP3H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
6	COMP3L	RO	0x0	COMP3L filtered status without latch 0: Input is higher than the low-boundary 1: Input is lower than the low-boundary
5	COMP2H	RO	0x0	COMP2H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
4	COMP2L	RO	0x0	COMP2L filtered status without latch 0: Input is higher than the low-boundary 1: Input is lower than the low-boundary
3	COMP1H	RO	0x0	COMP1H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
2	COMP1L	RO	0x0	COMP1L filtered status without latch 0: Input is higher than the low-boundary 1: Input is lower than the low-boundary
1	COMP0H	RO	0x0	COMP0H filtered status without latch 0: Input is lower than the high-boundary 1: Input is higher than the high-boundary
0	COMP0L	RO	0x0	COMP0L filtered status without latch 0: Input is higher than the low-boundary 1: Input is lower than the low-boundary

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14.6.2.2 Comparator Status Register (COMPSTS)

Table 14-6: Comparator Status Register (COMPSTS) Layout

COMPSTS (Comparator Status Register) Offset: 0x2F4 Default: 0x00000000 Access: COMP -> COMPSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 COMP7H	14 COMP7L	13 COMP6H	12 COMP6L	11 COMP5H	10 COMP5L	9 COMP4H	8 COMP4L
7 COMP3H	6 COMP3L	5 COMP2H	4 COMP2L	3 COMP1H	2 COMP1L	1 COMP0H	0 COMP0L

Table 14-7: Comparator Status Register (COMPSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	COMP7H	RO	0x0	Latched COMPFLTOUT.COMP7H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
14	COMP7L	RO	0x0	Latched COMPFLTOUT.COMP7L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary
13	COMP6H	RO	0x0	Latched COMPFLTOUT.COMP6H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
12	COMP6L	RO	0x0	Latched COMPFLTOUT.COMP6L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary
11	COMP5H	RO	0x0	Latched COMPFLTOUT.COMP5H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
10	COMP5L	RO	0x0	Latched COMPFLTOUT.COMP5L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary
9	COMP4H	RO	0x0	Latched COMPFLTOUT.COMP4H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
8	COMP4L	RO	0x0	Latched COMPFLTOUT.COMP4L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary

SPINTROL

Bits	Field Name	Type	Reset	Description
7	COMP3H	RO	0x0	Latched COMPFLTOUT.COMP3H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
6	COMP3L	RO	0x0	Latched COMPFLTOUT.COMP3L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary
5	COMP2H	RO	0x0	Latched COMPFLTOUT.COMP2H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
4	COMP2L	RO	0x0	Latched COMPFLTOUT.COMP2L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary
3	COMP1H	RO	0x0	Latched COMPFLTOUT.COMP1H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
2	COMP1L	RO	0x0	Latched COMPFLTOUT.COMP1L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary
1	COMP0H	RO	0x0	Latched COMPFLTOUT.COMP0H 0: Input has been lower than the high-boundary 1: Input has been higher than the high-boundary
0	COMP0L	RO	0x0	Latched COMPFLTOUT.COMP0L 0: Input has been higher than the low-boundary 1: Input has been lower than the low-boundary

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14.6.2.3 Comparator Status Clear Register (COMPSTSCLR)

Table 14-8: Comparator Status Clear Register (COMPSTSCLR) Layout

COMPSTSCLR (Comparator Status Clear Register) Offset: 0x2F8 Default: 0x00000000 Access: COMP -> COMPSTSCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 COMP7H	14 COMP7L	13 COMP6H	12 COMP6L	11 COMP5H	10 COMP5L	9 COMP4H	8 COMP4L
7 COMP3H	6 COMP3L	5 COMP2H	4 COMP2L	3 COMP1H	2 COMP1L	1 COMP0H	0 COMP0L

Table 14-9: Comparator Status Clear Register (COMPSTSCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	COMP7H	W1C	0x0	Latched COMP7H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP7H. This bit is self-cleared to 0.
14	COMP7L	W1C	0x0	Latched COMP7L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP7L. This bit is self-cleared to 0.
13	COMP6H	W1C	0x0	Latched COMP6H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP6H. This bit is self-cleared to 0.
12	COMP6L	W1C	0x0	Latched COMP6L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP6L. This bit is self-cleared to 0.
11	COMP5H	W1C	0x0	Latched COMP5H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP5H. This bit is self-cleared to 0.
10	COMP5L	W1C	0x0	Latched COMP5L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP5L. This bit is self-cleared to 0.

SPINTROL

Bits	Field Name	Type	Reset	Description
9	COMP4H	W1C	0x0	Latched COMP4H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP4H. This bit is self-cleared to 0.
8	COMP4L	W1C	0x0	Latched COMP4L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP4L. This bit is self-cleared to 0.
7	COMP3H	W1C	0x0	Latched COMP3H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP3H. This bit is self-cleared to 0.
6	COMP3L	W1C	0x0	Latched COMP3L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP3L. This bit is self-cleared to 0.
5	COMP2H	W1C	0x0	Latched COMP2H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP2H. This bit is self-cleared to 0.
4	COMP2L	W1C	0x0	Latched COMP2L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP2L. This bit is self-cleared to 0.
3	COMP1H	W1C	0x0	Latched COMP1H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP1H. This bit is self-cleared to 0.
2	COMP1L	W1C	0x0	Latched COMP1L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP1L. This bit is self-cleared to 0.
1	COMP0H	W1C	0x0	Latched COMP0H status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP0H. This bit is self-cleared to 0.
0	COMP0L	W1C	0x0	Latched COMP0L status clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears COMPSTS.COMP0L. This bit is self-cleared to 0.

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14.6.2.4 Comparator 0 Control Register (COMP0CTL)

Table 14-10: Comparator 0 Control Register (COMP0CTL) Layout

COMP0CTL (Comparator 0 Control Register) Offset: 0x2FC Default: 0x00000000 Access: COMP -> COMP0CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-11: Comparator 0 Control Register (COMP0CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP0 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC2 as too-high, DAC3 as too-low reference 11: DAC3 as too-high, DAC2 as too-low reference When PHCMPEN=1 00: PGA0 positive output 01: PGA0 negative output 10: ADC1 input from GPIO1 11: ADC5 input from GPIO5
6:5	INSEL	RW	0x0	COMP0 input select 00: PGA0 negative output 01: PGA0 positive output 10: ADC0 input from GPIO0 11: ADC4 input from GPIO4

SPINTROL

Bits	Field Name	Type	Reset	Description
4:3	HYSTSEL	RW	0x0	COMP0 hysteresis select 00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP0 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP0H enable 0: Disable COMP0H 1: Enable COMP0H
0	ENL	RW	0x0	COMP0L enable 0: Disable COMP0L 1: Enable COMP0L

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14.6.2.5 COMP0L Control Register (COMP0LCTL)

Table 14-12: COMP0L Control Register (COMP0LCTL) Layout

COMP0LCTL (COMP0L Control Register) Offset: 0x300 Default: 0x00000088 Access: COMP -> COMP0LCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-13: COMP0L Control Register (COMP0LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP0L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP0L status 1: PWMSYNC will clear the latched COMP0L status
7	POL4GPIO	RW	0x1	COMP0L output polarity for GPIO 0: Output low upon COMP0L event 1: Output high upon COMP0L event
6:4	SEL4GPIO	RW	0x0	COMP0L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

SPINTROL

Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP0L output polarity for PWM 0: Output low upon COMP0L event 1: Output high upon COMP0L event
2:0	SEL4PWM	RW	0x0	COMP0L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.6 COMP0H Control Register (COMP0HCTL)

Table 14-14: COMP0H Control Register (COMP0HCTL) Layout

COMP0HCTL (COMP0H Control Register) Offset: 0x304 Default: 0x00000088 Access: COMP -> COMP0HCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-15: COMP0H Control Register (COMP0HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP0H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP0H status 1: PWMSYNC will clear the latched COMP0H status
7	POL4GPIO	RW	0x1	COMP0H output polarity for GPIO 0: Output low upon COMP0H event 1: Output high upon COMP0H event
6:4	SEL4GPIO	RW	0x0	COMP0H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

SPINTROL

Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP0H output polarity for PWM 0: Output low upon COMP0H event 1: Output high upon COMP0H event
2:0	SEL4PWM	RW	0x0	COMP0H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.7 Comparator 1 Control Register (COMP1CTL)

Table 14-16: Comparator 1 Control Register (COMP1CTL) Layout

COMP1CTL (Comparator 1 Control Register) Offset: 0x308 Default: 0x00000000 Access: COMP -> COMP1CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-17: Comparator 1 Control Register (COMP1CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP1 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC2 as too-high, DAC3 as too-low reference 11: DAC3 as too-high, DAC2 as too-low reference When PHCMPEN=1 00: PGA1 positive output 01: PGA1 negative output 10: ADC2 input from GPIO2 11: ADC7 input from GPIO7
6:5	INSEL	RW	0x0	COMP1 input select 00: PGA1 negative output 01: PGA1 positive output 10: ADC0 input from GPIO0 11: ADC6 input from GPIO6

SPINTROL

Bits	Field Name	Type	Reset	Description
4:3	HYSTSEL	RW	0x0	COMP1 hysteresis select 00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP1 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP1H enable 0: Disable COMP1H 1: Enable COMP1H
0	ENL	RW	0x0	COMP1L enable 0: Disable COMP1L 1: Enable COMP1L

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14.6.2.8 COMP1L Control Register (COMP1LCTL)

Table 14-18: COMP1L Control Register (COMP1LCTL) Layout

COMP1LCTL (COMP1L Control Register) Offset: 0x30C Default: 0x00000088 Access: COMP -> COMP1LCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-19: COMP1L Control Register (COMP1LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP1L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP1L status 1: PWMSYNC will clear the latched COMP1L status
7	POL4GPIO	RW	0x1	COMP1L output polarity for GPIO 0: Output 0 upon COMP1L event 1: Output 1 upon COMP1L event
6:4	SEL4GPIO	RW	0x0	COMP1L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

SPINTROL

Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP1L output polarity for PWM 0: Output low upon COMP1L event 1: Output high upon COMP1L event
2:0	SEL4PWM	RW	0x0	COMP1L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.9 COMP1H Control Register (COMP1HCTL)

Table 14-20: COMP1H Control Register (COMP1HCTL) Layout

COMP1HCTL (COMP1H Control Register) Offset: 0x310 Default: 0x00000088
Access: COMP -> COMP1HCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-21: COMP1H Control Register (COMP1HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP1H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP1H status 1: PWMSYNC will clear the latched COMP1H status
7	POL4GPIO	RW	0x1	COMP1H output polarity for GPIO 0: Output 0 upon COMP1H event 1: Output 1 upon COMP1H event
6:4	SEL4GPIO	RW	0x0	COMP1H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

SPINTROL

Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP1H output polarity for PWM 0: Output low upon COMP1H event 1: Output high upon COMP1H event
2:0	SEL4PWM	RW	0x0	COMP1H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.10 Comparator 2 Control Register (COMP2CTL)

Table 14-22: Comparator 2 Control Register (COMP2CTL) Layout

COMP2CTL (Comparator 2 Control Register) Offset: 0x314 Default: 0x00000000 Access: COMP -> COMP2CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-23: Comparator 2 Control Register (COMP2CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP2 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC2 as too-high, DAC3 as too-low reference 11: DAC3 as too-high, DAC2 as too-low reference When PHCMPEN=1 00: PGA2 positive output 01: PGA2 negative output 10: ADC3 input from GPIO3 11: ADC9 input from GPIO9
6:5	INSEL	RW	0x0	COMP2 input select 00: PGA2 negative output 01: PGA2 positive output 10: ADC0 input from GPIO0 11: ADC8 input from GPIO8
4:3	HYSTSEL	RW	0x0	COMP2 hysteresis select

SPINTROL

Bits	Field Name	Type	Reset	Description
				00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP2 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP2H enable 0: Disable COMP2H 1: Enable COMP2H
0	ENL	RW	0x0	COMP2L enable 0: Disable COMP2L 1: Enable COMP2L

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14.6.2.11 COMP2L Control Register (COMP2LCTL)

Table 14-24: COMP2L Control Register (COMP2LCTL) Layout

COMP2LCTL (COMP2L Control Register) Offset: 0x318 Default: 0x00000088
Access: COMP -> COMP2LCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-25: COMP2L Control Register (COMP2LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP2L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP2L status 1: PWMSYNC will clear the latched COMP2L status
7	POL4GPIO	RW	0x1	COMP2L output polarity for GPIO 0: Output low upon COMP2L event 1: Output high upon COMP2L event
6:4	SEL4GPIO	RW	0x0	COMP2L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

SPINTROL

Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP2L output polarity for PWM 0: Output low upon COMP2L event 1: Output high upon COMP2L event
2:0	SEL4PWM	RW	0x0	COMP2L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.12 COMP2H Control Register (COMP2HCTL)

Table 14-26: COMP2H Control Register (COMP2HCTL) Layout

COMP2HCTL (COMP2H Control Register) Offset: 0x31C Default: 0x00000088 Access: COMP -> COMP2HCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-27: COMP2H Control Register (COMP2HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP2H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP2H status 1: PWMSYNC will clear the latched COMP2H status
7	POL4GPIO	RW	0x1	COMP2H output polarity for GPIO 0: Output low upon COMP2H event 1: Output high upon COMP2H event
6:4	SEL4GPIO	RW	0x0	COMP2H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP2H output polarity for PWM 0: Output low upon COMP2H event 1: Output high upon COMP2H event
2:0	SEL4PWM	RW	0x0	COMP2H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.13 Comparator 3 Control Register (COMP3CTL)

Table 14-28: Comparator 3 Control Register (COMP3CTL) Layout

COMP3CTL (Comparator 3 Control Register) Offset: 0x320 Default: 0x00000000 Access: COMP -> COMP3CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-29: Comparator 3 Control Register (COMP3CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP3 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC4 as too-high, DAC5 as too-low reference 11: DAC5 as too-high, DAC4 as too-low reference When PHCMPEN=1 00: PGA3 positive output 01: PGA3 negative output 10: ADC11 input from GPIO11 11: ADC15 input from GPIO15
6:5	INSEL	RW	0x0	COMP3 input select 00: PGA3 negative output 01: PGA3 positive output 10: ADC10 input from GPIO10 11: ADC14 input from GPIO14
4:3	HYSTSEL	RW	0x0	COMP3 hysteresis select

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Bits	Field Name	Type	Reset	Description
				00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP3 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP3H enable 0: Disable COMP3H 1: Enable COMP3H
0	ENL	RW	0x0	COMP3L enable 0: Disable COMP3L 1: Enable COMP3L

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14.6.2.14 COMP3L Control Register (COMP3LCTL)

Table 14-30: COMP3L Control Register (COMP3LCTL) Layout

COMP3LCTL (COMP3L Control Register) Offset: 0x324 Default: 0x00000088 Access: COMP -> COMP3LCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-31: COMP3L Control Register (COMP3LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP3L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP3L status 1: PWMSYNC will clear the latched COMP3L status
7	POL4GPIO	RW	0x1	COMP3L output polarity for GPIO 0: Output low upon COMP3L event 1: Output high upon COMP3L event
6:4	SEL4GPIO	RW	0x0	COMP3L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP3L output polarity for PWM 0: Output low upon COMP3L event 1: Output high upon COMP3L event
2:0	SEL4PWM	RW	0x0	COMP3L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.15 COMP3H Control Register (COMP3HCTL)

Table 14-32: COMP3H Control Register (COMP3HCTL) Layout

COMP3HCTL (COMP3H Control Register) Offset: 0x328 Default: 0x00000088
Access: COMP -> COMP3HCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-33: COMP3H Control Register (COMP3HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP3H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP3H status 1: PWMSYNC will clear the latched COMP3H status
7	POL4GPIO	RW	0x1	COMP3H output polarity for GPIO 0: Output low upon COMP3H event 1: Output high upon COMP3H event
6:4	SEL4GPIO	RW	0x0	COMP3H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output
3	POL4PWM	RW	0x1	COMP3H output polarity for PWM

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Bits	Field Name	Type	Reset	Description
				0: Output low upon COMP3H event 1: Output high upon COMP3H event
2:0	SEL4PWM	RW	0x0	COMP3H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.16 Comparator 4 Control Register (COMP4CTL)

Table 14-34: Comparator 4 Control Register (COMP4CTL) Layout

COMP4CTL (Comparator 4 Control Register) Offset: 0x32C Default: 0x00000000 Access: COMP -> COMP4CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-35: Comparator 4 Control Register (COMP4CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP4 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC4 as too-high, DAC5 as too-low reference 11: DAC5 as too-high, DAC4 as too-low reference When PHCMPEN=1 00: PGA4 positive output 01: PGA4 negative output 10: ADC12 input from GPIO12 11: ADC17 input from GPIO17
6:5	INSEL	RW	0x0	COMP4 input select 00: PGA4 negative out 01: PGA4 positive output 10: ADC10 input from GPIO10 11: ADC16 input from GPIO16
4:3	HYSTSEL	RW	0x0	COMP4 hysteresis select

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Bits	Field Name	Type	Reset	Description
				00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP4 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP4H enable 0: Disable COMP4H 1: Enable COMP4H
0	ENL	RW	0x0	COMP4L enable 0: Disable COMP4L 1: Enable COMP4L

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14.6.2.17 COMP4L Control Register (COMP4LCTL)

Table 14-36: COMP4L Control Register (COMP4LCTL) Layout

COMP4LCTL (COMP4L Control Register) Offset: 0x330 Default: 0x00000088
Access: COMP -> COMP4LCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-37: COMP4L Control Register (COMP4LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP4L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP4L status 1: PWMSYNC will clear the latched COMP4L status
7	POL4GPIO	RW	0x1	COMP4L output polarity for GPIO 0: Output low upon COMP4L event 1: Output high upon COMP4L event
6:4	SEL4GPIO	RW	0x0	COMP4L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP4L output polarity for PWM 0: Output low upon COMP4L event 1: Output high upon COMP4L event
2:0	SEL4PWM	RW	0x0	COMP4L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.18 COMP4H Control Register (COMP4HCTL)

Table 14-38: COMP4H Control Register (COMP4HCTL) Layout

COMP4HCTL (COMP4H Control Register) Offset: 0x334 Default: 0x00000088
Access: COMP -> COMP4HCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-39: COMP4H Control Register (COMP4HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP4H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP4H status 1: PWMSYNC will clear the latched COMP4H status
7	POL4GPIO	RW	0x1	COMP4H output polarity for GPIO 0: Output low upon COMP4H event 1: Output high upon COMP4H event
6:4	SEL4GPIO	RW	0x0	COMP4H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output
3	POL4PWM	RW	0x1	COMP4H output polarity for PWM 0: Output low upon COMP4H event 1: Output high upon COMP4H event

SPINTROL

Bits	Field Name	Type	Reset	Description
2:0	SEL4PWM	RW	0x0	COMP4H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.19 Comparator 5 Control Register (COMP5CTL)

Table 14-40: Comparator 5 Control Register (COMP5CTL) Layout

COMP5CTL (Comparator 5 Control Register) Offset: 0x338 Default: 0x00000000 Access: COMP -> COMP5CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-41: Comparator 5 Control Register (COMP5CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP5 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC4 as too-high, DAC5 as too-low reference 11: DAC5 as too-high, DAC4 as too-low reference When PHCMPEN=1 00: PGA5 positive output 01: PGA5 negative output 10: ADC13 input from GPIO13 11: ADC19 input from GPIO19
6:5	INSEL	RW	0x0	COMP5 input select 00: PGA5 negative output 01: PGA5 positive output 10: ADC10 input from GPIO10 11: ADC18 input from GPIO18
4:3	HYSTSEL	RW	0x0	COMP5 hysteresis select

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Bits	Field Name	Type	Reset	Description
				00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP5 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP5H enable 0: Disable COMP5H 1: Enable COMP5H
0	ENL	RW	0x0	COMP5L enable 0: Disable COMP5L 1: Enable COMP5L

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14.6.2.20 COMP5L Control Register (COMP5LCTL)

Table 14-42: COMP5L Control Register (COMP5LCTL) Layout

COMP5LCTL (COMP5L Control Register) Offset: 0x33C Default: 0x00000088 Access: COMP -> COMP5LCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-43: COMP5L Control Register (COMP5LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP5L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP5L status 1: PWMSYNC will clear the latched COMP5L status
7	POL4GPIO	RW	0x1	COMP5L output polarity for GPIO 0: Output low upon COMP5L event 1: Output high upon COMP5L event
6:4	SEL4GPIO	RW	0x0	COMP5L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP5L output polarity for PWM 0: Output low upon COMP5L event 1: Output high upon COMP5L event
2:0	SEL4PWM	RW	0x0	COMP5L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.21 COMP5H Control Register (COMP5HCTL)

Table 14-44: COMP5H Control Register (COMP5HCTL) Layout

COMP5HCTL (COMP5H Control Register) Offset: 0x340 Default: 0x00000088
Access: COMP -> COMP5HCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-45: COMP5H Control Register (COMP5HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP5H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP5H status 1: PWMSYNC will clear the latched COMP5H status
7	POL4GPIO	RW	0x1	COMP5H output polarity for GPIO 0: Output low upon COMP5H event 1: Output high upon COMP5H event
6:4	SEL4GPIO	RW	0x0	COMP5H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output
3	POL4PWM	RW	0x1	COMP5H output polarity for PWM

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Output low upon COMP5H event 1: Output high upon COMP5H event
2:0	SEL4PWM	RW	0x0	COMP5H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.22 Comparator 6 Control Register (COMP6CTL)

Table 14-46: Comparator 6 Control Register (COMP6CTL) Layout

COMP6CTL (Comparator 6 Control Register) Offset: 0x344 Default: 0x00000000 Access: COMP -> COMP6CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-47: Comparator 6 Control Register (COMP6CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP6 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC2 as too-high, DAC3 as too-low reference 11: DAC3 as too-high, DAC2 as too-low reference When PHCMPEN=1 00: ADC3 input from GPIO3 01: ADC7 input from GPIO7 10: ADC13 input from GPIO13 11: ADC17 input from GPIO17
6:5	INSEL	RW	0x0	COMP6 input select 00: ADC2 input from GPIO2 01: ADC6 input from GPIO6 10: ADC12 input from GPIO12 11: ADC16 input from GPIO16
4:3	HYSTSEL	RW	0x0	COMP6 hysteresis select

SPINTROL

Bits	Field Name	Type	Reset	Description
				00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP6 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP6H enable 0: Disable COMP6H 1: Enable COMP6H
0	ENL	RW	0x0	COMP6L enable 0: Disable COMP6L 1: Enable COMP6L

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14.6.2.23 COMP6L Control Register (COMP6LCTL)

Table 14-48: COMP6L Control Register (COMP6LCTL) Layout

COMP6LCTL (COMP6L Control Register) Offset: 0x348 Default: 0x00000088
Access: COMP -> COMP6LCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-49: COMP6L Control Register (COMP6LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP6L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP6L status 1: PWMSYNC will clear the latched COMP6L status
7	POL4GPIO	RW	0x1	COMP6L output polarity for GPIO 0: Output low upon COMP6L event 1: Output high upon COMP6L event
6:4	SEL4GPIO	RW	0x0	COMP6L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP6L output polarity for PWM 0: Output low upon COMP6L event 1: Output high upon COMP6L event
2:0	SEL4PWM	RW	0x0	COMP6L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.24 COMP6H Control Register (COMP6HCTL)

Table 14-50: COMP6H Control Register (COMP6HCTL) Layout

COMP6HCTL (COMP6H Control Register) Offset: 0x34C Default: 0x00000088 Access: COMP -> COMP6HCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-51: COMP6H Control Register (COMP6HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP6H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP6H status 1: PWMSYNC will clear the latched COMP6H status
7	POL4GPIO	RW	0x1	COMP6H output polarity for GPIO 0: Output low upon COMP6H event 1: Output high upon COMP6H event
6:4	SEL4GPIO	RW	0x0	COMP6H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output
3	POL4PWM	RW	0x1	COMP6H output polarity for PWM

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Output low upon COMP6H event 1: Output high upon COMP6H event
2:0	SEL4PWM	RW	0x0	COMP6H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.25 Comparator 7 Control Register (COMP7CTL)

Table 14-52: Comparator 7 Control Register (COMP7CTL) Layout

COMP7CTL (Comparator 7 Control Register) Offset: 0x350 Default: 0x00000000 Access: COMP -> COMP7CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				SYNCSEL			REFSEL
7	6	5	4	3	2	1	0
REFSEL	INSEL		HYSTSEL		PHCMPEN	ENH	ENL

Table 14-53: Comparator 7 Control Register (COMP7CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:9	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
8:7	REFSEL	RW	0x0	COMP7 reference select When PHCMPEN=0 00: DAC0 as too-high, DAC1 as too-low reference 01: DAC1 as too-high, DAC0 as too-low reference 10: DAC4 as too-high, DAC5 as too-low reference 11: DAC5 as too-high, DAC4 as too-low reference When PHCMPEN=1 00: ADC5 input from GPIO5 01: ADC9 input from GPIO9 10: ADC15 input from GPIO15 11: ADC19 input from GPIO19
6:5	INSEL	RW	0x0	COMP7 input select 00: ADC4 input from GPIO4 01: ADC8 input from GPIO8 10: ADC14 input from GPIO14 11: ADC18 input from GPIO18
4:3	HYSTSEL	RW	0x0	COMP7 hysteresis select

SPINTROL

Bits	Field Name	Type	Reset	Description
				00: 0 mV 01: 12 mV 10: 24 mV 11: 36 mV
2	PHCMPEN	RW	0x0	COMP7 phase comparison enable 0: Normal operation 1: Phase comparison mode
1	ENH	RW	0x0	COMP7H enable 0: Disable COMP7H 1: Enable COMP7H
0	ENL	RW	0x0	COMP7L enable 0: Disable COMP7L 1: Enable COMP7L

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14.6.2.26 COMP7L Control Register (COMP7LCTL)

Table 14-54: COMP7L Control Register (COMP7LCTL) Layout

COMP7LCTL (COMP7L Control Register) Offset: 0x354 Default: 0x00000088
Access: COMP -> COMP7LCTL.all

31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-55: COMP7L Control Register (COMP7LCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP7L status clear by PWMSYNC 0: PWMSYNC does not affect the COMP7L status 1: PWMSYNC will clear the latched COMP7L status
7	POL4GPIO	RW	0x1	COMP7L output polarity for GPIO 0: Output low upon COMP7L event 1: Output high upon COMP7L event
6:4	SEL4GPIO	RW	0x0	COMP7L output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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Bits	Field Name	Type	Reset	Description
3	POL4PWM	RW	0x1	COMP7L output polarity for PWM 0: Output low upon COMP7L event 1: Output high upon COMP7L event
2:0	SEL4PWM	RW	0x0	COMP7L output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.27 COMP7H Control Register (COMP7HCTL)

Table 14-56: COMP7H Control Register (COMP7HCTL) Layout

COMP7HCTL (COMP7H Control Register) Offset: 0x358 Default: 0x00000088 Access: COMP -> COMP7HCTL.all							
31	30	29	28	27	26	25	24
RESERVED		FLTRST	FLTTH				
23	22	21	20	19	18	17	16
FLTWIN					FLTDIV		
15	14	13	12	11	10	9	8
FLTDIV							SYNCCLREN
7	6	5	4	3	2	1	0
POL4GPIO	SEL4GPIO			POL4PWM	SEL4PWM		

Table 14-57: COMP7H Control Register (COMP7HCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:30	RESERVED_31_30	RO	0x0	Reserved
29	FLTRST	W1C	0x0	Reset all registers in the filter with the input 0: Write 0 has no effect and always read back 0. 1: Write 1 will fill all filter registers with the input This bit is self-cleared to 0
28:24	FLTTH	RW	0x0	Threshold is (FLTTH+1) 1's/0's for output to toggle
23:19	FLTWIN	RW	0x0	Filter's window size is (FLTWIN+1) samples
18:9	FLTDIV	RW	0x0	Filter's clock dividing ratio is (FLTDIV+1)
8	SYNCCLREN	RW	0x0	Enable latched COMP7H status clear by PWMSYNC 0: PWMSYNC does not affect the COMP7H status 1: PWMSYNC will clear the latched COMP7H status
7	POL4GPIO	RW	0x1	COMP7H output polarity for GPIO 0: Output low upon COMP7H event 1: Output high upon COMP7H event
6:4	SEL4GPIO	RW	0x0	COMP7H output select for GPIO 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output
3	POL4PWM	RW	0x1	COMP7H output polarity for PWM

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Bits	Field Name	Type	Reset	Description
				0: Output low upon COMP7H event 1: Output high upon COMP7H event
2:0	SEL4PWM	RW	0x0	COMP7H output select for PWM 000: Original output 001: Synchronous output with ADC clock 010: Digital filter output 011: Latched digital filter output 100: Original output or latched digital filter output 101: Synchronous output with ADC clock or latched digital filter output 110: Digital filter output or the latched one 111: Original output or synchronous output with ADC clock or latched digital filter output

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14.6.2.28 DAC0 Control Register (DAC0CTL)

Table 14-58: DAC0 Control Register (DAC0CTL) Layout

DAC0CTL (DAC0 Control Register) Offset: 0x35C Default: 0x00000002 Access: COMP -> DAC0CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				DBGRUN		COMPHSEL	
7	6	5	4	3	2	1	0
COMPHSEL	RAMPLOAD	RAMPEN	SYNCSEL			CODELOAD	EN

Table 14-59: DAC0 Control Register (DAC0CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:10	DBGRUN	RW	0x0	Ramping behavior on CPU halted or lockup 00: Stop ramping immediately 01: Stop ramping at PWM synchronous event 1x: Free running
9:7	COMPHSEL	RW	0x0	COMPH select Note: This field is only used for RAMP function 000: COMP0H 001: COMP1H 010: COMP2H 011: COMP3H 100: COMP4H 101: COMP5H 110: COMP6H 111: COMP7H
6	RAMPLOAD	RW	0x0	DAC Ramp load mode 0: Register shadowing is applied for ramping counter load from RAMPMAX 1: RAMP counter is directly loaded from the latest RAMPMAX
5	RAMPEN	RW	0x0	DAC Ramping enable 0: Disable ramping 1: Enable ramping. DAC0CODEA is equivalent to the 10 MSBs of RAMP0CNT

SPINTROL

Bits	Field Name	Type	Reset	Description
4:2	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
1	CODELOAD	RW	0x1	DAC code load mode 0: DAC code is updated upon PWMSYNC event 1: DAC code is immediately updated by writing to DAC0CODE
0	EN	RW	0x0	DAC enable 0: Disable 1: Enable

14.6.2.29 DAC0 Code Register (DAC0CODE)

Table 14-60: DAC0 Code Register (DAC0CODE) Layout

DAC0CODE (DAC0 Code Register) Offset: 0x360 Default: 0x00000000
Access: COMP -> DAC0CODE.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-61: DAC0 Code Register (DAC0CODE) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	VAL	RW	0x0	DAC code When DAC0CTL.CODELOAD=0, write to this field only affects the shadow code. When DAC0CTL.CODELOAD=1, write to this field affects both the shadow code and the active code.

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14.6.2.30 DAC0 Active Code Register (DAC0CODEA)

Table 14-62: DAC0 Active Code Register (DAC0CODEA) Layout

DAC0CODEA (DAC0 Active Code Register) Offset: 0x364 Default: 0x00000000 Access: COMP -> DAC0CODEA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-63: DAC0 Active Code Register (DAC0CODEA) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	CODEA	RO	0x0	Active DAC code

14.6.2.31 RAMP0 Delay Shadow Register (RAMP0DLY)

Table 14-64: RAMP0 Delay Shadow Register (RAMP0DLY) Layout

RAMP0DLY (RAMP0 Delay Shadow Register) Offset: 0x368 Default: 0x00000000 Access: COMP -> RAMP0DLY.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-65: RAMP0 Delay Shadow Register (RAMP0DLY) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Delay from PWMSYNC to start of ramping

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14.6.2.32 RAMP0 Delay Active Register (RAMP0DLYA)

Table 14-66: RAMP0 Delay Active Register (RAMP0DLYA) Layout

RAMP0DLYA (RAMP0 Delay Active Register) Offset: 0x36C Default: 0x00000000 Access: COMP -> RAMP0DLYA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-67: RAMP0 Delay Active Register (RAMP0DLYA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Delay from PWMSYNC to start of ramping

14.6.2.33 RAMP0 Decrement Shadow Register (RAMP0DEC)

Table 14-68: RAMP0 Decrement Shadow Register (RAMP0DEC) Layout

RAMP0DEC (RAMP0 Decrement Shadow Register) Offset: 0x370 Default: 0x00000000 Access: COMP -> RAMP0DEC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-69: RAMP0 Decrement Shadow Register (RAMP0DEC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Step size for decremental ramping

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14.6.2.34 RAMP0 Decrement Active Register (RAMP0DECA)

Table 14-70: RAMP0 Decrement Active Register (RAMP0DECA) Layout

RAMP0DECA (RAMP0 Decrement Active Register) Offset: 0x374 Default: 0x00000000 Access: COMP -> RAMP0DECA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-71: RAMP0 Decrement Active Register (RAMP0DECA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Step size for decremental ramping

14.6.2.35 RAMP0 Maximum Value Shadow Register (RAMP0MAX)

Table 14-72: RAMP0 Maximum Value Shadow Register (RAMP0MAX) Layout

RAMP0MAX (RAMP0 Maximum Value Shadow Register) Offset: 0x378 Default: 0x00000000 Access: COMP -> RAMP0MAX.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-73: RAMP0 Maximum Value Shadow Register (RAMP0MAX) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Maximum value when reset ramping

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14.6.2.36 RAMP0 Maximum Value Active Register (RAMP0MAXA)

Table 14-74: RAMP0 Maximum Value Active Register (RAMP0MAXA) Layout

RAMP0MAXA (RAMP0 Maximum Value Active Register) Offset: 0x37C Default: 0x00000000 Access: COMP -> RAMP0MAXA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-75: RAMP0 Maximum Value Active Register (RAMP0MAXA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Maximum value when reset ramping

14.6.2.37 RAMP0 Count Register (RAMP0CNT)

Table 14-76: RAMP0 Count Register (RAMP0CNT) Layout

RAMP0CNT (RAMP0 Count Register) Offset: 0x380 Default: 0x00000000 Access: COMP -> RAMP0CNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-77: RAMP0 Count Register (RAMP0CNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Count number of RAMP0

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14.6.2.38 DAC1 Control Register (DAC1CTL)

Table 14-78: DAC1 Control Register (DAC1CTL) Layout

DAC1CTL (DAC1 Control Register) Offset: 0x384 Default: 0x00000002 Access: COMP -> DAC1CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				DBGRUN		COMPHSEL	
7	6	5	4	3	2	1	0
COMPHSEL	RAMPLOAD	RAMPEN	SYNCSEL			CODELOAD	EN

Table 14-79: DAC1 Control Register (DAC1CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11:10	DBGRUN	RW	0x0	Ramping behavior on CPU halted or lockup 00: Stop ramping immediately 01: Stop ramping at PWM synchronous event 1x: Free running
9:7	COMPHSEL	RW	0x0	COMPH select Note: This field is only used for RAMP function 000: COMP0H 001: COMP1H 010: COMP2H 011: COMP3H 100: COMP4H 101: COMP5H 110: COMP6H 111: COMP7H
6	RAMPLOAD	RW	0x0	DAC Ramp load mode 0: Register shadowing is applied for ramping counter load from RAMPMAX 1: RAMP counter is directly loaded from the latest RAMPMAX
5	RAMPEN	RW	0x0	DAC Ramping enable 0: Disable ramping 1: Enable ramping. DAC1CODEA is equivalent to the 10 MSBs of RAMP1CNT

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Bits	Field Name	Type	Reset	Description
4:2	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
1	CODELOAD	RW	0x1	DAC code load mode 0: DAC code is updated upon PWMSYNC event 1: DAC code is immediately updated by writing to DAC1CODE
0	EN	RW	0x0	DAC enable 0: Disable 1: Enable

14.6.2.39 DAC1 Code Register (DAC1CODE)

Table 14-80: DAC1 Code Register (DAC1CODE) Layout

DAC1CODE (DAC1 Code Register) Offset: 0x388 Default: 0x00000000
Access: COMP -> DAC1CODE.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-81: DAC1 Code Register (DAC1CODE) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	VAL	RW	0x0	DAC code When DAC1CTL.CODELOAD=0, write to this field only affects the shadow code. When DAC1CTL.CODELOAD=1, write to this field affects both the shadow code and the active code.

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14.6.2.40 DAC1 Active Code Register (DAC1CODEA)

Table 14-82: DAC1 Active Code Register (DAC1CODEA) Layout

DAC1CODEA (DAC1 Active Code Register) Offset: 0x38C Default: 0x00000000 Access: COMP -> DAC1CODEA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-83: DAC1 Active Code Register (DAC1CODEA) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	CODEA	RO	0x0	Active DAC code

14.6.2.41 RAMP1 Delay Shadow Register (RAMP1DLY)

Table 14-84: RAMP1 Delay Shadow Register (RAMP1DLY) Layout

RAMP1DLY (RAMP1 Delay Shadow Register) Offset: 0x390 Default: 0x00000000 Access: COMP -> RAMP1DLY.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-85: RAMP1 Delay Shadow Register (RAMP1DLY) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Delay from PWMSYNC to start of ramping

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14.6.2.42 RAMP1 Delay Active Register (RAMP1DLYA)

Table 14-86: RAMP1 Delay Active Register (RAMP1DLYA) Layout

RAMP1DLYA (RAMP1 Delay Active Register) Offset: 0x394 Default: 0x00000000 Access: COMP -> RAMP1DLYA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-87: RAMP1 Delay Active Register (RAMP1DLYA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Delay from PWMSYNC to start of ramping

14.6.2.43 RAMP1 Decrement Shadow Register (RAMP1DEC)

Table 14-88: RAMP1 Decrement Shadow Register (RAMP1DEC) Layout

RAMP1DEC (RAMP1 Decrement Shadow Register) Offset: 0x398 Default: 0x00000000 Access: COMP -> RAMP1DEC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-89: RAMP1 Decrement Shadow Register (RAMP1DEC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Step size for decremental ramping

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14.6.2.44 RAMP1 Decrement Active Register (RAMP1DECA)

Table 14-90: RAMP1 Decrement Active Register (RAMP1DECA) Layout

RAMP1DECA (RAMP1 Decrement Active Register) Offset: 0x39C Default: 0x00000000 Access: COMP -> RAMP1DECA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-91: RAMP1 Decrement Active Register (RAMP1DECA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Step size for decremental ramping

14.6.2.45 RAMP1 Maximum Value Shadow Register (RAMP1MAX)

Table 14-92: RAMP1 Maximum Value Shadow Register (RAMP1MAX) Layout

RAMP1MAX (RAMP1 Maximum Value Shadow Register) Offset: 0x3A0 Default: 0x00000000 Access: COMP -> RAMP1MAX.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-93: RAMP1 Maximum Value Shadow Register (RAMP1MAX) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x0	Maximum value when reset ramping

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14.6.2.46 RAMP1 Maximum Value Active Register (RAMP1MAXA)

Table 14-94: RAMP1 Maximum Value Active Register (RAMP1MAXA) Layout

RAMP1MAXA (RAMP1 Maximum Value Active Register) Offset: 0x3A4 Default: 0x00000000 Access: COMP -> RAMP1MAXA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-95: RAMP1 Maximum Value Active Register (RAMP1MAXA) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Maximum value when reset ramping

14.6.2.47 RAMP1 Count Register (RAMP1CNT)

Table 14-96: RAMP1 Count Register (RAMP1CNT) Layout

RAMP1CNT (RAMP1 Count Register) Offset: 0x3A8 Default: 0x00000000 Access: COMP -> RAMP1CNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 14-97: RAMP1 Count Register (RAMP1CNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RO	0x0	Count number of RAMP1

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14.6.2.48 DAC2 Control Register (DAC2CTL)

Table 14-98: DAC2 Control Register (DAC2CTL) Layout

DAC2CTL (DAC2 Control Register) Offset: 0x3AC Default: 0x00000002 Access: COMP -> DAC2CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			SYNCSEL			CODELOAD	EN

Table 14-99: DAC2 Control Register (DAC2CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4:2	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
1	CODELOAD	RW	0x1	DAC code load mode 0: DAC code is updated upon PWMSYNC event 1: DAC code is immediately updated by writing to DAC2CODE
0	EN	RW	0x0	DAC enable 0: Disable 1: Enable

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14.6.2.49 DAC2 Code Register (DAC2CODE)

Table 14-100: DAC2 Code Register (DAC2CODE) Layout

DAC2CODE (DAC2 Code Register) Offset: 0x3B0 Default: 0x00000000 Access: COMP -> DAC2CODE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-101: DAC2 Code Register (DAC2CODE) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	VAL	RW	0x0	DAC code When DAC2CTL.CODELOAD=0, write to this field only affects the shadow code. When DAC2CTL.CODELOAD=1, write to this field affects both the shadow code and the active code.

14.6.2.50 DAC2 Active Code Register (DAC2CODEA)

Table 14-102: DAC2 Active Code Register (DAC2CODEA) Layout

DAC2CODEA (DAC2 Active Code Register) Offset: 0x3B4 Default: 0x00000000 Access: COMP -> DAC2CODEA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-103: DAC2 Active Code Register (DAC2CODEA) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	CODEA	RO	0x0	Active DAC code

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14.6.2.51 DAC3 Control Register (DAC3CTL)

Table 14-104: DAC3 Control Register (DAC3CTL) Layout

DAC3CTL (DAC3 Control Register) Offset: 0x3B8 Default: 0x00000002 Access: COMP -> DAC3CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			SYNCSEL			CODELOAD	EN

Table 14-105: DAC3 Control Register (DAC3CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4:2	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
1	CODELOAD	RW	0x1	DAC code load mode 0: DAC code is updated upon PWMSYNC event 1: DAC code is immediately updated by writing to DAC3CODE
0	EN	RW	0x0	DAC enable 0: Disable 1: Enable

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14.6.2.52 DAC3 Code Register (DAC3CODE)

Table 14-106: DAC3 Code Register (DAC3CODE) Layout

DAC3CODE (DAC3 Code Register) Offset: 0x3BC Default: 0x00000000 Access: COMP -> DAC3CODE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-107: DAC3 Code Register (DAC3CODE) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	VAL	RW	0x0	DAC code When DAC3CTL.CODELOAD=0, write to this field only affects the shadow code. When DAC3CTL.CODELOAD=1, write to this field affects both the shadow code and the active code.

14.6.2.53 DAC3 Active Code Register (DAC3CODEA)

Table 14-108: DAC3 Active Code Register (DAC3CODEA) Layout

DAC3CODEA (DAC3 Active Code Register) Offset: 0x3C0 Default: 0x00000000 Access: COMP -> DAC3CODEA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-109: DAC3 Active Code Register (DAC3CODEA) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	CODEA	RO	0x0	Active DAC code

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14.6.2.54 DAC4 Control Register (DAC4CTL)

Table 14-110: DAC4 Control Register (DAC4CTL) Layout

DAC4CTL (DAC4 Control Register) Offset: 0x3C4 Default: 0x00000002 Access: COMP -> DAC4CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			SYNCSEL			CODELOAD	EN

Table 14-111: DAC4 Control Register (DAC4CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4:2	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
1	CODELOAD	RW	0x1	DAC code load mode 0: DAC code is updated upon PWMSYNC event 1: DAC code is immediately updated by writing to DAC4CODE
0	EN	RW	0x0	DAC enable 0: Disable 1: Enable

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14.6.2.55 DAC4 Code Register (DAC4CODE)

Table 14-112: DAC4 Code Register (DAC4CODE) Layout

DAC4CODE (DAC4 Code Register) Offset: 0x3C8 Default: 0x00000000 Access: COMP -> DAC4CODE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-113: DAC4 Code Register (DAC4CODE) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	VAL	RW	0x0	DAC code When DAC4CTL.CODELOAD=0, write to this field only affects the shadow code. When DAC4CTL.CODELOAD=1, write to this field affects both the shadow code and the active code.

14.6.2.56 DAC4 Active Code Register (DAC4CODEA)

Table 14-114: DAC4 Active Code Register (DAC4CODEA) Layout

DAC4CODEA (DAC4 Active Code Register) Offset: 0x3CC Default: 0x00000000 Access: COMP -> DAC4CODEA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-115: DAC4 Active Code Register (DAC4CODEA) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	CODEA	RO	0x0	Active DAC code

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14.6.2.57 DAC5 Control Register (DAC5CTL)

Table 14-116: DAC5 Control Register (DAC5CTL) Layout

DAC5CTL (DAC5 Control Register) Offset: 0x3D0 Default: 0x00000002 Access: COMP -> DAC5CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			SYNCSEL			CODELOAD	EN

Table 14-117: DAC5 Control Register (DAC5CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4:2	SYNCSEL	RW	0x0	PWM synchronous output select 000: PWM0 synchronous output 001: PWM1 synchronous output 010: PWM2 synchronous output 011: PWM3 synchronous output 100: PWM4 synchronous output 101: PWM5 synchronous output 110: PWM6 synchronous output 111: PWM7 synchronous output
1	CODELOAD	RW	0x1	DAC code load mode 0: DAC code is updated upon PWMSYNC event 1: DAC code is immediately updated by writing to DAC5CODE
0	EN	RW	0x0	DAC enable 0: Disable 1: Enable

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14.6.2.58 DAC5 Code Register (DAC5CODE)

Table 14-118: DAC5 Code Register (DAC5CODE) Layout

DAC5CODE (DAC5 Code Register) Offset: 0x3D4 Default: 0x00000000 Access: COMP -> DAC5CODE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-119: DAC5 Code Register (DAC5CODE) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	VAL	RW	0x0	DAC code When DAC5CTL.CODELOAD=0, write to this field only affects the shadow code. When DAC5CTL.CODELOAD=1, write to this field affects both the shadow code and the active code.

14.6.2.59 DAC5 Active Code Register (DAC5CODEA)

Table 14-120: DAC5 Active Code Register (DAC5CODEA) Layout

DAC5CODEA (DAC5 Active Code Register) Offset: 0x3D8 Default: 0x00000000 Access: COMP -> DAC5CODEA.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 14-121: DAC5 Active Code Register (DAC5CODEA) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	CODEA	RO	0x0	Active DAC code

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14.6.2.60 DAC Buffer 0 Control Register (DACBUF0CTL)

Table 14-122: DAC Buffer 0 Control Register (DACBUF0CTL) Layout

DACBUF0CTL (DAC Buffer 0 Control Register) Offset: 0x3F4 Default: 0x00000000 Access: COMP -> DACBUF0CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				OE	INSEL		EN

Table 14-123: DAC Buffer 0 Control Register (DACBUF0CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	OE	RW	0x0	Enable output to GPIO10 pin 0: Disable 1: Enable
2:1	INSEL	RW	0x0	DAC buffer input select 00: DAC0 01: DAC1 10: DAC2 11: DAC3
0	EN	RW	0x0	DAC buffer enable 0: Disable 1: Enable

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14.6.2.61 DAC Buffer 1 Control Register (DACBUF1CTL)

Table 14-124: DAC Buffer 1 Control Register (DACBUF1CTL) Layout

DACBUF1CTL (DAC Buffer 1 Control Register) Offset: 0x3F8 Default: 0x00000000 Access: COMP -> DACBUF1CTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED				OE	INSEL		EN

Table 14-125: DAC Buffer 1 Control Register (DACBUF1CTL) Field Description

Bits	Field Name	Type	Reset	Description
31:4	RESERVED_31_4	RO	0x0	Reserved
3	OE	RW	0x0	Enable output to GPIO13 pin 0: Disable 1: Enable
2:1	INSEL	RW	0x0	DAC buffer 1 input select 00: DAC0 01: DAC1 10: DAC4 11: DAC5
0	EN	RW	0x0	DAC buffer 1 enable 0: Disable 1: Enable

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14.6.2.62 COMP Register Write-Allow Key Register (COMPREGKEY)

Table 14-126: COMP Register Write-Allow Key Register (COMPREGKEY) Layout

COMPREGKEY (COMP Register Write-Allow Key Register) Offset: 0x3FC Default: 0x1ACCE551 Access: COMP -> COMPREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 14-127: COMP Register Write-Allow Key Register (COMPREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected COMP registers

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15 Buffered 10-bit DAC

15.1 Buffered DAC overview

The buffered DAC module consists of six internal 10-bit DAC and two analog output buffers that are capable of driving external load. The buffered DAC is a general purpose DAC that can be configured to generate a DC voltage and AC waveforms such as triangle, square waves and so forth. Each DAC output is divided from AVDD pin with 10-bit resolution, shown as following equation:

$$\mathrm{VOUT} = \frac{AVDD}{2^{10}} * CODE \quad (Typically, AVDD = 3.3V)$$

15.2 Buffered DAC architecture

The block diagram for the buffered DAC is shown in Figure 15-1.

Buffered DAC module has two sets of DAC code registers: CODE and CODEA. CODEA is a read-only register that directly control the buffered DAC value, and CODE is a writable shadow register that loads into CODEA either immediately or synchronized with the next PWMSYNC event, depends on the DACxCTL.CODELOAD setting. If DACxCTL.CODELOAD=0, it's in shadow mode, the value written to CODE register will load to CODEA register on next PWMSYNC signal. And if DACxCTL.CODELOAD=1, it's in direct mode, the value written to CODE register will load into CODEA register immediately, then 10-bit DAC output will also change immediately.

The high and low thresholds of the comparator are generated by two DACs, selected from the Table 14-1.

SPC2168 implements two internal DAC buffers, each DAC's output can be sent to the DAC buffer depending on the DAC buffer MUX setting (DACBUFCTL.INSEL), shown as Table 15-1.

Table 15-1: DAC buffer MUX

DACBUF0CTL.INSEL	DAC buffer 0 output	DACBUF1CTL.INSEL	DAC buffer 1 output
0	DAC0	0	DAC0
1	DAC1	1	DAC1
2	DAC2	2	DAC4
3	DAC3	3	DAC5

DAC buffer output can be directly sent to the ADC through ADC input MUX (shown in Table 12-4). The output of DAC buffer can also be sent out to the ADC10 pin or ADC13 pin, depends on the setting DACBUF0CTL.OE and DACBUF1CTL.OE.

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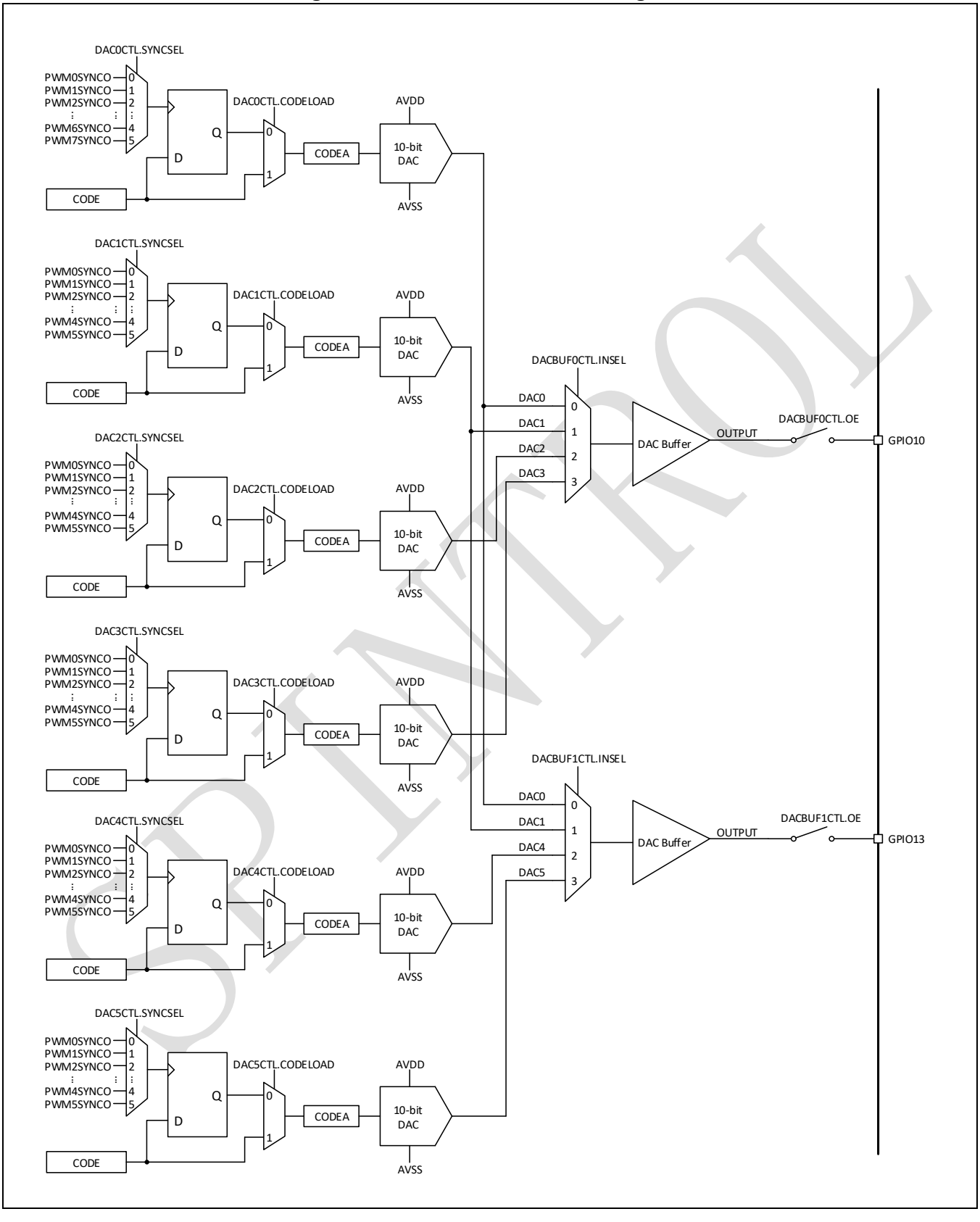
Figure 15-1: Buffered DAC block diagram



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Example 15.2.1 DAC and DAC buffer configuration

Set DAC0 output to 1.65V, (AVDD=3.3V), send it to DAC buffer and use ADC to measure, also send it to ADC10 pin.

- Enable DAC0, set DAC0 output to 1.65V
- Enable DAC buffer, select DAC0 as input
- Set ADC input MUX, select DAC buffer as input
- Send DAC buffer output to ADC10 pin

Example 15.2.1

```
Void COMP_Example15_2_1(void)
{
COMP->DAC0CODE.all=512;/* Set DAC0 output to 1.65V */
COMP->DAC0CTL.bit.CODELOAD=1;/* direct mode, dac code immediately update */
COMP->DAC0CTL.bit.EN=1;/* Enable DAC0 */
COMP->DACBUF0CTL.bit.INSEL=0;/* Send DAC0 to DAC buffer input */
ADC->ADCBGCTL.bit.EN=1;/* Enable ADC Bandgap */
COMP->DACBUF0CTL.bit.EN=1;/* Enable DAC buffer */
ADC->ADCSOCCTL[0].bit.SHEN=2;/* Enable Sampler B */
ADC->ADCSOCCTL[0].bit.CHSELP=3;/* Sampler B Positive =    DAC Buffer 0 */
ADC->ADCSOCCTL[0].bit.CHSELN=0;/* Sampler B Negative =    GND */
COMP->DACBUF0CTL.bit.OE=1;/* Send DAC buffer output to ADC10 pin */
}
```

15.3 Ramp generator

The ramp generator can produce a falling ramp reference (REFP voltage) for the too high compactor, see Figure 14-1. Only DAC0 and DAC1 have ramp capability.

Figure 15-2 shows ramp generator diagram. There's two sets of registers for ramp, one is read-only active registers, named RAMPDLYA, RAMPDECA, and RAMPMAXA, which can directly control ramp function. The other is a set of writable shadow registers called RAMPDLY, RAMPDEC, and RAMPMAX. Those shadow registers will load to read-only registers only under certain conditions, for example rising edge of RAMPEN or PWMSYNC, as shown in Figure 15-2.

The most significant 10bits of RAMPCNT will be sent to register CODEA, which controls 10-bit DAC output. RAMPMAXA is initial DAC value, RAMPDLYA is delay counter. For every PWMCLK cycle, RAMPDLYA will decrease one until it reaches zero. RAMPDECA controls DAC decrease step, for each time RAMPDLAYA is zero RAMPCNT value will subtract RAMPDECA.

When ramp generator is enabled (RAMPEN=1), RAMPCNT register will first load from RAMPMAX, and the register remains stable until the PWMSYNC is triggered. Then for every PWMCLK cycle, RAMPDLYA will decrease one. When RAMPDLYA reaches 0, RAMPCNT value will subtract RAMPDECA. Afterwards RAMPDLYA will load initial value for the next PWMCLK cycle and repeat. Therefore, DAC output will decrease RAMPDECA step for each (RAMPDLYA+1) PWMCLK cycles.

When RAMPLOAD=0, ramp generator block is in shadow mode. This means that while COMPxH is asserted, RAMPMAX value will not load to RAMPMAXA immediately. RAMPCNT will be controlled by the previous RAMPMAXA value, and updated RAMPMAX value will load to RAMPMAXA only at the next PWMSYNC rising edge. If RAMPLOAD=1, ramp generator block is in direct mode, which means that when COMPxH is asserted, RAMPMAX value will directly load to RAMPMAXA and control RAMPCNT.

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Figure 15-2: Ramp generator diagram

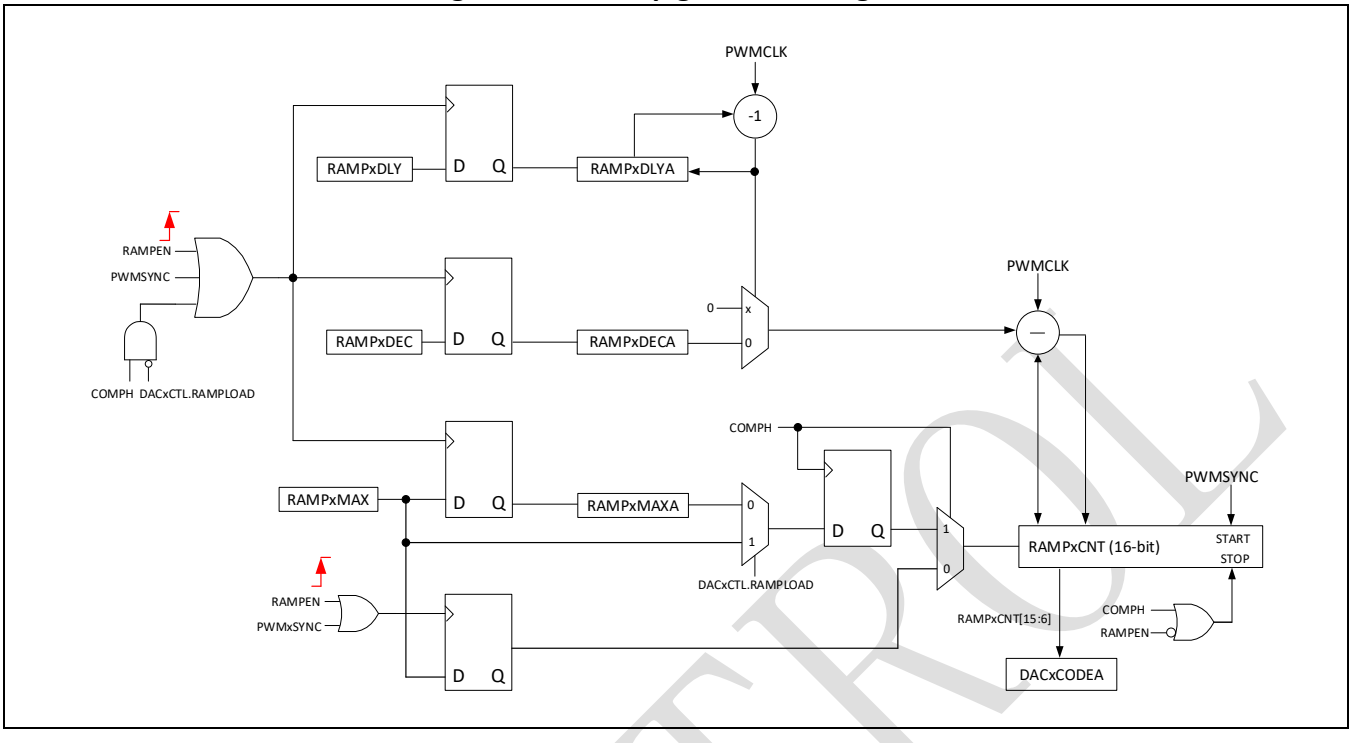
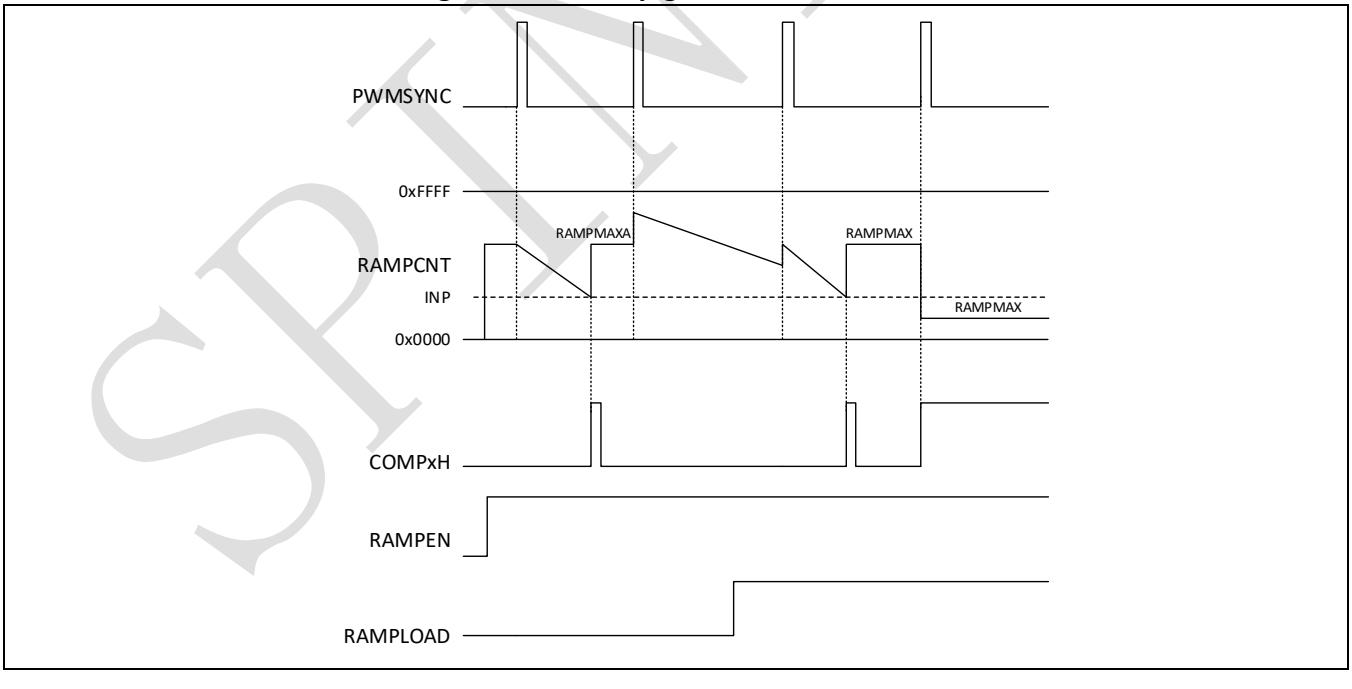


Figure 15-3 shows an example for DAC output (same as RAMPCNT) during PWMSYNC triggered and COMPxH asserted. Suppose the positive input to the too high comparator is fixed (INP in Figure 15-3).

Figure 15-3: Ramp generator waveform



15.4 Power-up sequence

When powering up the DAC or DAC buffer, the following sequence must be used:

Step 1: Power up ADC bandgap

Step 2: Power up the analog circuits of DAC or DAC buffer

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15.5 Registers

Please see Section 14.5 for DAC related register map and definitions.

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16 Temperature sensor

16.1 T-sensor overview

The SPC2168 implements an internal temperature sensor to measure the junction temperature of the device. The sensor output can be sampled with the ADC on Sampler C, which was shown in Figure 12-1.

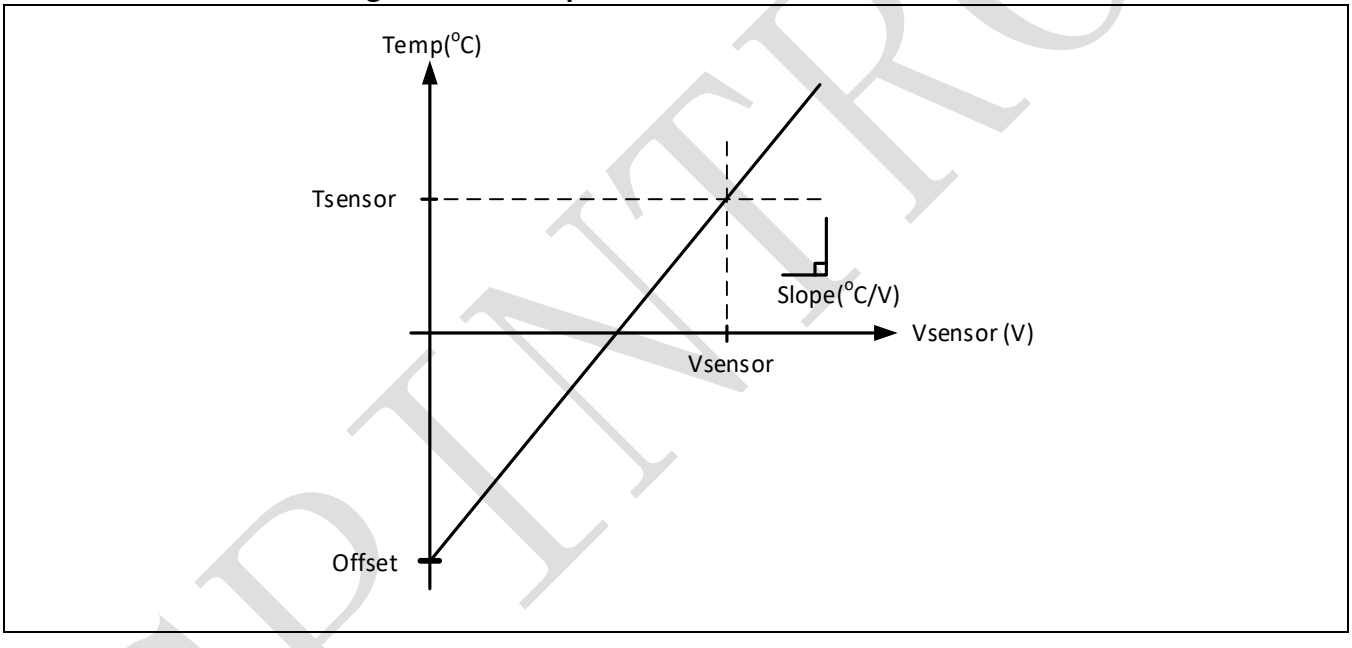
16.2 Transfer function

The temperature sensor output and the resulting ADC values increase with increasing junction temperature. As shown in Figure 16-1, the transfer function of the sensor is defined as:

$$\text{Temperature} = \text{Slope} \times \text{Vsensor} + \text{Offset}$$

Where Slope = 4238.97 °C/V, Offset = -283.36 °C.

Figure 16-1: Temperature sensor transfer function



So the measure temperature step is shown below:

Step 1. In target temperature T, measure the sensor output as Vsensor. The Vsensor should be calibrated using ADC gain and offset trim value.

Step 2. Using the above formula to calculate the target temperature.

Note: One ADC code is cooresponding 1.9°C. ADC sampling time should be 2us at least to meet the settling requirement of temperature sensor. SPC2168 support the function named ADC_CalculateTemperature in SDK to get the temperature directly.

SPINTROL

16.3 Power-up sequence

When powering up the T-sensor, the following sequence must be used:

Step 1: Power up ADC bandgap

Step 2: After 200us, power up ADC reference buffer

Step 3: After 200us, power up the analog circuits of ADC

16.4 Precision improvement

The accurary of temperature sensor will be degraded by inherent mismatch from internal device. Because this temperature sensor is always used for over-temperature protection that didn't need high precision case, the temperature sensor is not factory trimmed.

However, SPC2168 support to use dynamic element matching (DEM) to correct this mismatch and get the better accuary for tempearature sensor. Customer can call the function named ADC_CalculateTemperature in SDK.

16.5 Registers

Please see Table 12-356 and Table 12-357 for T-sensor related register definitions.

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17 UART

17.1 UART overview

The SPC2168 implements one Universal Asynchronous Receiver/Transmitter (UART) port. The port contains a UART and a slow serial infrared Transmit encoder and Receive decoder that conform to the IrDA serial infrared specification.

The UART port performs serial-to-parallel conversion on data characters received from a peripheral device and parallel-to-serial conversion on data characters received from CPU.

The CPU can read a complete UART status for the Line Status Register. Status information includes the type and condition of transfer operations and error conditions (parity, overrun, framing or break interrupt) associated with UART.

The UART port operates in either FIFO or non-FIFO mode. In FIFO mode, a 64-byte Transmit FIFO holds data from the CPU until it is transmitted on the serial link; a 64-byte Receive FIFO buffers data from the serial link until it is read by the CPU. In non-FIFO mode, the Transmit and Receive FIFOs are bypassed, and the Transmit Holding Register and Receive buffer Register are used instead.

The UART includes a programmable baud-rate generator that can divide the input clock by 1 to (2^{16}-1), which produces a 16X clock that can be used to drive the internal transmit and receive logic. Software can program interrupts to meet its requirements, which minimizes the number of computations required to handle the communications link. UART operates in an environment that is either controlled by software and can be polled or is interrupt driven.

The UART port supports baud rates of 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230K, 460K, 921K, 1.8M and 3.6M.

17.2 UART features

The UART has the following features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- Independently controlled transmit, receive, line status and data-set interrupts
- Programmable serial interface:
  - 5 – 8 data bits
  - Even, odd, or no parity detection
  - One, one-and-a-half, or two stop bits generation
  - Baud-rate generation up to 3.6 Mbps
  - False start-bit detection
- 64-byte Transmit FIFO
- 64-byte Receive FIFO
- Complete status-reporting capability
- Ability to generate and detect line breaks
- Internal diagnostic capabilities that include:

SPINTROL

- Loopback controls for communications link fault isolation
- Break, parity and framing-error simulation

- Fully prioritized interrupt system controls
- Serial Infrared asynchronous interface that conform to the Infrared Data Association(IrDA) specification

17.3 UART signal descriptions

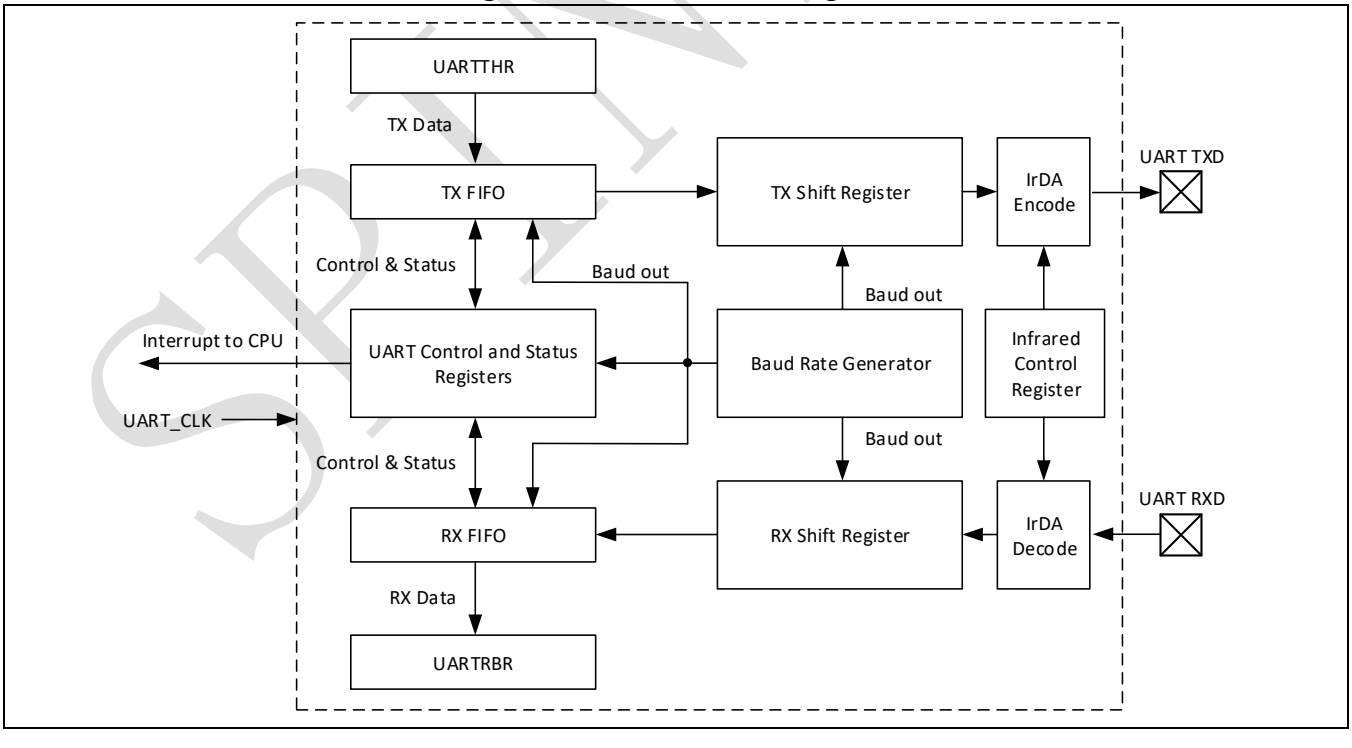
Table 17-1 lists and describes each external signal that is connected to a UART module. The pins transmit digital CMOS-level signals and are connected to through GPIOs. Please refer to the GPIO pin configuration registers for details.

Table 17-1: UART signal descriptions

Name	Type	Descriptions
RXD	Input	**Serial Input** Serial data input to the Receive Shift register; in Infrared mode, it is connected to the infrared receiver input
TXD	Output	**Serial Output** Serial data output to the communication-link peripheral or data set. The TXD signal is set to the logic 1 state upon a reset operation. It is connected to the output of the infrared transmitter in infrared mode.

The block diagram is shown in Figure 17-1.

Figure 17-1: UART block diagram



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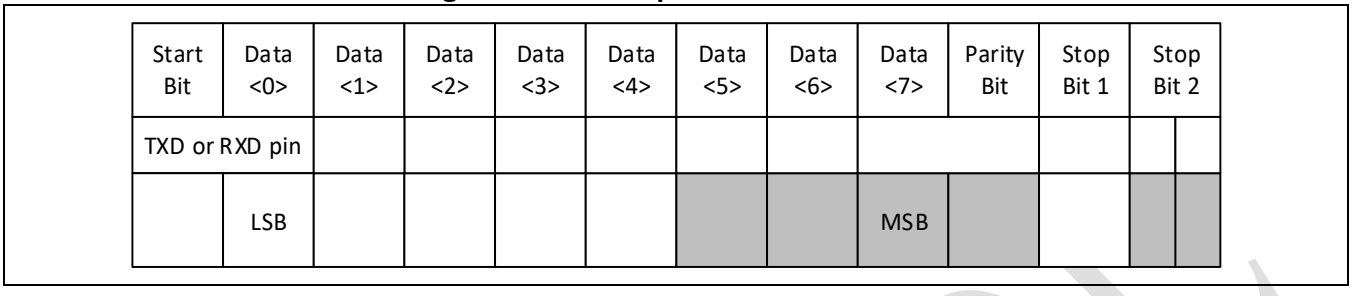
17.4 UART operation

Figure 17-2 shows the format of a UART data frame.

Figure 17-2: Example UART data frame



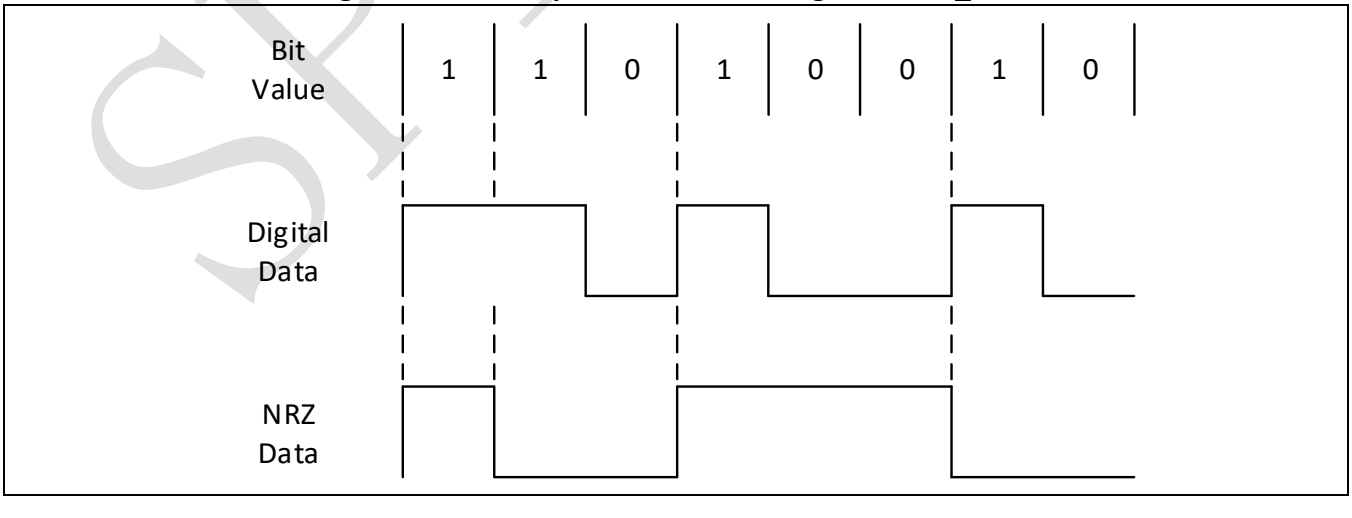
The receive-data sample-counter frequency is 16 times the value of the bit frequency. The 16X clock is created by the baud-rate generator. Each bit is sampled three times in the middle. Shaded bits in Figure 17-2 are optional and can be programmed by software.

Each data Frame is between 9 and 11 bits long, depending on the size of the data programmed, whether parity is enabled. A data frame begins by transmitting a start bit that is represented by a high to low transition. The start bit is followed by 8 bits of data that begin with the Least Significant bit (LSB). The data bits are followed by an optional parity bit. The parity bit is set if: even parity is enabled and the data byte has an odd number of ones or if odd parity is enabled and the data byte has an even number of ones. The data frame ends with 1 stop bit. The stop bit is represented by 1 successive bit period of logic one.

The UART module has two FIFOs: one Transmit and one Receive. The Transmit FIFO is 64 bytes deep and 8 bits wide. The Receive FIFO is 64 bytes deep and 11 bits wide. Three bits are used for tracking errors.

The UART can use NRZ coding to represent individual bit values. To enable NRZ coding, set the UARTIER.NRZME field in the Interrupt Enable Register. A bit value of 1 is represented by a line transition, and 0 is represented by no line transition. Figure 17-3 shows the data byte 0b0100_1011 in NRZ coding. The LSB in the byte is transmitted first.

Figure 17-3: Example NRZ bit Encoding – 0b0100_1011



SPINTROL

17.4.1 Reset

The UART is disabled on reset. To enable it, software must program the GPIO Pin Configuration registers, and then set the UARTIER.UUE field in the Interrupt Enable Register. When the UART is enabled, the receiver waits for a frame start bit and the transmitter sends data if it is available in the Transmit Holding Register. Transmit data can be written to the Transmit Holding Register before the UART unit is enabled. In FIFO mode, data is transmitted from the FIFO to the Transmit Holding Register before it goes to the pin.

When the UART unit is disabled, the transmitter or receiver finishes the current byte and stops transmitting or receiving more data. Data in the FIFO is not cleared and transmission resumes when the UART is enabled.

17.4.2 FIFO operation

The UART has a Transmit FIFO and a Receive FIFO, with each FIFO holding 64 characters of data. There is one method for moving data into and out of the FIFOs: Program I/O. In Program I/O mode, polling is used.

17.4.2.1 FIFO interrupt mode operation

The UARTMCR.OUT2 field in the Modem Control Register is a global UART interrupt enable bit and must be set to enable UART interrupts.

17.4.2.2 Receive interrupt

For a receive interrupt to occur, the Receive FIFO and receive interrupts must be enabled. The UARTIIR.IID field in the Interrupt Identification Register changes to show that receive data is available when the FIFO reaches its trigger threshold. The UARTIIR.IID field changes to show the next waiting interrupt when the FIFO drops below the trigger threshold. A change in the UARTIIR.IID field triggers an interrupt to the core. Software reads the UARTIIR.IID field to determine the cause of the interrupt.

The receive-line-status interrupt has the highest priority; the received-data-available interrupt is lower. The line-status interrupt occurs only when the character at the front of the FIFO has errors.

The UARTLSR.DR field in the Line Status Register is set when a character is transferred from the Shift register to the Receive FIFO. UARTLSR.DR is cleared when the FIFO is empty.

Note: If the receive interrupt is enabled but the Receive FIFO is not enabled, a receive interrupt occurs upon a receive data is available in the Receive Buffer Register (UARTRBR).

17.4.2.3 Character timeout interrupt

A character timeout interrupt occurs when the receive FIFO and receive timeout interrupt are enabled and all of the following conditions exist:

- At least one character is in the FIFO.
- The most recently received character was received more than four continuous character times ago.
- The most recent FIFO read was performed more than four continuous character times ago.

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After the reads one character from the Receive FIFO or a new start bit is received, the timeout interrupt is cleared, and the timeout is reset. If a timeout interrupt has not occurred, the timeout is reset when a new character is received or the reads the Receive FIFO.

17.4.2.4 Transmit interrupt

Transmit interrupts can occur only when the Transmit FIFO and transmit interrupt are enabled. When the FIFO is closed, writing the THR register once generates a new transmit interrupt. The transmit data-request interrupt occurs when the Transmit FIFO is at least half empty. The interrupt is cleared when the Transmit Holding Register is written or the Interrupt Identification Register is read.

17.4.2.5 Removing trailing bytes

The CPU must remove trailing bytes. The presence of trailing bytes is signaled by the assertion of a character timeout interrupt. When servicing a character timeout interrupt, the CPU uses the following procedure:

1. Read the Line Status Register and check for errors.
2. Disable the receiver timeout interrupt via UARTIER.RTOIE field in the Interrupt Enable Register.
3. Read data from the UART FIFO.
4. Read the Line Status Register, check for errors, and loop back to step 3. If the UARTLSR.DR field is set, go to step 5.
5. No more data in FIFO: Re-enable RTO interrupt via the UARTIER.RTOIE field in the Interrupt Enable Register.
6. Done.

17.4.2.6 FIFO polled mode operation

When the FIFOs are enabled, clearing the bits [4:0] in the Interrupt Enable Register places the port in FIFO polled operating mode. The receiver and the transmitter are controlled separately. Either one or both can be in polled mode. In polled mode, software checks receiver and transmitter status via the Line Status Register. The CPU polls the following bits for receive and transmit data service:

- Receive Data Service – the CPU checks the UARTLSR.DR field, which is set when one or more bytes remain in the Receive FIFO or Receive Buffer Register.
- Transmit Data Service – the CPU checks the UARTLSR.TDRQ field in the Line Status Register, which is set when the transmitter needs data.

The CPU can also check the UARTLSR.TXDONE field in the Line Status Register, which is set when the Transmit FIFO is empty.

SPINTROL

17.4.3 Auto-baud-rate detection

The UART supports auto-baud-rate detection. When enabled, the UART counts the numbers of clock cycles within the start-bit pulse. This number is then written into the Auto-Baud Count Register and is used to calculate the baud rate. When the Auto-Baud Count Register is written, an auto-baud-lock interrupt is generated (if enabled), and the UART automatically programs the Divisor Latch Registers with the appropriate baud rate. If preferred, the CPU can read the Auto-Baud Count Register and use this information to program the Divisor Latch Low Byte Register and Divisor Latch High Byte Register with a baud rate calculated by the CPU. After the baud rate has been programmed, the CPU verifies that the predetermined characters (usually AT or at) are being received correctly.

If the UART is to program the Divisor Latch Registers, software can use the formula-based method for auto-baud calculation. The baud rates that are seen in most commercial electronics, which are referred to as “common”. Any baud rate shown in Table 17-2 can be programmed by the UART. This method works well for higher baud rates, but it could fail below 28.8 kbps if the remote transmitter’s actual baud rate differs by more than one percent of its target.

When the baud rate is detected, the auto-baud circuitry disables itself by clearing the UARTACR.CNTVAL field in the Auto-Baud Count Register. To re-enable auto-baud detection, set the UARTABR.ABE field again.

Note: 1. Changing the baud rate is not permitted when actively transmitting or receiving data. Auto-baud-rate detection is not supported in IrDA (serial infrared) mode.
2. Only after the UART configuration is completed and enabled can the automatic baud rate function be configured.

17.4.4 Programmable baud-rate generator

The UART contains a programmable baud-rate generator that can take a fixed-input clock and divide it down to generate the preferred baud rate. The baud rate is calculated by taking the UART peripheral clock.

The baud-rate generator output frequency is 16 times the baud rate. Two 8-bit Divisor Latch Registers (Divisor Latch Low Register and Divisor Latch High Register) store the divisor in a 16-bit binary format. Load these divisor latches during initialization to ensure that the baud-rate generator operates properly. The 16X clock stops if each Divisor Latch register is loaded with 0x0. The baud rate of the data shifted into or out of a UART is given by the formula:

$$\text{BaudRate} = \frac{UART_CLK}{16 \times Divisor}$$

For example: if the Divisor is 24 and UART clock is 24 MHz, the baud rate is 62500 bps.

Note: Changing the baud rate is not permitted when actively transmitting or receiving data.

Refer to Table 17-2 for a list of recommended baud rates based on divisor values (Divisor Latch High Byte Register: Divisor Latch Low Byte Register).

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The divisor reset value is 0x0002. Changing the baud rate (writing to registers Divisor Latch Low Byte Register and Divisor Latch High Byte Register) is not permitted while actively transmitting or receiving data.

Table 17-2: Recommended baud rates

Required Baud Rate (bps)
9600
19200
38400
57600
115200
230400
460800
921600
1842000
3686400

17.4.5 Serial infrared asynchronous interface

The Slow Serial Infrared (SIR) interface is used with the UART to support two-way wireless communication that uses infrared transmission. The SIR interface provides a Transmit encoder and Receive decoder to support a physical link that conforms to the lrDA Serial Infrared Specification.

The SIR interface does not contain the actual IR LED driver or the receive amplifier. The I/O pins attached to the SIR interface have only digital CMOS-level signals. SIR supports two-way communication, but full-duplex communication is not possible because reflections from the transmit LED enter the receiver. SIR supports frequencies up to 115.2 kbps.

Note: This SIR interface should be turned on and off only while the UART module is completely idle and disabled. On-the-fly changes are likely to produce problems and are not recommended.

The SIR modulation technique works with 7- or 8- bit characters with an optional parity bit. The data is preceded by a zero-value start bit and ends with one stop bit. The encoding scheme sends a 1.6-us pulse 3/16 of a bit wide in the middle of every zero-value bit and sends no pulses for bits with a value of one. The pulse for each zero-value bit must occur, even for consecutive bits with no edge between them. Figure 17-4 shows an example of Transmit and Receive operation.

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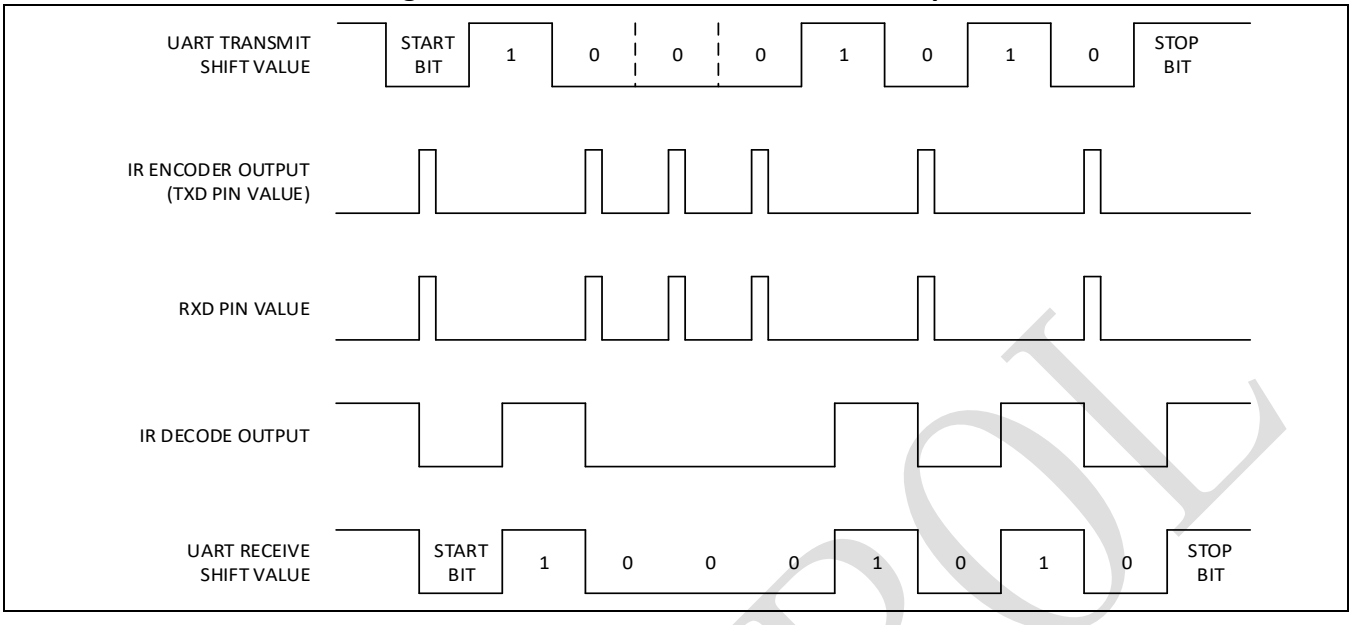
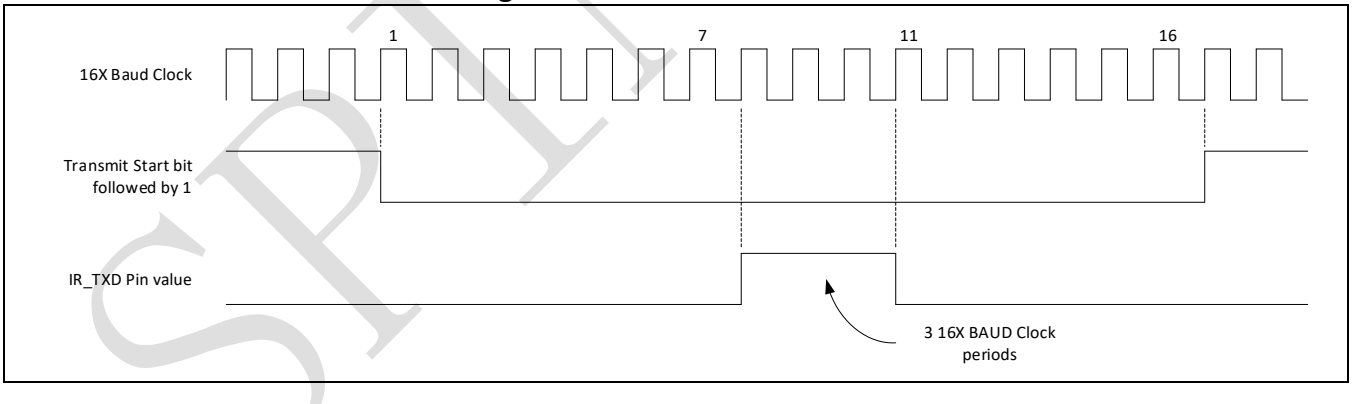
Figure 17-4: IR transmit and receive example



The top line in Figure 17-4 shows an asynchronous transmission as it is sent from the UART. The second line shows the pulses generated by the IR encoder at the TXD pin. A 1.6us pulse is generated in the middle of the START bit and any data bit that is a zero. The third line shows the values received at the RXD input pin. The fourth line shows the receive-decoder output. The Receive decoder drives the receive data line low when it detects a pulse. The bottom line shows how the UART receiver interrupts the decoder action. This last line is the same as the first, but it is shifted half a bit period.

Each zero bit has a pulse width of 3/16 of a bit time, shown in Figure 17-5.

Figure 17-5: Pulse of a zero bit



To prevent transmitter LED reflection feedback to the receiver, disable the IR Receive decoder when the IR Transmit encoder transmits data, and disable the IR Transmit encoder Receive decoder when the IR Receive decoder receives data. RCVEIR and XMITIR must not be set at the same time.

Note: This restriction specifically is to ensure no feedback; no filtering is performed to remove this feedback data.

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17.5 Registers

17.5.1 UART register map

Table 17-3: UART Module Base Address

Peripheral Module	Base Address
UART	0x4000 4000

Table 17-4: UART Register Map

Register	Offset	Description	Reset Value
UARTRBR	0x00	UART Receive Buffer Register	0x00000000
UARTTHR	0x00	UART Transmit Holding Register	0x00000000
UARTDLL	0x00	UART Divisor Latch Low Byte Register	0x00000002
UARTDLH	0x04	UART Divisor Latch High Byte Register	0x00000000
UARTIER	0x04	UART Interrupt Enable Register	0x00000000
UARTIIR	0x08	UART Interrupt Identification Register	0x00000001
UARTFCR	0x08	UART FIFO Control Register	0x00000000
UARTLCR	0x0C	UART Line Control Register	0x00000000
UARTMCR	0x10	UART Modem Control Register	0x00000000
UARTLSR	0x14	UART Line Status Register	0x00000060
UARTISR	0x20	UART Infrared Selection Register	0x00000000
UARTFOR	0x24	UART Receive FIFO Occupancy Register	0x00000000
UARTABR	0x28	UART Auto-Baud Control Register	0x00000000
UARTACR	0x2C	UART Auto-Baud Count Register	0x00000000

SPINTROL

17.5.2 UART registers

17.5.2.1 UART Receive Buffer Register (UARTRBR)

Table 17-5: UART Receive Buffer Register (UARTRBR) Layout

UARTRBR (UART Receive Buffer Register) Offset: 0x0 Default: 0x00000000 Access: UART -> UARTRBR.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 17-6: UART Receive Buffer Register (UARTRBR) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	In non-FIFO mode, this register holds the characters received by the UART Receive Shift Register. If this register is configured to use fewer than eight bits, the bits are right-justified and the most significant bits (MSB) are zeroed. Reading the register empties the register and clears the <Data Ready> field in the Line Status Register. UARTRBR latches the value of the data byte at the front of the FIFO in FIFO mode.

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17.5.2.2 UART Transmit Holding Register (UARTTHR)

Table 17-7: UART Transmit Holding Register (UARTTHR) Layout

UARTTHR (UART Transmit Holding Register) Offset: 0x0 Default: 0x00000000 Access: UART -> UARTTHR.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 17-8: UART Transmit Holding Register (UARTTHR) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	WO	0x0	This register holds the data byte to be transmitted next in non-FIFO mode. When the Transmit Shift Register (TSR) is emptied, the contents of this register are loaded into the Transmit Shift Register and the <Transmit Data Request> field in the Line Status Register is set. A write to Transmit Holding Register puts data into the top of the FIFO in FIFO mode. The data at the front of the FIFO is loaded into the TSR when the TSR is empty.

17.5.2.3 UART Divisor Latch Low Byte Register (UARTDLL)

Table 17-9: UART Divisor Latch Low Byte Register (UARTDLL) Layout

UARTDLL (UART Divisor Latch Low Byte Register) Offset: 0x0 Default: 0x00000002 Access: UART -> UARTDLL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
VAL							

Table 17-10: UART Divisor Latch Low Byte Register (UARTDLL) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:0	VAL	RW	0x2	Low-byte compare value to generate baud rate

SPINTROL

17.5.2.4 UART Divisor Latch High Byte Register (UARTDLH)

Table 17-11: UART Divisor Latch High Byte Register (UARTDLH) Layout

UARTDLH (UART Divisor Latch High Byte Register) Offset: 0x4 Default: 0x00000000 Access: UART -> UARTDLH.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
VAL							

Table 17-12: UART Divisor Latch High Byte Register (UARTDLH) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:0	VAL	RW	0x0	High-byte compare value to generate baud rate

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17.5.2.5 UART Interrupt Enable Register (UARTIER)

Table 17-13: UART Interrupt Enable Register (UARTIER) Layout

UARTIER (UART Interrupt Enable Register) Offset: 0x4 Default: 0x00000000 Access: UART -> UARTIER.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7 DMAE	6 UUE	5 NRZME	4 RTOIE	3 RESERVED	2 RLSE	1 TIE	0 RAVIE

Table 17-14: UART Interrupt Enable Register (UARTIER) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	DMAE	RW	0x0	UART DMA Enable 0: Disable UART DMA 1: Enable UART DMA
6	UUE	RW	0x0	UART Unit Enable 0: The unit is disabled 1: The unit is enabled
5	NRZME	RW	0x0	NRZM Coding Enable NRZM encoding/decoding is used only in UART mode, not in Infrared mode. If the serial infrared receiver or transmitter is enabled, NRZM coding is disabled. 0: NRZM coding is disabled. General NRZ level coding is used so signal is low at 0 and high at 1. 1: NRZM coding is enabled. Signal keeps unchanged at 0 and toggles at 1.
4	RTOIE	RW	0x0	Receiver Time-out Interrupt Enable (Source UARTIIR.TOD) 0: Receiver data time-out interrupt disabled 1: Receiver data time-out interrupt enabled
3	RESERVED_3	RW	0x0	Reserved
2	RLSE	RW	0x0	Receiver Line Status Interrupt Enable (Source UARTIIR.IID) 0: Receiver line status interrupt disabled 1: Receiver line status interrupt enabled

SPINTROL

Bits	Field Name	Type	Reset	Description
1	TIE	RW	0x0	Transmit Data Request Interrupt Enable (Source UARTIIR.IID) 0: Transmit FIFO data request interrupt disabled 1: Transmit FIFO data request interrupt enabled
0	RAVIE	RW	0x0	Receiver Data Available Interrupt Enable (Source UARTIIR.IID) 0: Receiver data available (trigger threshold reached) interrupt disable 1: Receiver data available (trigger threshold reached) interrupt enabled

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17.5.2.6 UART Interrupt Identification Register (UARTIIR)

Table 17-15: UART Interrupt Identification Register (UARTIIR) Layout

UARTIIR (UART Interrupt Identification Register) Offset: 0x8 Default: 0x00000001 Access: UART -> UARTIIR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
FIFOSTS		EOC	ABL	TOD	IID		NIP

Table 17-16: UART Interrupt Identification Register (UARTIIR) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:6	FIFOSTS	RO	0x0	FIFO Mode Enable Status 00: Non-FIFO mode is selected 01: Reserved 10: Reserved 11: FIFO mode is selected
5	EOC	RO	0x0	DMA End of Descriptor Chain 00: UART DMA is still pending 01: UART DMA finished
4	ABL	RO	0x0	Auto-baud Lock 0: Auto-baud circuitry has not programmed Divisor Latch registers (DLR) 1: Divisor Latch registers (DLR) programmed by auto-baud circuitry
3	TOD	RO	0x0	Time Out Detected 0: No time out interrupt is pending 1: Time out interrupt is pending (FIFO mode only)
2:1	IID	RO	0x0	Interrupt Source Encoded 00: Invalid option 01: Transmit requests data 10: Received data available 11: Receive error (Overflow, parity, framing, break, FIFO error)
0	NIP	RO	0x1	No Interrupt Pending 0: Interrupt is pending (active low) 1: No interrupt is pending

SPINTROL

17.5.2.7 UART FIFO Control Register (UARTFCR)

Table 17-17: UART FIFO Control Register (UARTFCR) Layout

UARTFCR (UART FIFO Control Register) Offset: 0x8 Default: 0x00000000 Access: UART -> UARTFCR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RXTH		BUS32	RESERVED	TXTH	CLRTF	CLRRF	TRFIFOE

Table 17-18: UART FIFO Control Register (UARTFCR) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:6	RXTH	WO	0x0	Receiver Interrupt Trigger Level (threshold) When the number of bytes in the Receive FIFO equals the threshold programmed into this field and the received-data-available interrupt is enabled via the UARTIER, an interrupt is generated and appropriate bits are set in the UARTIIR. 00: 1 byte or more in FIFO causes interrupt 01: 8 bytes or more in FIFO causes interrupt 10: 16 bytes or more in FIFO causes interrupt 11: 32 bytes or more in FIFO causes interrupt
5	BUS32	WO	0x0	Peripheral bus width 0: 8-bit peripheral 1: 32-bit peripheral
4	RESERVED_4	WO	0x0	Reserved
3	TXTH	WO	0x0	Transmitter Interrupt Trigger Level (threshold) 0: Interrupt request when FIFO is half empty 1: Interrupt request when FIFO is empty
2	CLRTF	W1C	0x0	Reset Transmit FIFO When set, all the bytes in the Transmit FIFO are cleared. The TDRQ bit in the UARTLSR is set and the UARTIIR shows a transmitter requests data interrupt, if the TIE bit in the UARTIER register is set. The Transmit Shift register is not cleared, and it completes the current transmission. 0: Write a 0 has no effect and always reads back 0

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Bits	Field Name	Type	Reset	Description
				1: Write a 1 clears the transmit FIFO This bit is self-cleared to 0
1	CLRRF	W1C	0x0	Reset Receive FIFO When set, all the bytes in the Receive FIFO are cleared. The DR bit in the UARTLSR is cleared to 0. All the error bits in the FIFO and the FIFOE bit in the UARTLSR are cleared. Any error bits, OE, PE, FE or BI, that has been set in UARTLSR are still set. The Receive Shift Register is not cleared. If the UARTIIR has been set to “received data available”, it is cleared. 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clears the transmit FIFO This bit is self-cleared to 0
0	TRFIFOE	WO	0x0	Transmit and Receive FIFO Enable TRFIFOE enable or disables the Transmit and Receive FIFOs. When TRFIFOE is set, both FIFOs are enabled (FIFO mode). When TRFIFOE is clear, the FIFOs are both disabled (non-FIFO mode). Writing 0b0 to this bit clears all bytes in both FIFOs. When changing from FIFO mode to non-FIFO mode and vice versa, data is cleared automatically from the FIFOs. This bit must be set when other bits in this register are written or the other bits are not programmed. 0: FIFOs are disabled 1: FIFOs are enabled

SPINTROL

17.5.2.8 UART Line Control Register (UARTLCR)

Table 17-19: UART Line Control Register (UARTLCR) Layout

UARTLCR (UART Line Control Register) Offset: 0xC Default: 0x00000000 Access: UART -> UARTLCR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
DLAB	SB	STKYP	EPS	PEN	STB	WLS	

Table 17-20: UART Line Control Register (UARTLCR) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	DLAB	RW	0x0	Divisor Latch Access Bit Must be set to access the Divisor Latch registers of the baud-rate generator during a Read or Write operation. Must be clear to access the Receive buffer, the Transmit Holding Register, or the UARTIER. 0: Access Transmit Holding Register, Receive Buffer Register, and Interrupt Enable Register 1: Access Divisor Latch registers (UARTDLL and UARTDLH)
6	SB	RW	0x0	Set Break Causes a break condition to be transmitted to the receiving UART. Acts only on the TXD pin and has no effect on the Transmit logic. In FIFO mode, wait until the transmitter is idle (UARTLSR.TXDONE=1) to set and clear SB. 0: No effect on TXD output 1: Forces TXD output to 0 (space)
5	STKYP	RW	0x0	Sticky Parity. This bit is ignored if PEN=0 0: No effect on parity bit 1: Forces parity bit to be opposite of EPS bit value
4	EPS	RW	0x0	Even Parity Select. This bit is ignored if PEN=0 0: Sends or checks for odd parity 1: Sends or checks for even parity
3	PEN	RW	0x0	Parity Enable 0: No parity bit 1: Enable parity bit

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Bits	Field Name	Type	Reset	Description
2	STB	RW	0x0	Stop bits 0: 1 stop bit 1: 1.5 stop bit for 5-bit character 2 stop bit for 6/7/8 bit character
1:0	WLS	RW	0x0	Word length select for each transferred character 00: 5-bit character 01: 6-bit character 10: 7-bit character 11: 8-bit character

17.5.2.9 UART Modem Control Register (UARTMCR)

Table 17-21: UART Modem Control Register (UARTMCR) Layout

UARTMCR (UART Modem Control Register) Offset: 0x10 Default: 0x00000000 Access: UART -> UARTMCR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		RESERVED	RESERVED	GIE	RESERVED	RESERVED	RESERVED

Table 17-22: UART Modem Control Register (UARTMCR) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	RESERVED_5	RW	0x0	Reserved
4	RESERVED_4	RW	0x0	Reserved
3	GIE	RW	0x0	Global interrupt enable 0: Disable UART interrupt to CPU 1: Enable UART interrupt to CPU
2:	RESERVED_2	RW	0x0	Reserved
1	RESERVED_1	RW	0x0	Reserved
0	RESERVED_0	RW	0x0	Reserved

SPINTROL

17.5.2.10 UART Line Status Register (UARTLSR)

Table 17-23: UART Line Status Register (UARTLSR) Layout

UARTLSR (UART Line Status Register) Offset: 0x14 Default: 0x00000060 Access: UART -> UARTLSR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7 FIFOERR	6 TXDONE	5 TDRQ	4 BI	3 FE	2 PE	1 OE	0 DR

Table 17-24: UART Line Status Register (UARTLSR) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	FIFOERR	RO	0x0	FIFO Error Status This bit is always 0 in non-FIFO mode. In FIFO mode, FIFOERR is set when there is at least one parity error, framing error, or break indication for any of the characters in the FIFO. The CPU read of the UARTLSR does not reset this bit. FIFOERR is reset when all errorneous characters have been read from the FIFO. 0: No FIFO or no errors in receive FIFO 1: At least one character in receive FIFO has errors
6	TXDONE	RO	0x1	Transmit Done Set when the Transmit Holding Register and the Transmit Shift Register are both empty. It is cleared when either the Transmit Holding Register or the Transmit Shift Register contains a data character. In FIFO mode, TXDONE is set when the Transmit FIFO and the Transmit Shift Register are both empty. 0: There is data in the transmit shift register, the Transmit Holding Register, or the FIFO. 1: All the data in the transmitter has been shifted out
5	TDRQ	RO	0x1	Transmit Data Request Indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the transmit-data request interrupt enable is set. The TDRQ bit is set when a character is transferred from the Transmit Holding Register into the Transmit Shift Register. The bit is cleared with the loading of the Transmit Holding Register. In FIFO mode, TDRQ is set when half of the characters in the FIFO

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Bits	Field Name	Type	Reset	Description
				have been loaded into the Shift Register or the CLRTF bit in UARTFCR has been set. It is cleared when the FIFO has more than half data. If more than 64 characters are loaded into the FIFO, the excess characters are lost. 0: There is data in the holding register or FIFO waiting to be shifted out 1: The transmit FIFO has half or less than half data
4	BI	RO	0x0	Receive Break Interrupt BI is set when the received data input is held low for longer than a full-word transmission time (the total time of start bit + data bits + parity bit + stop bit). BI is cleared when the CPU reads the UARTLSR. In FIFO mode, only one character equal to 0x00, is loaded into the FIFO regardless of the length of the break condition. BI shows the break condition for the character at the front of the FIFO, not the most recently received character. 0: No break signal has been received 1: Break signal received
3	FE	RO	0x0	Receive Framing Error FE indicates that the received character did not have a valid stop bit. FE is set when the bit following the last data bit or parity bit is detected to be 0. FE is cleared when the CPU reads the LSR. The UART resynchronizes after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this start bit twice and then reads in the data. In FIFO mode, FE shows a framing error for the character at the front of the FIFO, not for the most recently received character. 0: No Framing error 1: Invalid stop bit has been detected
2	PE	RO	0x0	Receive Parity Error Indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. PE is set upon detection of a parity error and is cleared when the CPU reads the UARTLSR. In FIFO mode, PE shows a parity error for the character at the front of the FIFO, not the most recently received character. 0: No Parity Error 1: Parity error has occurred
1	OE	RO	0x0	Receive Overflow Error

SPINTROL

Bits	Field Name	Type	Reset	Description
				In non-FIFO mode, indicates that data in Receive Buffer register was not read by the CPU before the next character was received. The new character is lost. In FIFO mode, OE indicates that all 64 bytes of the FIFO are full and the most recently received byte has been discarded. OE is set upon detection of an overflow condition and cleared when the CPU reads the UARTLSR. 0: No data has been overflow 1: Receive data has been overflow
0	DR	RO	0x0	Receive Data Ready (i.e. Not Empty) Set when a complete incoming character has been received and transferred into the Receive Buffer Register or the FIFO. In non-FIFO mode, DR is cleared when the Receive buffer is read. In FIFO mode, DR is cleared if the FIFO is empty (last character has been read from UARTRBR) or the FIFO is reset with UARTFCR.CLRRF. 0: No data has been received 1: Data is available in UARTRBR or the FIFO

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17.5.2.11 UART Infrared Selection Register (UARTISR)

Table 17-25: UART Infrared Selection Register (UARTISR) Layout

UARTISR (UART Infrared Selection Register) Offset: 0x20 Default: 0x00000000 Access: UART -> UARTISR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			RXPL	TXPL	RESERVED	RCVEIR	XMITIR

Table 17-26: UART Infrared Selection Register (UARTISR) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4	RXPL	RW	0x0	Receive Data Polarity 0: SIR decoder takes positive pulses as zeros 1: SIR decoder takes negative pulses as zeros
3	TXPL	RW	0x0	Transmit Data Polarity 0: SIR encoder generates a positive pulse for a data bit of zero 1: SIR encoder generates a negative pulse for a data bit of zero
2	RESEVED_2	RW	0x0	Reserved
1	RCVEIR	RW	0x0	Receiver SIR Enable When RCVEIR is set, the signal from the RXD pin is processed by lrDA decoder before it is fed to the UART. IF RCVEIR is clear, than all clocking to the lrDA decoder is blocked and the RXD pin is fed directly to the UART. 0: Receiver is in UART mode 1: Receiver is in infrared mode
0	XMITIR	RW	0x0	Transmitter SIR Enable When XMITIR is set, the normal TXD output from the UART is processed by the lrDA encoder before it is fed to the device pin. If XMITIR is clear, all clocking to the lrDA encoder is blocked and the UART's TXD signal is connected directly to the device pin. 0: TXD signal is connected directly 1: TXD output from the UART is processed by the lrDA encoder

SPINTROL

17.5.2.12 UART Receive FIFO Occupancy Register (UARTFOR)

Table 17-27: UART Receive FIFO Occupancy Register (UARTFOR) Layout

UARTFOR (UART Receive FIFO Occupancy Register) Offset: 0x24 Default: 0x00000000 Access: UART -> UARTFOR.all							
31	30	29	28	27	26	25	24
RESERVED_31_7							
23	22	21	20	19	18	17	16
RESERVED_31_7							
15	14	13	12	11	10	9	8
RESERVED_31_7							
7	6	5	4	3	2	1	0
RESERVED_31_7	BYTECNT						

Table 17-28: UART Receive FIFO Occupancy Register (UARTFOR) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6:0	BYTECNT	RO	0x0	Number of bytes (0-64) remaining in the Receive FIFO

17.5.2.13 UART Auto-Baud Control Register (UARTABR)

Table 17-29: UART Auto-Baud Control Register (UARTABR) Layout

UARTABR (UART Auto-Baud Control Register) Offset: 0x28 Default: 0x00000000 Access: UART -> UARTABR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					ABUP	ABLIE	ABE

Table 17-30: UART Auto-Baud Control Register (UARTABR) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	ABUP	RW	0x0	Method to program Divisor Latch registers 0: Software Programs Divisor Latch registers 1: UART Programs Divisor Latch registers
1	ABLIE	RW	0x0	Auto-baud-lock interrupt enable (UARTIIR.ABL) 0: Auto-baud-lock interrupt disabled 1: Auto-baud-lock interrupt enabled
0	ABE	RW	0x0	Auto-baud detection enable 0: Auto-baud disabled 1: Auto-baud enabled

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17.5.2.14 UART Auto-Baud Count Register (UARTACR)

Table 17-31: UART Auto-Baud Count Register (UARTACR) Layout

UARTACR (UART Auto-Baud Count Register) Offset: 0x2C Default: 0x00000000 Access: UART -> UARTACR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
CNTVAL							
7	6	5	4	3	2	1	0
CNTVAL							

Table 17-32: UART Auto-Baud Count Register (UARTACR) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	CNTVAL	RO	0x0	Number of UART clock cycles within a start-bit pulse

SPINTROL

18 I2C

18.1 I2C overview

The SPC2168 implements a hardware I2C module, which provides an interface between a MCU and any I2C-bus-compatible device that connects via the I2C serial bus. The external components attached to the I2C bus can serially transmit/receive data to/from the MCU device through the two-wire I2C interface.

The I2C bus is multiple master bus and the I2C module supports the multi-master mode that allows more than one device capable of controlling the bus to be connected to it. Each I2C device is recognized by a unique address and can operate as either transmitter or receiver, according to the function of the device. In addition to being a transmitter or receiver, a device connected to the I2C bus can also be considered as master or slave when performing data transfers. Note that a master device is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. During this transfer, any device addressed by this master is considered a slave.

18.2 I2C features

The SPC2168 I2C module has the following features:

- Compliant with I2C specification version 2.1
- Supports three speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s) and High-Speed mode (3.4 Mb/s)
- Clock synchronization
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- Two independent transmit and receive FIFOs with 16 sample in depth and 32 bit in width

18.3 I2C signal description

Table 18-1: I2C signal description

Signal Name	Type	Descriptions
I2C_SCL	Input/Output	I2C serial clock line (open drain)
I2C_SDA	Input/Output	I2C serial data line (open drain)

18.4 I2C operation

The I2C module can be controlled via software to be either:

- An I2C master only, communicating with other I2C slaves; OR
- An I2C slave only, communicating with one more I2C masters.

The master is responsible for generating the clock and controlling the transfer of data. The slave is responsible for either transmitting or receiving data to/from the master. The acknowledgement of data is sent by the device that is receiving data, which can be either a master or a slave. As mentioned previously, the I2C protocol also allows multiple masters to reside on the I2C bus and uses an arbitration procedure to determine bus ownership.

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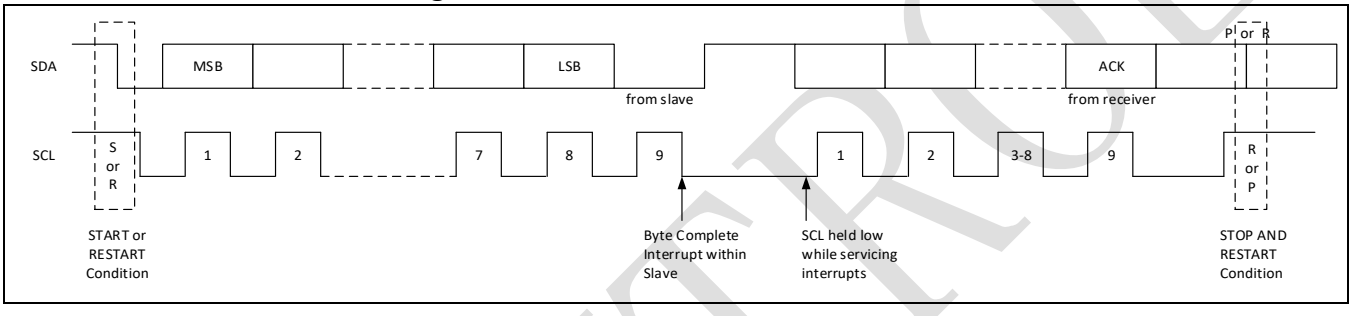
Each slave has a unique address that is determined by the system designer. When a master wants to communicate with a slave, the master transmits a START/RESTART condition that is then followed by the slave's address and a control bit (R/W) to determine if the master wants to transmit data or receive data from the slave. The slave then sends an acknowledge (ACK) pulse after the address.

If the master (master-transmitter) is writing to the slave (slave-receiver), the receiver gets one byte of data. This transaction continues until the master terminates the transmission with a STOP condition. If the master is reading from a slave (master-receiver), the slave transmits (slave-transmitter) a byte of data to the master, and the master then acknowledges the transaction with the ACK pulse. This transaction continues until the master terminates the transmission by not acknowledging (NACK) the transaction after the last byte is received, and then the master issues a STOP condition or addresses another slave after issuing a RESTART condition. This behavior is illustrated in Figure 18-1.

Figure 18-1: Data transfer on the I2C bus



The I2C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain or open-collector to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400 pF. Data is transmitted in byte packages.

Note: Putting data into the FIFO generates a START, and emptying the FIFO generates a STOP. For more information, refer to Section 18.4.1.

18.4.1 START and STOP generation

When operating as an I2C master, putting data into the Transmit FIFO causes the I2C to generate a START condition on the I2C bus. Allowing the Transmit FIFO to empty causes the I2C to generate a STOP condition on the I2C bus.

When operating as a slave, the I2C does not generate START and STOP conditions, as per the protocol. However, if a read request is made to the I2C, it holds the SCL line low until read data has been supplied to it. This action stalls the I2C bus until read data is provided by the slave I2C, or the I2C slave is disabled by writing a 0 to EN in register I2CENABLE.

18.4.2 Combined formats

The SPC2168 I2C module supports mixed read and write combined format transactions in both 7-bit and 10-bit addressing modes.

The I2C does not support mixed address combined format transactions, that is, a 7-bit address transaction followed by a 10-bit address transaction or vice versa.

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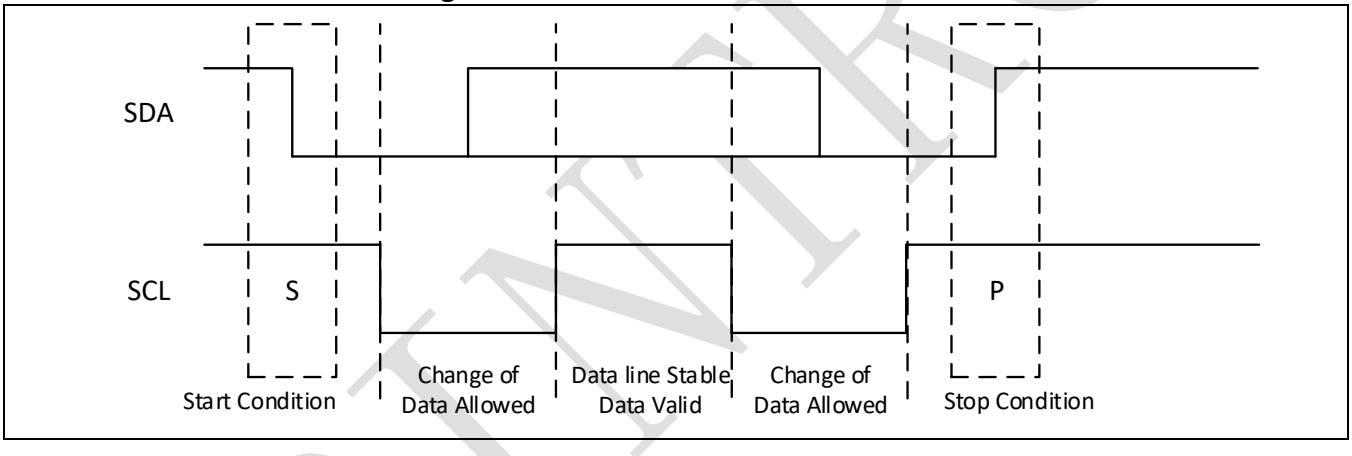
To initiate combined format transfers, set the register I2CCTL.RESTARTEN to 1. With this value set and operating as a master, when the I2C completes an I2C transfer, it checks the Transmit FIFO and executes the next transfer. If the direction of this transfer differs from the previous transfer, the combined format is used to issue the transfer. If the Transmit FIFO is empty when the current I2C transfer completes, a STOP is issued and the next transfer is issued following a START condition.

18.5 I2C protocols

18.5.1 START and STOP conditions

When the bus is idle, both the SCL and SDA signals are pulled high through external pull-up resistors on the bus. When the master wants to start a transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is 1. When the master must terminate the transmission, it issues a STOP condition, which is defined to be a low-to-high transition of the SDA line while SCL is 1. Figure 18-2 shows the timing of the START and STOP conditions. When data is being transmitted on the bus, the SDA line must be stable when SCL is 1.

Figure 18-2: START and STOP condition



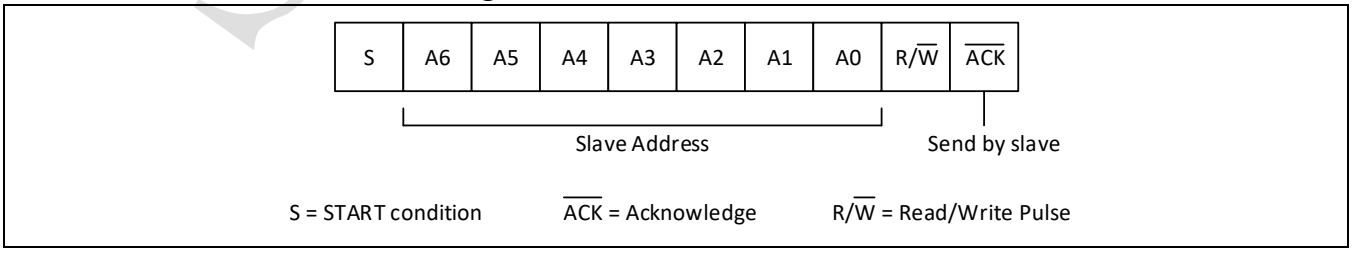
18.5.2 Address formats

The I2C module supports two address formats: the 7-bit and 10-bit address formats.

7-Bit Address Format

During the 7-bit address format, the first seven bits (bits 7:1) of the first byte set the slave address and the LSB bit (bit 0) is the R/W bit as shown in Figure 18-3. When bit 0 (R/W) is set to 0, the master writes to the slave. When bit 0 (R/W) is set to 1, the master reads from the slave.

Figure 18-3: 7-bit address format



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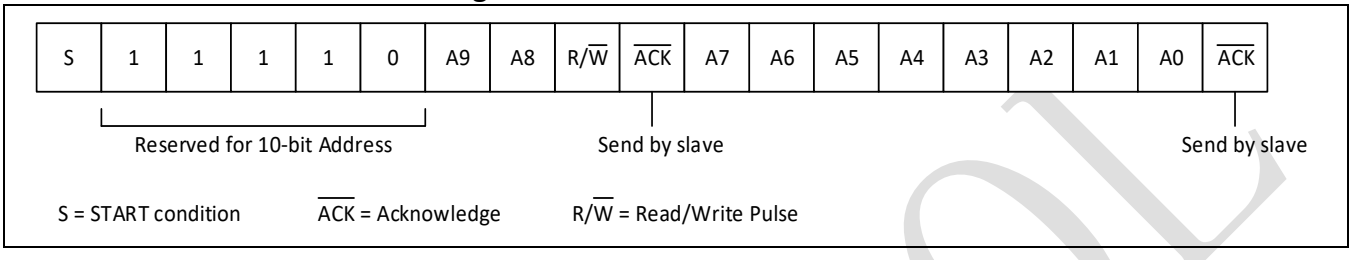
10-Bit Address Format

During 10-bit addressing, two bytes are transferred to set the 10-bit address. The transfer of the first byte contains the following bit definition. The first five bits (bits 7:3) notify the slaves that this is a 10-bit transfer followed by the next two bits (bits 2:1), which set the slaves address bits 9:8, and the LSB bit (bit 0) is the R/W bit. The second byte transferred sets bits 7:0 of the slave address. Figure 18-4 shows the 10-bit address format.

Figure 18-4: 10-bit address format



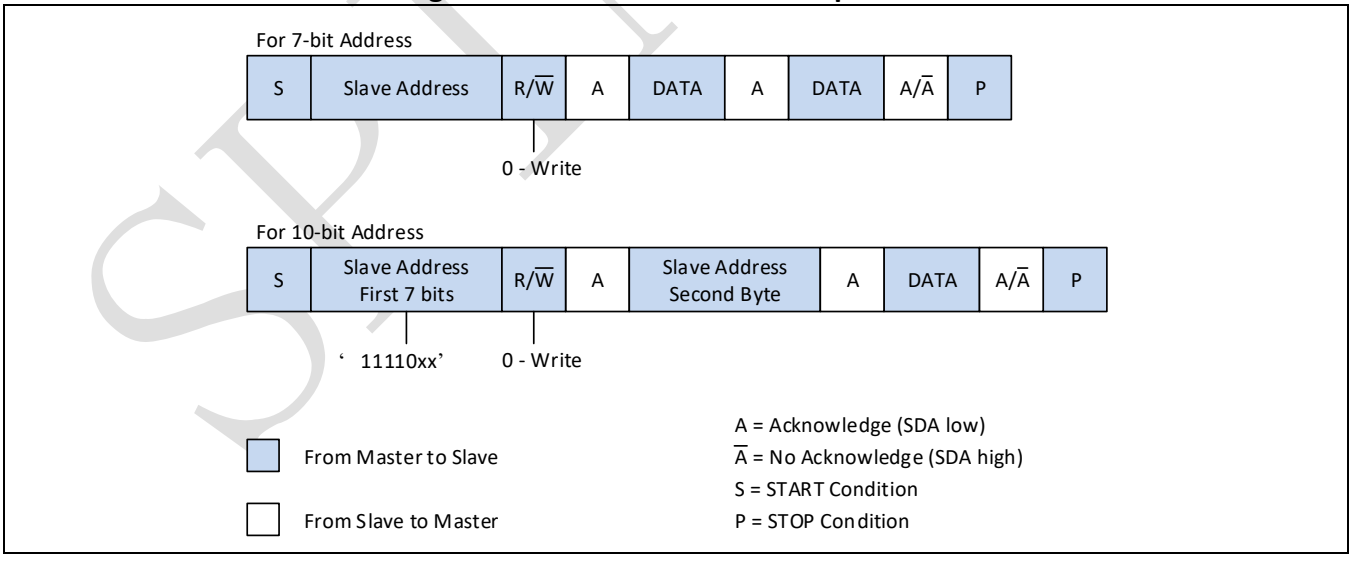
18.5.3 Transmitting and receiving protocol

The master can initiate data transmission and reception to/from the bus, acting as either a master-transmitter or master-receiver. A slave responds to requests from the master to either transmit data or receive data to/from the bus, acting as either a slave-transmitter or slave-receiver, respectively.

Master-Transmitter and Slave-Receiver

All data is transmitted in byte format, with no limit on the number of bytes transferred per data transaction. After the master sends the address and R/W bit or the master transmits a byte of data to the slave, the slave-receiver must respond with the acknowledge signal (ACK). When a slave-receiver does not respond with an ACK pulse, the master aborts the transfer by issuing a STOP condition. The slave must leave the SDA line high so that the master can abort the transfer.

Figure 18-5: Master-transmitter protocol



Master-Receiver and Slave-Transmitter

If the master is receiving data as shown in Figure 18-6, then the master responds to the slave-transmitter with an acknowledge pulse after a byte of data has been received, except for the last byte. This method is how the master-receiver notifies the slave-transmitter that this is the last byte. The slave-transmitter

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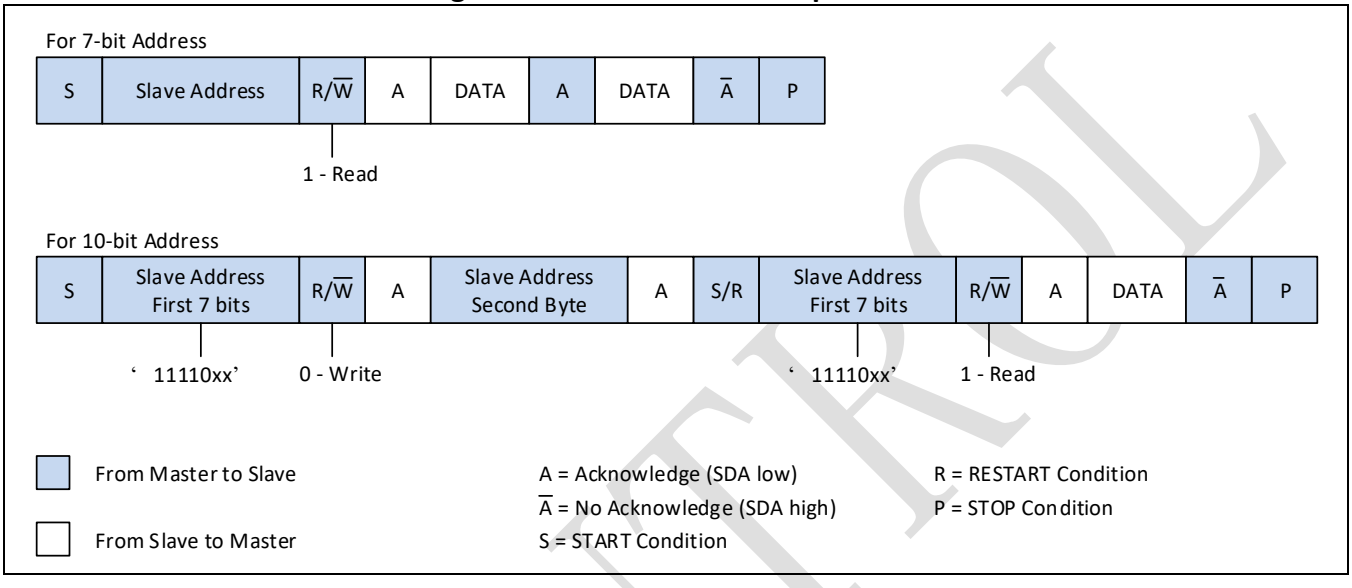
relinquishes the SDA line after detecting the No Acknowledge (NACK) so that the master can issue a STOP condition.

When a master refuses to relinquish the bus with a STOP condition, the master can issue a RESTART condition. This is identical to a START condition except it occurs after the ACK pulse. Operating in master mode, the I2C can then communicate with the same slave using a transfer of a different direction.

Figure 18-6: Master-receiver protocol



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18.6 Registers

18.6.1 I2C register map

Table 18-2: I2C Module Base Address

Peripheral Module	Base Address
I2C	0x4000 6000

Table 18-3: I2C Register Map

Register	Offset	Description	Reset Value
I2CCTL	0x00	I2C Control Register	0x0000007F
I2CMASTERADDR	0x04	I2C Master Address Register	0x00001055
I2CSLVADDR	0x08	I2C Slave Address Register	0x00000055
I2CHSMADDR	0x0C	I2C High Speed Master Mode Code Address Register	0x00000001
I2CDATACMD	0x10	I2C Data Buffer and Command Register	0x00000000
I2CSSHCNT	0x14	Standard Speed I2C Clock SCL High Count Register	0x000001F4
I2CSSLCNT	0x18	Standard Speed I2C Clock SCL Low Count Register	0x0000024C
I2CFSHCNT	0x1C	Fast Speed I2C Clock SCL High Count Register	0x0000004B
I2CFSLCNT	0x20	Fast Speed I2C Clock SCL Low Count Register	0x000000A3
I2CHSHCNT	0x24	High Speed I2C Clock SCL High Count Register	0x00000008
I2CHSLCNT	0x28	High Speed I2C Clock SCL Low Count Register	0x00000014
I2CIF	0x2C	I2C Interrupt Flag Register	0x00000000
I2CIE	0x30	I2C Interrupt Enable Register	0x000008FF
I2CRAWIF	0x34	I2C Raw Interrupt Flag Register	0x00000000
I2CRXTH	0x38	I2C Receive FIFO Threshold Register	0x00000000
I2CTXTH	0x3C	I2C Transmit FIFO Threshold Register	0x00000000
I2CINTCLR	0x40	Clear Combined and Individual Interrupt Register	0x00000000
I2CRXUDFCLR	0x44	Clear RXUDF Interrupt Register	0x00000000
I2CRXOVFCLR	0x48	Clear RXOVF Interrupt Register	0x00000000
I2CTXOVFCLR	0x4C	Clear TXOVF Interrupt Register	0x00000000
I2CRDREQCLR	0x50	Clear RDREQ Interrupt Register	0x00000000
I2CTXABRTCLR	0x54	Clear TXABRT Interrupt Register	0x00000000
I2CRXDONECLR	0x58	Clear RXDONE Interrupt Register	0x00000000
I2CACTCLR	0x5C	Clear ACT Interrupt Register	0x00000000
I2CSTOPDETCLR	0x60	Clear STOPDET Interrupt Register	0x00000000
I2CSTARTDETCLR	0x64	Clear STARTDET Interrupt Register	0x00000000
I2CGENCALLCLR	0x68	Clear GENCALL Interrupt Register	0x00000000
I2CENABLE	0x6C	I2C Enable Register	0x00000000
I2CSTS	0x70	I2C Status Register	0x00000006
I2CTFLVL	0x74	I2C Transmit FIFO Level Register	0x00000000
I2CRFLVL	0x78	I2C Receive FIFO Level Register	0x00000000
I2CSDAHOLD	0x7C	I2C SDA Hold-Time Register	0x00000001
I2CTXABRTSRC	0x80	I2C Transmit Abort Source Register	0x00000000

SPINTROL

Register	Offset	Description	Reset Value
I2CSDASETUP	0x94	I2C SDA Setup Register	0x00000064
I2CACKGC	0x98	I2C ACK General Call Register	0x00000001
I2CENSTS	0x9C	I2C Enable Status Register	0x00000000
I2CFSSPKLEN	0xA0	I2C Fast Speed Spike Suppresion Limit Register	0x00000006
I2CHSSPKLEN	0xA4	I2C High Speed Spike Suppresion Limit Register	0x00000002

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18.6.2 I2C registers

18.6.2.1 I2C Control Register (I2CCTL)

Table 18-4: I2C Control Register (I2CCTL) Layout

I2CCTL (I2C Control Register) Offset: 0x0 Default: 0x0000007F Access: I2C -> I2CCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	SLVDIS	RESTARTEN	ADDRSTS	SLVADDR10B	SPEED		MASTER

Table 18-5: I2C Control Register (I2CCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	SLVDIS	RW	0x1	Disable I2C slave NOTE: This bit should be the same as MASTER 0: Enable I2C slave 1: Disable I2C slave
5	RESTARTEN	RW	0x1	Determines whether RESTART conditions may be sent when acting as a master. Some older slaves do not support handling RESTART conditions; however, RESTART conditions are used in several I2C operations. When RESTART is disabled, the master is prohibited from performing the following functions: – Change direction within a transfer (split) – Send a START BYTE – High-speed mode operation – Combined format transfers in 7-bit addressing modes – Read operation with a 10-bit address – Send multiple bytes per transfer By replacing RESTART condition followed by a STOP and a subsequent START condition, split operations are broken down into multiple I2C transfers. If the above operations are performed, it will result in setting bit 6 (TXABRT) of the I2CRAWIF register. 0: Disable 1: Enable
4	ADDRSTS	RO	0x1	Read-only copy of I2CMASTERADDR[12]. 0: 7-bit addressing 1: 10-bit addressing

SPINTROL

Bits	Field Name	Type	Reset	Description
3	SLVADDR10B	RW	0x1	Addressing mode in slave mode. 0: 7-bit addressing. The I2C ignores transactions that involve 10-bit addressing; for 7-bit addressing, only the lower 7 bits of the I2CSLVADDR register are compared. 1: 10-bit addressing. The I2C responds to only 10-bit addressing transfers that match the full 10 bits of the I2CSLVADDR register.
2:1	SPEED	RW	0x3	I2C speed in master mode. 00: Invalid. Hardware will set it to 0x3 when write 0 01: Standard mode (100 kbit/s) 10: Fast mode (400 kbit/s) 11: High speed mode (3.4 Mbit/s)
0	MASTER	RW	0x1	Enable I2C master NOTE: This bit should be the same as SLVDIS 0: Disalbe I2C master 1: Enable I2C master

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18.6.2.2 I2C Master Address Register (I2CMASTERADDR)

Table 18-6: I2C Master Address Register (I2CMASTERADDR) Layout

I2CMASTERADDR (I2C Master Address Register) Offset: 0x4 Default: 0x00001055 Access: I2C -> I2CMASTERADDR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED			MASTERADDR10B	SPECIAL	GCORSTART	TARADDR	
7	6	5	4	3	2	1	0
TARADDR							

Table 18-7: I2C Master Address Register (I2CMASTERADDR) Field Description

Bits	Field Name	Type	Reset	Description
31:13	RESERVED_31_13	RO	0x0	Reserved
12	MASTERADDR10B	RW	0x1	Addressing mode in master mode 0: 7-bit addressing 1: 10-bit addressing
11	SPECIAL	RW	0x0	Special command enable 0: Disable special command and ignore GCORSTART bit 1: Enable special command as specified in GCORSTART bit
10	GCORSTART	RW	0x0	Special command select 0: General Call After issuing a General Call, only writes may be performed. Attempting to issue a read command results in setting bit 6 (TXABRT) of the I2CRAWIF register. The I2C remains in General Call mode until the SPECIAL bit is cleared 1: Start Byte
9:0	TARADDR	RW	0x55	Target address for any master transaction. These bits are ignored for issuing a General Call. To generate a START BYTE, the CPU needs to write only once into these bits. It should not be the same as I2CSLVADDR.

SPINTROL

18.6.2.3 I2C Slave Address Register (I2CSLVADDR)

Table 18-8: I2C Slave Address Register (I2CSLVADDR) Layout

I2CSLVADDR (I2C Slave Address Register) Offset: 0x8 Default: 0x00000055 Access: I2C -> I2CSLVADDR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						VAL	
7	6	5	4	3	2	1	0
VAL							

Table 18-9: I2C Slave Address Register (I2CSLVADDR) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9:0	VAL	RW	0x55	Slave address when I2C acts as a slave This register can be written only when the I2C interface is disabled (I2CENABLE=0). Writes at other times have no effect. Note: The default values cannot be any of the reserved address locations: that is, 0x00 to 0x07, or 0x78 to 0x7f. The correct operation of the device is not guaranteed if you program the I2CSLVADDR or I2CMASTERADDR to a reserved value.

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18.6.2.4 I2C High Speed Master Mode Code Register (I2CHSMADDR)

Table 18-10: I2C High Speed Master Mode Code Register (I2CHSMADDR) Layout

I2CHSMADDR (I2C High Speed Master Mode Code Address Register) Offset: 0xC Default: 0x00000001 Access: I2C -> I2CHSMADDR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					VAL		

Table 18-11: I2C High Speed Master Mode Code Register (I2CHSMADDR) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2:0	VAL	RW	0x1	The 3LSBs of the 8-bit high-speed mode master code in format of (0x00001xxx) This register can be written only when the I2C interface is disabled (I2CENABLE=0) Writes at other times have no effect.

SPINTROL

18.6.2.5 I2C Data Buffer and Command Register (I2CDATACMD)

Table 18-12: I2C Data Buffer and Command Register (I2CDATACMD) Layout

I2CDATACMD (I2C Data Buffer and Command Register) Offset: 0x10 Default: 0x00000000 Access: I2C -> I2CDATACMD.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							CMD
7	6	5	4	3	2	1	0
DATA							

Table 18-13: I2C Data Buffer and Command Register (I2CDATACMD) Field Description

Bits	Field Name	Type	Reset	Description
31:9	RESERVED_31_9	RO	0x0	Reserved
8	CMD	RW	0x0	Master mode 0: Write 1: Read Slave mode 0: Always read back 0 in receiver mode It should be set as 0 in transmitter mode 1: Write a 1 has no effect in receiver mode Write a 1 in transmitter mode results in TXABRT interrupt
7:0	DATA	RW	0x0	Data transmitted or received on the I2C bus. A write to the register sets the data to be transmitted. A read to the register gets the received data.

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18.6.2.6 Standard Speed I2C Clock SCL High Count Register (I2CSSHCNT)

Table 18-14: Standard Speed I2C Clock SCL High Count Register (I2CSSHCNT) Layout

I2CSSHCNT (Standard Speed I2C Clock SCL High Count Register) Offset: 0x14 Default: 0x000001F4 Access: I2C -> I2CSSHCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 18-15: Standard Speed I2C Clock SCL High Count Register (I2CSSHCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x1F4	Duration for SCL high in standard speed mode. i.e. SCL is high for I2CSSHCNT clock cycles The minimum valid value is 6. Write a value below 6 will be reset as 6 by the hardware. Register can be written only when I2CENABLE=0. Writes at other times have no effect.

SPINTROL

18.6.2.7 Standard Speed I2C Clock SCL Low Count Register (I2CSSLCNT)

Table 18-16: Standard Speed I2C Clock SCL Low Count Register (I2CSSLCNT) Layout

I2CSSLCNT (Standard Speed I2C Clock SCL Low Count Register) Offset: 0x18 Default: 0x0000024C Access: I2C -> I2CSSLCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 18-17: Standard Speed I2C Clock SCL Low Count Register (I2CSSLCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x24C	Duration for SCL low in standard speed mode. i.e. SCL is low for I2CSSLCNT clock cycles The minimum valid value is 8. Write a value below 8 will be reset as 8 by the hardware. Register can be written only when I2CENABLE=0. Writes at other times have no effect.

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18.6.2.8 Fast Speed I2C Clock SCL High Count Register (I2CFSHCNT)

Table 18-18: Fast Speed I2C Clock SCL High Count Register (I2CFSHCNT) Layout

I2CFSHCNT (Fast Speed I2C Clock SCL High Count Register) Offset: 0x1C Default: 0x0000004B Access: I2C -> I2CFSHCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 18-19: Fast Speed I2C Clock SCL High Count Register (I2CFSHCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x4B	Duration for SCL high in fast speed mode. i.e. SCL is high for I2CFSHCNT clock cycles The minimum valid value is 6. Write a value below 6 will be reset as 6 by the hardware. Register can be written only when I2CENABLE=0. Writes at other times have no effect.

18.6.2.9 Fast Speed I2C Clock SCL Low Count Register (I2CFSLCNT)

Table 18-20: Fast Speed I2C Clock SCL Low Count Register (I2CFSLCNT) Layout

I2CFSLCNT (Fast Speed I2C Clock SCL Low Count Register) Offset: 0x20 Default: 0x000000A3 Access: I2C -> I2CFSLCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 18-21: Fast Speed I2C Clock SCL Low Count Register (I2CFSLCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0xA3	Duration for SCL low in fast speed mode. i.e. SCL is low for I2CFSLCNT clock cycles The minimum valid value is 8. Write a value below 8 will be reset as 8 by the hardware. Register can be written only when I2CENABLE=0. Writes at other times have no effect.

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18.6.2.10 High Speed I2C Clock SCL High Count Register (I2CHSHCNT)

Table 18-22: High Speed I2C Clock SCL High Count Register (I2CHSHCNT) Layout

I2CHSHCNT (High Speed I2C Clock SCL High Count Register) Offset: 0x24 Default: 0x00000008 Access: I2C -> I2CHSHCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 18-23: High Speed I2C Clock SCL High Count Register (I2CHSHCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x8	Duration for SCL high in high speed mode. i.e. SCL is high for I2CHSHCNT clock cycles The minimum valid value is 6. Write a value below 6 will be reset as 6 by the hardware. Register can be written only when I2CENABLE=0. Writes at other times have no effect.

18.6.2.11 High Speed I2C Clock SCL Low Count Register (I2CHSLCNT)

Table 18-24: High Speed I2C Clock SCL Low Count Register (I2CHSLCNT) Layout

I2CHSLCNT (High Speed I2C Clock SCL Low Count Register) Offset: 0x28 Default: 0x00000014 Access: I2C -> I2CHSLCNT.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 18-25: High Speed I2C Clock SCL Low Count Register (I2CHSLCNT) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x14	Duration for SCL low in high speed mode. i.e. SCL is low for I2CHSLCNT clock cycles The minimum valid value is 8. Write a value below 8 will be reset as 8 by the hardware. Register can be written only when I2CENABLE=0. Writes at other times have no effect.

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18.6.2.12 I2C Interrupt Flag Register (I2CIF)

Table 18-26: I2C Interrupt Flag Register (I2CIF) Layout

I2CIF (I2C Interrupt Flag Register) Offset: 0x2C Default: 0x00000000 Access: I2C -> I2CIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				GENCALL	STARTDET	STOPDET	ACT
7	6	5	4	3	2	1	0
RXDONE	TXABRT	RDREQ	TXDREQ	TXOVF	RXDAV	RXOVF	RXUDF

Table 18-27: I2C Interrupt Flag Register (I2CIF) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11	GENCALL	RO	0x0	General Call address received and acknowledged 0: Not occur 1: Ocurred
10	STARTDET	RO	0x0	START or RESTART condition flag 0: Condition is not detected 1: Condition is detected
9	STOPDET	RO	0x0	STOP condition flag 0: Condition is not detected 1: Condition is detected
8	ACT	RO	0x0	Latched I2C activity status flag 0: There is no activity detected on I2C interface 1: Activity has been detected on I2C interface
7	RXDONE	RO	0x0	Flag to indicate external master receive is done when I2C acts as a slave transmitter 0: Slave transmission is acknowledged by the other master, which continues data receiving. 1: Slave transmission is not acknowledge by the other master, which finishes the data receiving.
6	TXABRT	RO	0x0	Latched transmission abort flag 0: No transmission abortion occurred 1: Transimission aborted and TX FIFO remains in flushed state until the register I2CTXABRTCLR is read

SPINTROL

Bits	Field Name	Type	Reset	Description
5	RDREQ	RO	0x0	Latched external master read request flag when the I2C is acting as a slave 0: No read request is received from another master 1: Read request was received from another master. The processor must respond to this interrupt and then write the requested data to the I2CDATACMD register.
4	TXDREQ	RO	0x0	Flag to indicate the transmit buffer is at or below the threshold value set in the I2CTXTH register so as to request for more data 0: Transmit buffer is above threshold 1: Transmit buffer is at or below the threshold Self-cleared when level goes above threshold
3	TXOVF	RO	0x0	Flag to indicate an attempt to write I2CDATACMD register when transmit buffer is fill to 15 0: Transmit buffer does not overflow 1: Transmit buffer overflows
2	RXDAV	RO	0x0	Flag to indicate the receive buffer reaches or goes above the threshold in the I2CRXTH register so that data is available for read. 0: Receive buffer is below threshold 1: Receive buffer is at or above the threshold Self-cleared when level goes below threshold
1	RXOVF	RO	0x0	Flag to indicate the receive buffer is completely filled to 16 and an additional byte is received from an external I2C device. The I2C acknowledges this, but any data bytes received after the FIFO is full are lost. 0: Receive buffer does not overflow 1: Receive buffer overflows
0	RXUDF	RO	0x0	Flag to indicate the processor attempts to read the receive buffer via I2CDATACMD register when it is empty 0: Receive buffer does not underflow 1: Receive buffer underflows

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18.6.2.13 I2C Interrupt Enable Register (I2CIE)

Table 18-28: I2C Interrupt Enable Register (I2CIE) Layout

I2CIE (I2C Interrupt Enable Register) Offset: 0x30 Default: 0x000008FF Access: I2C -> I2CIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				GENCALL	STARTDET	STOPDET	ACT
7	6	5	4	3	2	1	0
RXDONE	TXABRT	RDREQ	TXDREQ	TXOVF	RXDAV	RXOVF	RXUDF

Table 18-29: I2C Interrupt Enable Register (I2CIE) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11	GENCALL	RW	0x1	Enable/disable GENCALL interrupt 0: Disable GENCALL interrupt 1: Enable GENCALL interrupt
10	STARTDET	RW	0x0	Enable/disable STARTDET interrupt 0: Disable STARTDET interrupt 1: Enable STARTDET interrupt
9	STOPDET	RW	0x0	Enable/disable STOPDET interrupt 0: Disable STOPDET interrupt 1: Enable STOPDET interrupt
8	ACT	RW	0x0	Enable/disable ACTIVITY interrupt 0: Disable ACTIVITY interrupt 1: Enable ACTIVITY interrupt
7	RXDONE	RW	0x1	Enable/disable RXDONE interrupt 0: Disable RXDONE interrupt 1: Enable RXDONE interrupt
6	TXABRT	RW	0x1	Enable/disable TXABRT interrupt 0: Disable TXABRT interrupt 1: Enable TXABRT interrupt
5	RDREQ	RW	0x1	Enable/disable RDREQ interrupt 0: Disable RDREQ interrupt 1: Enable RDREQ interrupt
4	TXDREQ	RW	0x1	Enable/disable TXDREQ interrupt 0: Disable TXDREQ interrupt

SPINTROL

Bits	Field Name	Type	Reset	Description
				1: Enable TXDREQ interrupt
3	TXOVF	RW	0x1	Enable/disable TXOVF interrupt 0: Disable TXOVF interrupt 1: Enable TXOVF interrupt
2	RXDAV	RW	0x1	Enable/disable RXDAV interrupt 0: Disable RXDAV interrupt 1: Enable RXDAV interrupt
1	RXOVF	RW	0x1	Enable/disable RXOVF interrupt 0: Disable RXOVF interrupt 1: Enable RXOVF interrupt
0	RXUDF	RW	0x1	Enable/disable RXUDF interrupt 0: Disable RXUDF interrupt 1: Enable RXUDF interrupt

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18.6.2.14 I2C Raw Interrupt Flag Register (I2CRAWIF)

Table 18-30: I2C Raw Interrupt Flag Register (I2CRAWIF) Layout

I2CRAWIF (I2C Raw Interrupt Flag Register) Offset: 0x34 Default: 0x00000000 Access: I2C -> I2CRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED				GENCALL	STARTDET	STOPDET	ACT
7	6	5	4	3	2	1	0
RXDONE	TXABRT	RDREQ	TXDREQ	TXOVF	RXDAV	RXOVF	RXUDF

Table 18-31: I2C Raw Interrupt Flag Register (I2CRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:12	RESERVED_31_12	RO	0x0	Reserved
11	GENCALL	RO	0x0	General Call address received and acknowledged 0: Not occur 1: Ocurred
10	STARTDET	RO	0x0	START or RESTART condition flag 0: Condition is not detected 1: Condition is detected
9	STOPDET	RO	0x0	STOP condition flag 0: Condition is not detected 1: Condition is detected
8	ACT	RO	0x0	Latched I2C activity status flag 0: There is no activity detected on I2C interface 1: Activity has been detected on I2C interface
7	RXDONE	RO	0x0	Flag to indicate external master receive is done when I2C acts as a slave transmitter 0: Slave transmission is acknowledged by the other master, which continues data receiving. 1: Slave transmission is not acknowledge by the other master, which finishes the data receiving.
6	TXABRT	RO	0x0	Latched transmission abort flag 0: No transmission abortion occurred 1: Transimission aborted and TX FIFO remains in flushed state until the register I2CTXABRTCLR is read

SPINTROL

Bits	Field Name	Type	Reset	Description
5	RDREQ	RO	0x0	Latched external master read request flag when the I2C is acting as a slave 0: No read request is received from another master 1: Read request was received from another master. The processor must respond to this interrupt and then write the requested data to the I2CDATACMD register.
4	TXDREQ	RO	0x0	Flag to indicate the transmit buffer is at or below the threshold value set in the I2CTXTH register so as to request more data. 0: Transmit buffer is above threshold 1: Transmit buffer is at or below the threshold Self-cleared when level goes above threshold
3	TXOVF	RO	0x0	Flag to indicate an attempt to write I2CDATACMD register when transmit buffer is fill to 15 0: Transmit buffer does not overflow 1: Transmit buffer overflows
2	RXDAV	RO	0x0	Flag to indicate the receive buffer reaches or goes above the threshold in the I2CRXTH register so that data is available for read. 0: Receive buffer is below threshold 1: Receive buffer is at or above the threshold Self-cleared when level goes below threshold
1	RXOVF	RO	0x0	Flag to indicate the receive buffer is completely filled to 16 and an additional byte is received from an external I2C device. The I2C acknowledges this, but any data bytes received after the FIFO is full are lost. 0: Receive buffer does not overflow 1: Receive buffer overflows
0	RXUDF	RO	0x0	Flag to indicate the processor attempts to read the receive buffer via I2CDATACMD register when it is empty 0: Receive buffer does not underflow 1: Receive buffer underflows

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18.6.2.15 I2C Receive FIFO Threshold Register (I2CRXTH)

Table 18-32: I2C Receive FIFO Threshold Register (I2CRXTH) Layout

I2CRXTH (I2C Receive FIFO Threshold Register) Offset: 0x38 Default: 0x00000000 Access: I2C -> I2CRXTH.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
KEY				VAL			

Table 18-33: I2C Receive FIFO Threshold Register (I2CRXTH) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:4	KEY	WO	0x0	Must write 0x0 to this field when write to low LSBs, else LSBs is always 0xF. Always read back 0
3:0	VAL	RW	0x0	Receive FIFO threshold level to trigger the RXDAV interrupt 0000: 1 entry 0001: 2 entries 0010: 3 entries 0011: 4 entries 0100: 5 entries 0101: 6 entries 0110: 7 entries 0111: 8 entries 1000: 9 entries 1001: 10 entries 1010: 11 entries 1011: 12 entries 1100: 13 entries 1101: 14 entries 1110: 15 entries 1111: 16 entries

SPINTROL

18.6.2.16 I2Ctransmit FIFO Threshold Register (I2CTXTH)

Table 18-34: I2Ctransmit FIFO Threshold Register (I2CTXTH) Layout

I2CTXTH (I2C Transmit FIFO Threshold Register) Offset: 0x3C Default: 0x00000000 Access: I2C -> I2CTXTH.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
KEY				VAL			

Table 18-35: I2Ctransmit FIFO Threshold Register (I2CTXTH) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:4	KEY	WO	0x0	Must write 0x0 to this field when write to low LSBs, else LSBs is always 0xF. Always read back 0
3:0	VAL	RW	0x0	Transmit FIFO threshold level to trigger the TXDREQ interrupt 0000: 0 entry 0001: 1 entries 0010: 2 entries 0011: 3 entries 0100: 4 entries 0101: 5 entries 0110: 6 entries 0111: 7 entries 1000: 8 entries 1001: 9 entries 1010: 10 entries 1011: 11 entries 1100: 12 entries 1101: 13 entries 1110: 14 entries 1111: 15 entries

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18.6.2.17 Clear Combined and Individual Interrupt Register (I2CINTCLR)

Table 18-36: Clear Combined and Individual Interrupt Register (I2CINTCLR) Layout

I2CINTCLR (Clear Combined and Individual Interrupt Register) Offset: 0x40 Default: 0x00000000 Access: I2C -> I2CINTCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-37: Clear Combined and Individual Interrupt Register (I2CINTCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the combined interrupt, all individual interrupts, and the I2CTXABRTSRC register. This bit does not clear hardware clearable interrupts but software clearable interrupts. Refer to I2CTXABRTSRC.STARTNORESTART for an exception to clear I2CTXABRTSRC register.

18.6.2.18 Clear RXUDF Interrupt Register (I2CRXUDFCLR)

Table 18-38: Clear RXUDF Interrupt Register (I2CRXUDFCLR) Layout

I2CRXUDFCLR (Clear RXUDF Interrupt Register) Offset: 0x44 Default: 0x00000000 Access: I2C -> I2CRXUDFCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-39: Clear RXUDF Interrupt Register (I2CRXUDFCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the RXUDF flag

SPINTROL

18.6.2.19 Clear RXOVF Interrupt Register (I2CRXOVFCLR)

Table 18-40: Clear RXOVF Interrupt Register (I2CRXOVFCLR) Layout

I2CRXOVFCLR (Clear RXOVF Interrupt Register) Offset: 0x48 Default: 0x00000000 Access: I2C -> I2CRXOVFCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-41: Clear RXOVF Interrupt Register (I2CRXOVFCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the RXOVF flag

18.6.2.20 Clear TXOVF Interrupt Register (I2CTXOVFCLR)

Table 18-42: Clear TXOVF Interrupt Register (I2CTXOVFCLR) Layout

I2CTXOVFCLR (Clear TXOVF Interrupt Register) Offset: 0x4C Default: 0x00000000 Access: I2C -> I2CTXOVFCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-43: Clear TXOVF Interrupt Register (I2CTXOVFCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the TXOVF flag

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18.6.2.21 Clear RDREQ Interrupt Register (I2CRDREQCLR)

Table 18-44: Clear RDREQ Interrupt Register (I2CRDREQCLR) Layout

I2CRDREQCLR (Clear RDREQ Interrupt Register) Offset: 0x50 Default: 0x00000000 Access: I2C -> I2CRDREQCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-45: Clear RDREQ Interrupt Register (I2CRDREQCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the RDREQ flag

18.6.2.22 Clear TXABRT Interrupt Register (I2CTXABRTCLR)

Table 18-46: Clear TXABRT Interrupt Register (I2CTXABRTCLR) Layout

I2CTXABRTCLR (Clear TXABRT Interrupt Register) Offset: 0x54 Default: 0x00000000 Access: I2C -> I2CTXABRTCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-47: Clear TXABRT Interrupt Register (I2CTXABRTCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the TXABRT flag and the I2CTXABRTSRC register. This also releases the TX FIFO from the flushed/reset state, allowing more writes to the TX FIFO. Refer to I2CTXABRTSRC.STARTNORESTART for an exception to clear I2CTXABRTSRC register.

SPINTROL

18.6.2.23 Clear RXDONE Interrupt Register (I2CRXDONECLR)

Table 18-48: Clear RXDONE Interrupt Register (I2CRXDONECLR) Layout

I2CRXDONECLR (Clear RXDONE Interrupt Register) Offset: 0x58 Default: 0x00000000 Access: I2C -> I2CRXDONECLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-49: Clear RXDONE Interrupt Register (I2CRXDONECLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the RXDONE flag

18.6.2.24 Clear ACT Interrupt Register (I2CACTCLR)

Table 18-50: Clear ACT Interrupt Register (I2CACTCLR) Layout

I2CACTCLR (Clear ACT Interrupt Register) Offset: 0x5C Default: 0x00000000 Access: I2C -> I2CACTCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-51: Clear ACT Interrupt Register (I2CACTCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Reading this register clears the ACT flag if the I2C is not active anymore. If the I2C module is still active on the bus, the ACTIVITY flag continues to be set. It is automatically cleared by hardware if the module is disabled and there is no further activity on the bus.

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18.6.2.25 Clear STOPDET Interrupt Register (I2CSTOPDETCLR)

Table 18-52: Clear STOPDET Interrupt Register (I2CSTOPDETCLR) Layout

I2CSTOPDETCLR (Clear STOPDET Interrupt Register) Offset: 0x60 Default: 0x00000000 Access: I2C -> I2CSTOPDETCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-53: Clear STOPDET Interrupt Register (I2CSTOPDETCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the STOPDET flag

18.6.2.26 Clear STARTDET Interrupt Register (I2CSTARTDETCLR)

Table 18-54: Clear STARTDET Interrupt Register (I2CSTARTDETCLR) Layout

I2CSTARTDETCLR (Clear STARTDET Interrupt Register) Offset: 0x64 Default: 0x00000000 Access: I2C -> I2CSTARTDETCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-55: Clear STARTDET Interrupt Register (I2CSTARTDETCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the STARTDET flag

SPINTROL

18.6.2.27 Clear GENCALL Interrupt Register (I2CGENCALLCLR)

Table 18-56: Clear GENCALL Interrupt Register (I2CGENCALLCLR) Layout

I2CGENCALLCLR (Clear GENCALL Interrupt Register) Offset: 0x68 Default: 0x00000000 Access: I2C -> I2CGENCALLCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							CLR

Table 18-57: Clear GENCALL Interrupt Register (I2CGENCALLCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	CLR	RO	0x0	Read this register to clear the GENCALL flag

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18.6.2.28 I2C Enable Register (I2CENABLE)

Table 18-58: I2C Enable Register (I2CENABLE) Layout

I2CENABLE (I2C Enable Register) Offset: 0x6C Default: 0x00000000 Access: I2C -> I2CENABLE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							EN

Table 18-59: I2C Enable Register (I2CENABLE) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	EN	RW	0x0	Controls whether the I2C is enabled. There are two I2C clock delay when enable or disable the I2C. When I2C is disabled, the following occurs: – The TX FIFO and RX FIFO get flushed. – Status bits in the I2CIF register are still active until I2C goes into IDLE state. – If the module is transmitting, it stops as well as deletes the contents of the transmit buffer after the current transfer is complete. – If the module is receiving, the I2C stops the current transfer at the end of the current byte and does not acknowledge the transfer. 0: Disable I2C (Hold FIFOs in an erased state). Software can disable I2C while it is active. However, it is important that care be taken to ensure that i2c is disabled properly. 1: Enable I2C

SPINTROL

18.6.2.29 I2C Status Register (I2CSTS)

Table 18-60: I2C Status Register (I2CSTS) Layout

I2CSTS (I2C Status Register) Offset: 0x70 Default: 0x00000006 Access: I2C -> I2CSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED	SACT	MACT	RFF	RFNE	TFE	TFNF	ACT

Table 18-61: I2C Status Register (I2CSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:7	RESERVED_31_7	RO	0x0	Reserved
6	SACT	RO	0x0	Slave FSM (Finite State Machine) activity status 0: Slave FSM is in IDLE state (Inactive) 1: Slave FSM is not in IDLE state (Active)
5	MACT	RO	0x0	Master FSM activity status 0: Master FSM is in IDLE state (Inactive) 1: Master FSM is not in IDLE state (Active)
4	RFF	RO	0x0	Receive FIFO completely full 0: Receive FIFO contains empty location 1: Receive FIFO is completely full
3	RFNE	RO	0x0	Receive FIFO not empty 0: Receive FIFO is empty 1: Receive FIFO contains one or more entries
2	TFE	RO	0x1	Transmit FIFO completely empty 0: Transmit FIFO contains one or more valid entries 1: Transmit FIFO is completely empty
1	TFNF	RO	0x1	Transmit FIFO not full 0: Transmit FIFO is full 1: Transmit FIFO contains empty locations
0	ACT	RO	0x0	I2C activity status (Logic OR of SACT and MACT) 0: Both master and slave FSM are in idle state 1: Either master or slave FSM is active

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18.6.2.30 I2C Transmit FIFO Level Register (I2CTFLVL)

Table 18-62: I2C Transmit FIFO Level Register (I2CTFLVL) Layout

I2CTFLVL (I2C Transmit FIFO Level Register) Offset: 0x74 Default: 0x00000000 Access: I2C -> I2CTFLVL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			VAL				

Table 18-63: I2C Transmit FIFO Level Register (I2CTFLVL) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4:0	VAL	RO	0x0	Number of valid data entries in the transmit FIFO.

18.6.2.31 I2C Receive FIFO Level Register (I2CRFLVL)

Table 18-64: I2C Receive FIFO Level Register (I2CRFLVL) Layout

I2CRFLVL (I2C Receive FIFO Level Register) Offset: 0x78 Default: 0x00000000 Access: I2C -> I2CRFLVL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			VAL				

Table 18-65: I2C Receive FIFO Level Register (I2CRFLVL) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4:0	VAL	RO	0x0	Number of valid data entries in the receive FIFO.

SPINTROL

18.6.2.32 I2C SDA Hold-Time Register (I2CSDAHOLD)

Table 18-66: I2C SDA Hold-Time Register (I2CSDAHOLD) Layout

I2CSDAHOLD (I2C SDA Hold-Time Register) Offset: 0x7C Default: 0x00000001 Access: I2C -> I2CSDAHOLD.all							
31	30	29	28	27	26	25	24
RESERVED_31_16							
23	22	21	20	19	18	17	16
RESERVED_31_16							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 18-67: I2C SDA Hold-Time Register (I2CSDAHOLD) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15:0	VAL	RW	0x1	Configure SDA hold time as VAL CLK_I2C cycles. i.e. If the required hold delay is 1000ns, then for an CLK_I2C frequency of 10 MHz, this register is recommended to be programmed as 11. This register can be written only when I2CENABLE=0. Writes at other times have no effect.

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18.6.2.33 I2C Transmit Abort Source Register (I2CTXABRTSRC)

Table 18-68: I2C Transmit Abort Source Register (I2CTXABRTSRC) Layout

I2CTXABRTSRC (I2C Transmit Abort Source Register) Offset: 0x80 Default: 0x00000000 Access: I2C -> I2CTXABRTSRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 SLVRDINTX	14 SARBLOST	13 SLVFLUSHTF	12 MARBLOST	11 MASTERDIS	10 RD10BNORESTART	9 STARTNORESTART	8 HSNORESTART
7 STARTACKDET	6 HSACKDET	5 GCREAD	4 GCNACK	3 TXDATANACK	2 ADDR10B2NACK	1 ADDR10B1NACK	0 ADDR7BNACK

Table 18-69: I2C Transmit Abort Source Register (I2CTXABRTSRC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	SLVRDINTX	RO	0x0	Role of I2C: Slave transmitter This bit is set when the processor side responds to a slave mode request for data to be transmitted to a remote master and user writes a 1 in CMD (bit 8) of I2CDATACMD register.
14	SARBLOST	RO	0x0	Role of I2C: Slave transmitter This bit is set when slave lost the bus while transmitting data to a remote master. I2CTXABRTSRC.MARBLOST is set at the same time. Note: Even though the slave never 'owns' the bus, something could go wrong on the bus. This is a failsafe check. For instance, during a data transmission at the low-to-high transition of SCL, if what is on the data bus is not what is supposed to be transmitted, then I2C no longer own the bus.
13	SLVFLUSHTF	RO	0x0	Role of I2C: Slave transmitter This bis is set when slave has received a read command and some data exists in the TX FIFO so the slave issues a TXABRT interrupt to flush old data in TX FIFO.
12	MARBLOST	RO	0x0	Role of I2C: Master/slave transmitter This bit is set when master has lost arbitration, or if I2CTXABRTSRC.SARBLOST is also set, then the slave transmitter has lost arbitration.
11	MASTERDIS	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when user tries to initiate a master operation with the master mode is disabled.

SPINTROL

Bits	Field Name	Type	Reset	Description
10	RD10BNORESTART	RO	0x0	Role of I2C: Master receiver This bit is set when the restart is disabled (I2CCTL.RESTARTEN=0) and the master sends a read command in 10-bit addressing mode.
9	STARTNORESTART	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when the restart is disabled (I2CCTL.RESTARTEN=0) and the user is trying to send a START Byte. Follow configurations below to avoid this error (1) I2CCTL.RESTARTEN=1 (2) I2CMASTERADDR.SPECIAL=0 or I2CMASTERADDR.GCORSTART=0 Otherwise, this bit is set again at next clock after it is cleared by reading from I2CTXABRTCLR register.
8	HSNORESTART	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when the restart is disabled (I2CCTL.RESTARTEN=0) and the user is trying to use the master to transfer data in high speed mode.
7	STARTACKDET	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when master has sent a START Byte and the START Byte was acknowledged (wrong behavior).
6	HSACKDET	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when master is in high speed mode and the high speed master code was acknowledged (wrong behavior).
5	GCREAD	RO	0x0	Role of I2C: Master transmitter This bit is set when master sent a General Call but the user programmed the byte following the General Call to be a read from the bus (I2CDATACMD.CMD=1).
4	GCNACK	RO	0x0	Role of I2C: Master transmitter This bit is set when master sent a General Call and no slave on the bus acknowledged the General Call.
3	TXDATANACK	RO	0x0	Role of I2C: Master transmitter This bit is set when master has received an acknowledgement for the address, but when it sent data byte(s) following the address, it did not receive an acknowledge from the remote slave(s).

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Bits	Field Name	Type	Reset	Description
2	ADDR10B2NACK	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when master is in 10-bit address mode and the second address byte of the 10-bit address was not acknowledged by any slave.
1	ADDR10B1NACK	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when master is in 10-bit address mode and the first 10-bit address byte was not acknowledged by any slave.
0	ADDR7BNACK	RO	0x0	Role of I2C: Master transmitter/receiver This bit is set when master is in 7-bit addressing mode and the address sent was not acknowledged by any slave.

18.6.2.34 I2C SDA Setup Register (I2CSDASETUP)

Table 18-70: I2C SDA Setup Register (I2CSDASETUP) Layout

I2CSDASETUP (I2C SDA Setup Register) Offset: 0x94 Default: 0x00000064 Access: I2C -> I2CSDASETUP.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
VAL							

Table 18-71: I2C SDA Setup Register (I2CSDASETUP) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:0	VAL	RW	0x64	Configure SDA setup time as *VAL* CLK_I2C cycles i.e. If the required setup delay is 1000ns, then for an CLK_I2C frequency of 10 MHz, this register is recommended to be programmed as 11.

SPINTROL

18.6.2.35 I2C ACK General Call Register (I2CACKGC)

Table 18-72: I2C ACK General Call Register (I2CACKGC) Layout

I2CACKGC (I2C ACK General Call Register) Offset: 0x98 Default: 0x00000001 Access: I2C -> I2CACKGC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							ACKGC

Table 18-73: I2C ACK General Call Register (I2CACKGC) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	ACKGC	RW	0x1	Respond upon General Call 0: Responds General Call with an NACK 1: Responds General Call with an ACK

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18.6.2.36 I2C Enable Status Register (I2CENSTS)

Table 18-74: I2C Enable Status Register (I2CENSTS) Layout

I2CENSTS (I2C Enable Status Register) Offset: 0x9C Default: 0x00000000 Access: I2C -> I2CENSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					SLVRDLOST	SLVDISONBUSY	EN

Table 18-75: I2C Enable Status Register (I2CENSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	SLVRDLOST	RO	0x0	Slave received data lost upon disable I2C 0: Slave receiver operation is done before I2CENABLE is changed from 1 to 0 1: Slave receiver operation is aborted with at least one data byte received from an I2C transfer when I2CENABLE is changed from 1 to 0
1	SLVDISONBUSY	RO	0x0	Slave disabled while it is busy 0: I2CENABLE is stable during slave operation 1: I2CENABLE is changed from 1 to 0 when I2C slave is receiving from a remote mater on (a) The address byte of the slave transmitter (b) The address and data bytes of the slave receiver
0	EN	RO	0x0	I2C enabled status 0: I2C is deemed completely inactive Can safely read SLVRDLOST and SLVDISONBUSY bits 1: I2C is deemed to be in an enabled state

SPINTROL

18.6.2.37 I2C Fast Speed Spike Suppresion Limit Register (I2CFSSPKLEN)

Table 18-76: I2C Fast Speed Spike Suppresion Limit Register (I2CFSSPKLEN) Layout

I2CFSSPKLEN (I2C Fast Speed Spike Suppresion Limit Register) Offset: 0xA0 Default: 0x00000006 Access: I2C -> I2CFSSPKLEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
VAL							

Table 18-77: I2C Fast Speed Spike Suppresion Limit Register (I2CFSSPKLEN) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:0	VAL	RW	0x6	Duration in fast speed mode of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic. The minimum value is 1 and write a 0 will be reset as 1 by the hardware. This register can be written only when I2CENABLE=0. Writes at other times have no effect.

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18.6.2.38 I2C High Speed Spike Suppresion Limit Register (I2CHSSPKLEN)

Table 18-78: I2C High Speed Spike Suppresion Limit Register (I2CHSSPKLEN) Layout

I2CHSSPKLEN (I2C High Speed Spike Suppresion Limit Register) Offset: 0xA4 Default: 0x00000002 Access: I2C -> I2CHSSPKLEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
VAL							

Table 18-79: I2C High Speed Spike Suppresion Limit Register (I2CHSSPKLEN) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7:0	VAL	RW	0x2	Duration in high speed mode of the longest spike in the SCL or SDA lines that are filtered out by the spike suppression logic. The minimum value is 1 and write a 0 will be reset as 1 by the hardware. This register can be written only when I2CENABLE=0. Writes at other times have no effect.

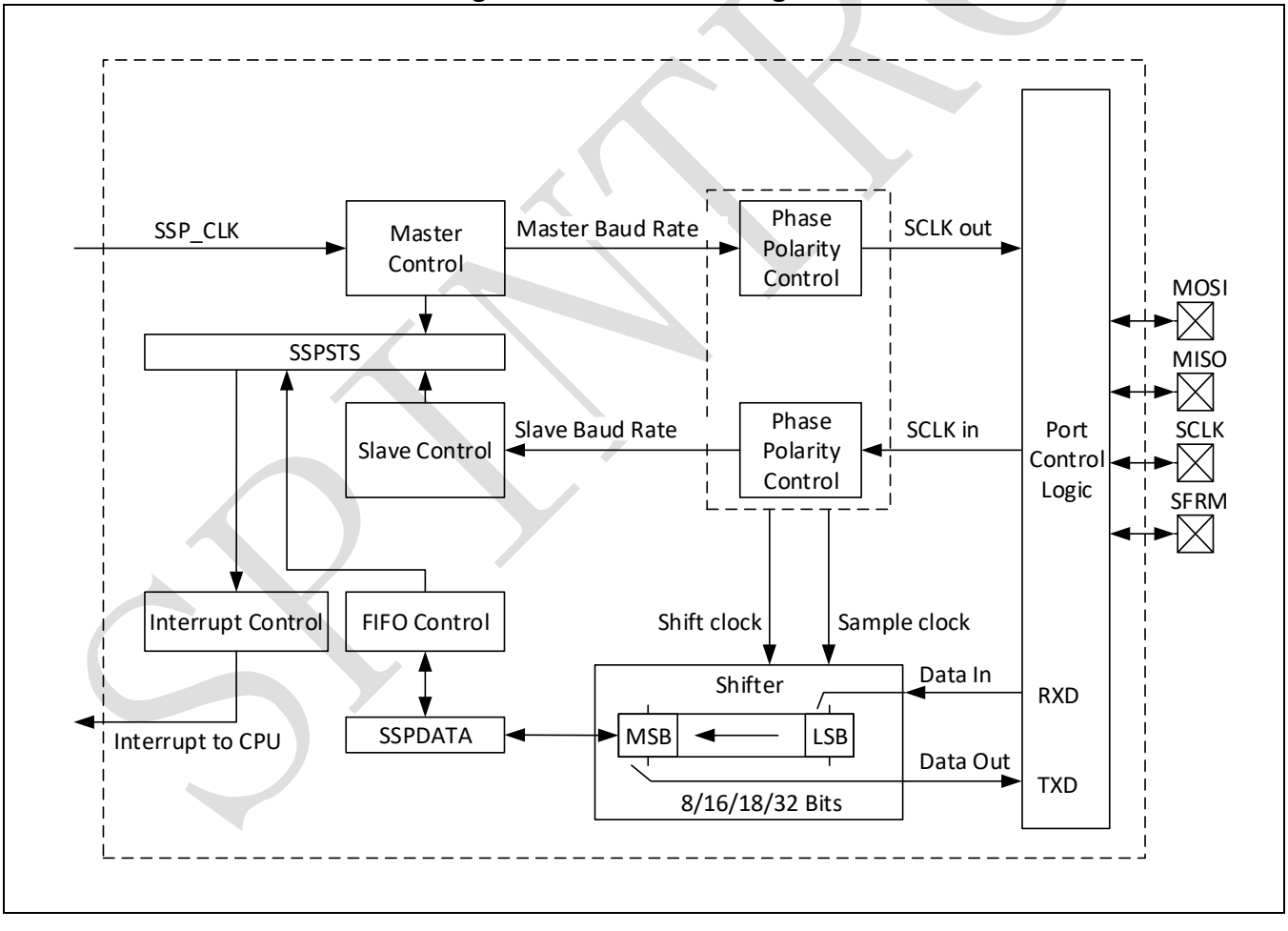
SPINTROL

19 SSP

19.1 SSP overview

The SPC2168 SSP interface is a synchronous, full duplex, serial data transfer port that can be used as a connection to a variety of external interfaces, such as flash, ADC, CODEC, etc. The SSP interface can be programmed to operate in Master Mode (the attached peripheral devices as slaves) or Slave Mode (the attached peripheral devices as masters). The SSP port supports different serial bit rates through the configurable interface clocks. Serial data sample size can be configured to 8, 16, 18, or 32 bits in length. A FIFO is provided for Transmit data and a second independent FIFO is provided for Receive data. Both FIFOs are 16 sample in depth and 32 bit in width. The FIFOs can be loaded or emptied by CPU. The SSP can be driven by polling mode or interrupt request mode. SSP module is mainly composed of control, status and data registers, shifter logic, FIFO control logic, master and slave control logic and port control logic, as shown in Figure 19-1.

Figure 19-1: SSP block diagram



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19.2 SSP features

The SPC2168 SSP has following enhanced features:

- Directly supports Motorola Serial Peripheral interface (SPI)
- Data transfer rate up to 50 Mbps
- Master or Slave mode operation
- Full duplex
- Receive only operation
- Programmable data frame size: 1 to 32 bits
- Programmable polarity for select port (SFRM)
- MSB-first data order
- Programmable clock polarity and phase
- Two independent transmit and receive FIFO with 16 sample in depth and 32 bit in width, and all support packed mode

19.3 SSP signal description

Table 19-1 describes the SPC2168 SSP interface bus signals.

Table 19-1: SSP signal description

Signal Name	Type	Descriptions
MOSI	Input/ Output	This port is used to transmit data out of the SPI module when it is configured as a Master and receive data when it is configured as Slave.
MISO	Input/ Output	This port is used to transmit data out of the SPI module when it is configured as a Slave and receive data when it is configured as Master.
SCLK	Input/ Output	This port is used to output the clock with respect to which the SPI transfers data or receive clock in case of Slave.
SFRM	Input/ Output	This port is used to output the select signal from the SPI module to another peripheral with which a data transfer is to take place when its configured as a Master and its used as an input to receive the slave select signal when the SPI is configured as Slave.

19.4 SSP function description

This section describes the various modes of operation of the SSP. Include connection, baud rate generation, FIFO operation, data frame formats and interrupts.

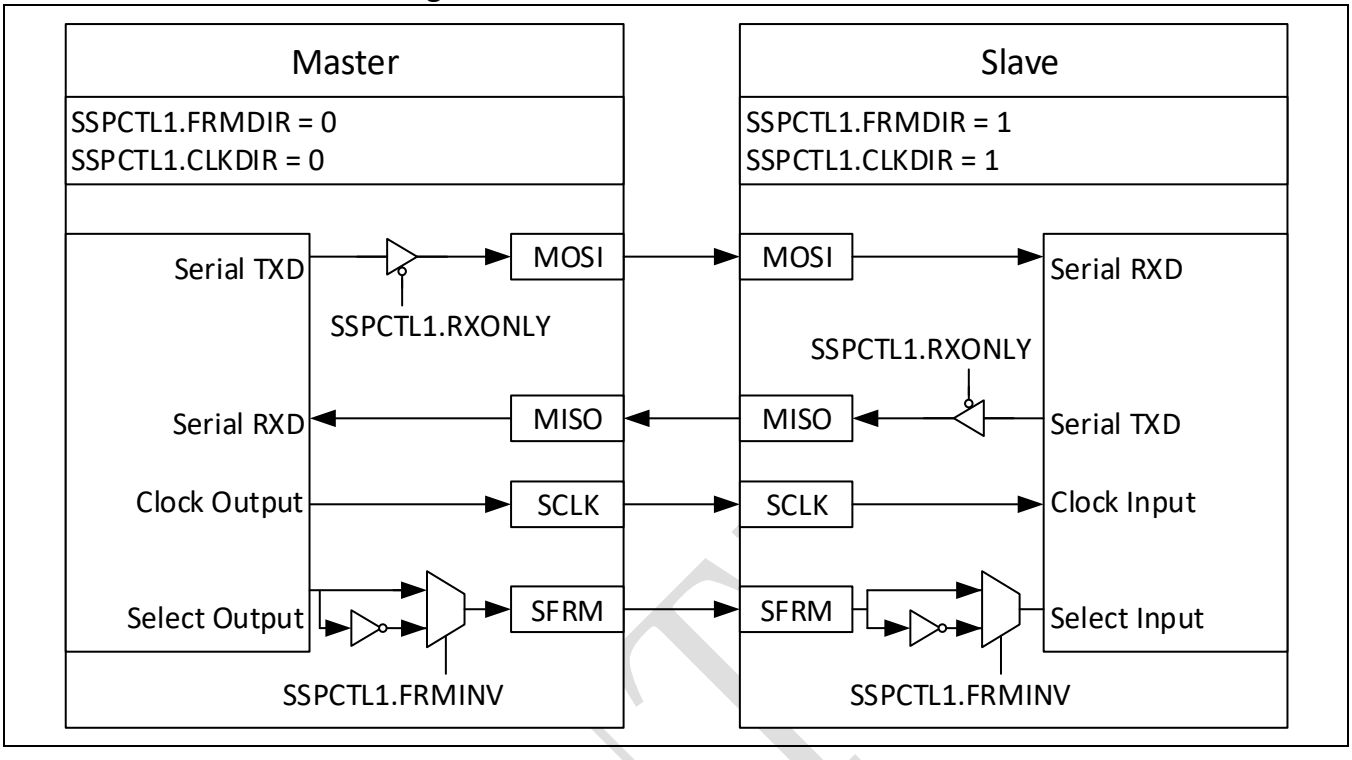
19.4.1 Introduction to operation

SSP can be configured as master or slave. The master send clock SCLK and signal SFRM to slave, and slave begin transfer data based on SCLK and SFRM. The master data port (MOSI/MISO) connect with slave data port with the same name. Master send data to MOSI, receive data from MISO. Slave receive data from

SPINTROL

MOSI, and send data to MISO. As shown in Figure 19-2, a typical connections of the SSP for communications between two controllers: a master and a slave.

Figure 19-2: SSP master-slave connection



There are three possible methods for data transmission:

- Master sends data; slave sends dummy data.
- Master sends data; slave sends data.
- Master sends dummy data; slave sends data.

When sending dummy data, SSPCTL1.RXONLY can be set high if do not want to send data from serial TXD to external MOSI port.

19.4.2 Baud rate generation

SSP baud rate clock is generated by SSPCLK, which is divided from SYSCLK1 as shown in Figure 3-11. The SSP clock divider is 16 bits.

19.4.3 FIFO operation

The SPC2168 SSP has two independent FIFOs for transmitting and receiving. The CPU will load and empty those FIFOs. The CPU will transfer one FIFO entry per access and the accesses must always be 32-bits wide. The CPU writes to TXFIFO are 32-bits wide, but the serializing logic will ignore all bits beyond the programmed FIFO data size (SSPCTL0.ESIZESEL and SSPCTL0.SIZESEL). The CPU reads from the RXFIFO are also 32-bits wide with zeros inserted in the MSBs down to the programmed data size.

The CPU only see one 32-bit location for both TXFIFO and RXFIFO. For data transmission, the SSP interface takes the data from TXFIFO, serialized the data and transmits the data through TXD interface signal to the external peripherals. For data receiving, the serial data through RXD serial interface signal is converted to parallel data and written into the RXFIFO. Depends on whether the access is a READ or

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WRITE transfer from CPU, the FIFO Data Register automatically target the RXFIFO or TXFIFO. From the memory-map perspective, the TXFIFO and RXFIFO share the same address.

An interrupt service request is generated if a programmable FIFO trigger threshold exceeded which signals the CPU to empty the RXFIFO or refill the TXFIFO.

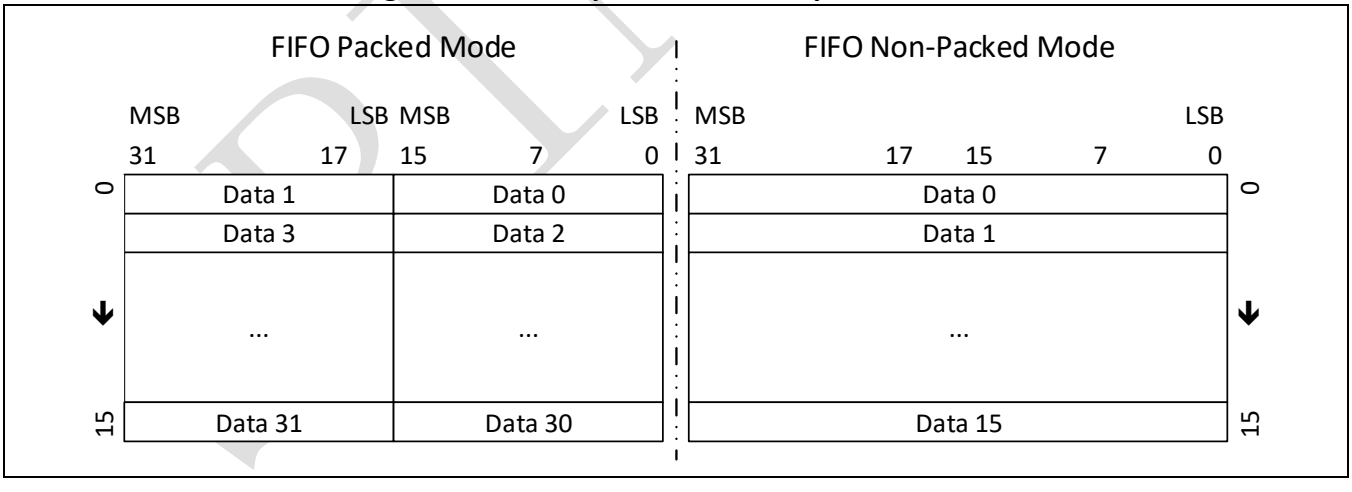
Note: If SSP was configured as slave and worked in receive only mode (SSPCTL1.RXONLY=1), there is no need to write Transmit FIFO when receiving data (half-duplex). However, writing Transmit FIFO can still sending data.

19.4.3.1 Parallel data formats for FIFO storage

The sample data size can be 8, 16, 18 or 32 bits. The data in the FIFOs is either stored as 32-bits wide per data sample or as 16-bits wide per sample (packed mode). Within 32-bits or 16-bits sample mode, the stored data sample is right-justified, with LSB of the word in bit 0. The unused bits are packed as zero above the MSB for read mode and 'don't care' bit for write mode. The logic in SSP will automatically formats data in the Transmit FIFO so that the sample data will be properly transmitted on TXD signal with the selected frame format.

When the FIFOs are operating in packed mode, as shown in Figure 19-3, each FIFO is 32 rows in depth by 16-bits in width for a total of 32 data samples. Each sample can be 8 or 16 bits in length. When the data is serialized and transmitted, bits15-0 are transmitted first, followed by bits31-16. The best practice for packed mode is to treat FIFO as a single entry of two samples. Thus, the CPU should write and read 32 bits of data at a time where each Write or Read transfers two samples. The entire FIFO width (32 bits) must be read or written in this mode. Also the FIFO trigger threshold need to be calculated in 32-bits read and write, not based on 16-bits.

Figure 19-3: FIFO packed and non-packed mode



Read SSPSTS.RFODDSTS and SSPSTS.TFODDSTS can show even sampled data in FIFO or not. These state bits will help to read data in packed FIFO correctly.

19.4.3.2 Trailing bytes in RXFIFO

When the number of samples in the RXFIFO is less than its trigger threshold level and no additional data is received, the remaining bytes are called RXFIFO trailing bytes. The trailing bytes left in the RXFIFO are handled by the CPU polling method by default. To read out the trailing bytes from the RXFIFO, software

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should read all trailing bytes as indicated by the Receive FIFO Not Empty (SSPSTS.RNE) fields in the SSP Status Register.

19.4.3.3 FIFO threshold

Each FIFO has a configurable trigger threshold that can be used to trigger an interrupt. When the number of entries in RXFIFO exceeds the RXFIFO trigger threshold (SSPCTL1.RFTH field in SSP Control Register 1), an interrupt can be generated (if enabled) to signal the CPU to empty the RXFIFO. When the number of entries in the TXFIFO is less than or equal to the TXFIFO trigger threshold (SSPCTL1.TFTH field in SSP Control Register 1) plus 1, an interrupt can be generated (if enabled) to signal the CPU to refill the TXFIFO.

The CPU can poll the SSP Status Register to determine how many samples are in a FIFO or whether the FIFO is full or empty. Software is responsible for ensuring that the proper RXFIFO/TXFIFO trigger threshold values are chosen to prevent RXFIFO overflow or TXFIFO underflow errors.

19.4.4 Frame formats

19.4.4.1 Clock phase and polarity controls

The SSPCTL1.CLKPOL control clock polarity and specifies an active high or low clock and has no significant effect on the transmission format. The SSPCTL1.CLKPHS control clock phase and selects one of two fundamentally different transmission formats.

Clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transmissions to allow a master device to communicate with peripheral slaves having different requirements.

SCLK only toggles during active transfers (does not run continuously).

19.4.4.2 SFRM polarity control

The SSPCTL1.FRMINV control select signal polarity, normally used as high when idle and low when transfer data.

19.4.4.3 PHS = 0 frame format

When the SSP port is disabled or in idle mode, SFRM is high, MOSI and MISO is Hi-impedance, SCLK is low (SSPCTL1.CLKPOL = 0) or high (SSPCTL1.CLKPOL = 1). As shown in Figure 19-4.

When transmit data is ready to be sent and SSPCTL1.CLKPHS is low, the first SCLK edge is used to sample the first data bit for both master and slave. SFRM goes low (half clock period before the first edge of SCLK) and stay low during the transfer period. SFRM goes high again after half clock period of last SCLK edge.

The MSB of the transmit data is driven onto MOSI/MISO before half clock period of the first SCLK edge. The remainder bits of transmit data will be driven onto MOSI/MISO when the even edge of SCLK occurred. And odd edge of SCLK occurred will sample MOSI/MISO data bit and shift it into the LSB, MSB will be shift out and be latched for next edge driven onto MOSI/MISO. 1-32 bits can be transferred per frame.

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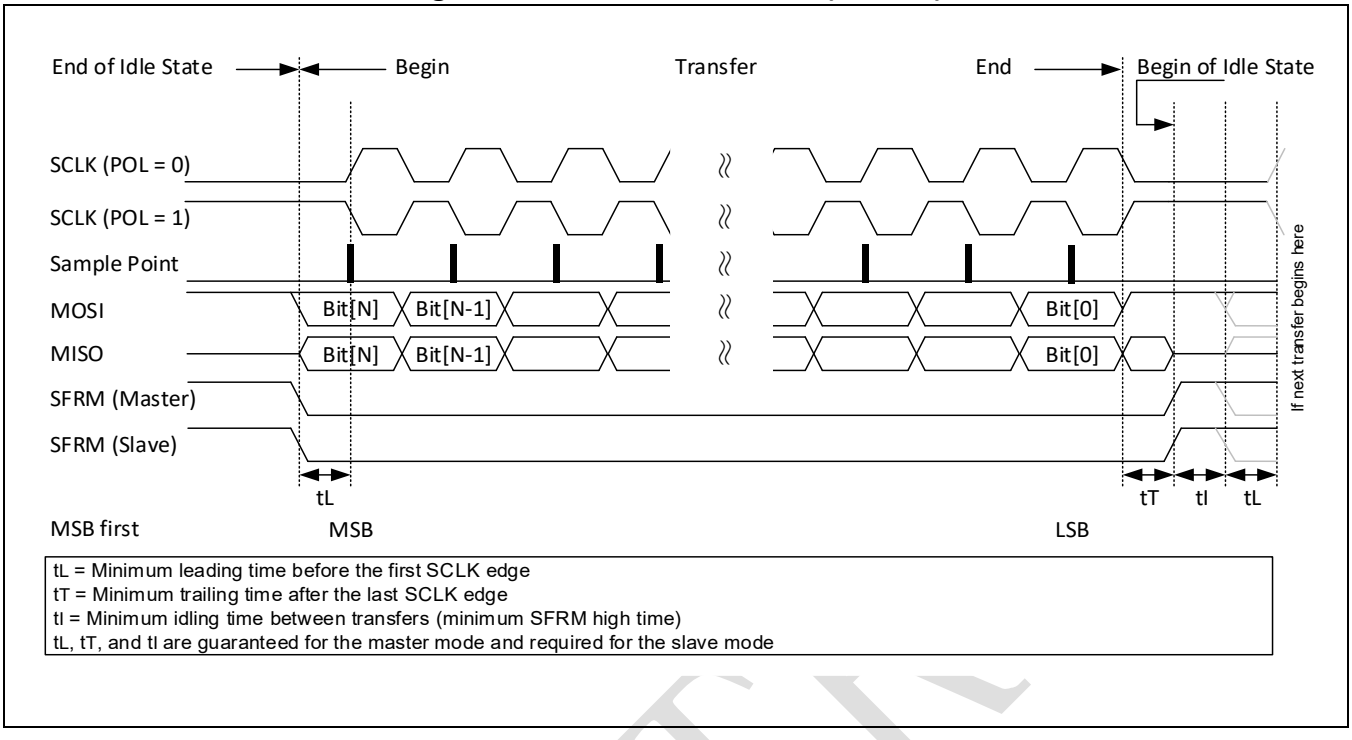
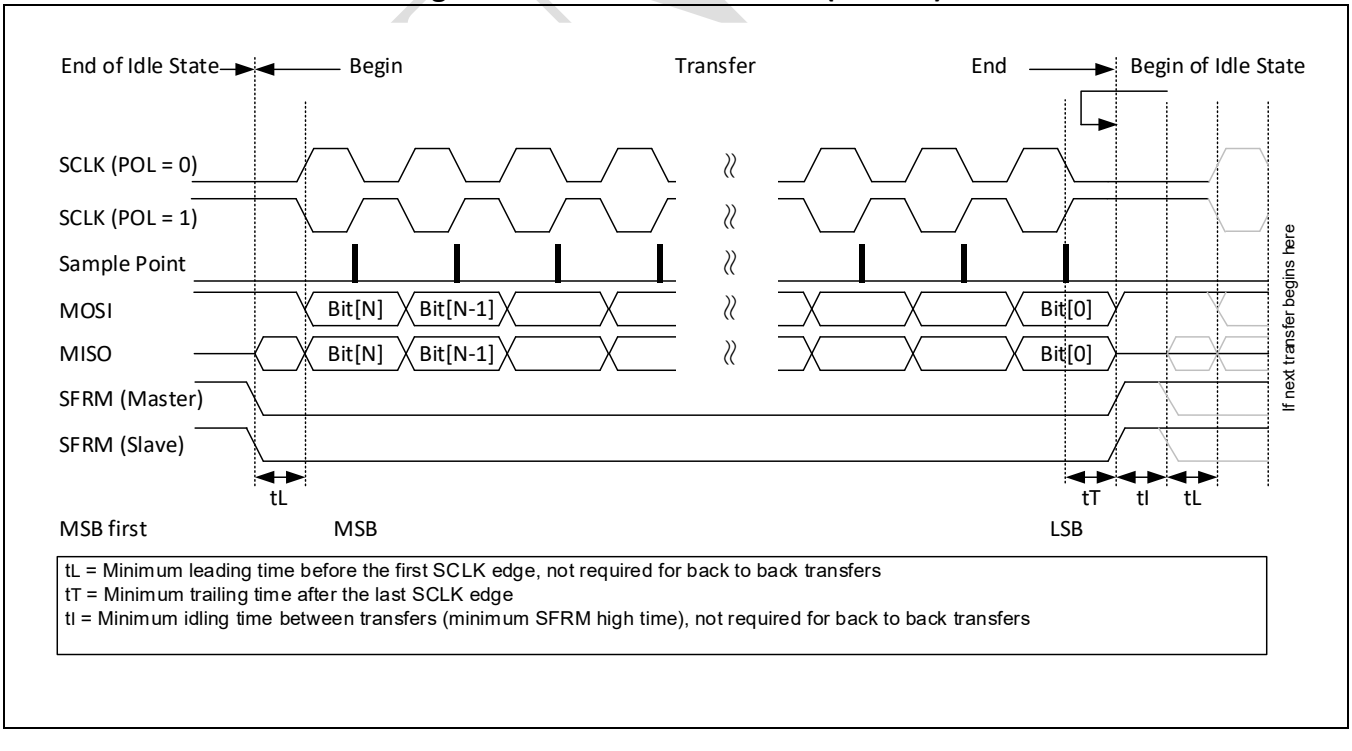
Figure 19-4: SSP clock format 0 (PHS = 0)



19.4.4.4 PHS = 1 frame format

When the SSP port is disabled or in idle mode, SFRM is high, MOSI and MISO is Hi-impedance, SCLK is low (SSPCTL1.CLKPOL = 0) or high (SSPCTL1.CLKPOL = 1). As shown in Figure 19-5.

Figure 19-5: SSP clock format 1 (PHS = 1)



When transmit data is ready to be sent and SSPCTL1.CLKPHS is low, the first SCLK edge is used to drive the first data bit for both master and slave. SFRM goes low (half clock period before the first edge of SCLK) and stay low during the transfer period. SFRM goes high again after last SCLK edge.

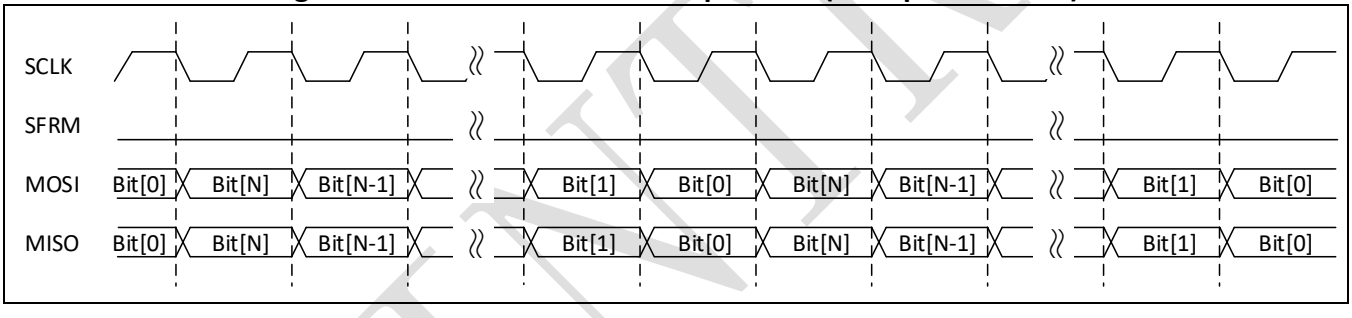
The MSB of the transmit data is driven onto MOSI/MISO on the first SCLK edge. The remainder bits of transmit data will be driven onto MOSI/MISO when the odd edge of SCLK occurred. And even edge of SCLK occurred will sample MOSI/MISO data bit and shift it into the LSB, MSB will be shift out and be latched for next edge driven onto MOSI/MISO. 1-32 bits can be transferred per frame.

19.4.4.5 Back to back mode

For back-to-back transfers, start and completion are like those of single transfer, but SFRM does not de-assert between words. Both transmitter and receiver are configured for the word length and internally track the start and end of frames. There is no “dead” bits and the LSB of one frame is followed immediately by the MSB of the next.

For enable back to back mode, be ensure that more than one data left in the TXFIFO when transfer data. If don’t want to use back to back mode, FIFO packed mode should be disabled, and TXFIFO should be empty before current data transfer finished.

Figure 19-6: Motorola SPI frame protocol (multiple transfers)



The SSP port can be either a master or a slave device, but the clock and frame direction must be the same. So the SSPCTL1.CLKDIR and SSPCTL1.FRMDIR fields must either both be set or cleared.

Note: The input clock to SSP port must not be active when SFRM is de-asserted. When the SSP port is slave to clock and frame, SSPCTL1.SLVCLKSEL must be set.

19.4.5 SSP interrupts

The SSP Status registers (SSPSTS) contain bits that signal overrun errors as well as the TXFIFO and RXFIFO service requests. Each of these hardware-detected events signals an interrupt request to the interrupt controller. SSPSTS also contains flags that indicate if the SSP port is actively transmitting data, if the TXFIFO is not full, and if the RXFIFO is not empty. A signal-interrupt signal is sent to the interrupt controller. These events can cause an interrupt request: end-of-chain, receiver time out, peripheral trailing byte, RXFIFO overrun, RXFIFO service request, and TXFIFO service request.

Bits that cause an interrupt request remain set until they are cleared by writing a 0b1 to each bit. Once a status bit is cleared, the interrupt is cleared. Read-write bits are called status bits (status bits are referred to as ‘sticky’; and once set by hardware, they can only be cleared by writing a 0b1 to each bit), read-only bits are called flags. Writing a 0b1 to a sticky status bit clears it, writing a 0b0 has no effect. Read-only flags are set to 0b1 and are cleared automatically to 0b0 by hardware, and writes have no

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effect. Some bits that cause interrupt requests have corresponding mask bits in the Control registers (SSPCTL0/ SSPCTL1).

All bits in SSPSTS are read-only except the RFOVF, TFUDF and RXTO, which are all read-write.

The reset state of read-write bits is 0b0 and all bits return to their reset state when SSPCTL0.EN bit is cleared.

SPINTROL

19.5 Registers

19.5.1 SSP register map

Table 19-2: SSP Module Base Address

Peripheral Module	Base Address
SSP	0x4000 5000

Table 19-3: SSP Register Map

Register	Offset	Description	Reset Value
SSPCTL0	0x00	SSP Control Register 0	0x00000000
SSPCTL1	0x04	SSP Control Register 1	0x00000000
SSPSTS	0x08	SSP Status Register	0x0000F004
SSPFRC	0x0C	SSP Interrupt Force Register	0x00000000
SSPDATA	0x10	SSP Data Register	0x00000000
SSPTO	0x28	SSP Time Out Register	0x00000000

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19.5.2 SSP registers

19.5.2.1 SSP Control Register 0 (SSPCTL0)

Table 19-4: SSP Control Register 0 (SSPCTL0) Layout

SSPCTL0 (SSP Control Register 0) Offset: 0x0 Default: 0x00000000 Access: SSP -> SSPCTL0.all							
31	30	29	28	27	26	25	24
RESERVED	RESERVED	FPACKEN	RESERVED		RESERVED		
23	22	21	20	19	18	17	16
TFINTMSK	RFINTMSK	RESERVED	ESIZESEL	RESERVED			
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
EN	RESERVED	FRMSEL		SIZESEL			

Table 19-5: SSP Control Register 0 (SSPCTL0) Field Description

Bits	Field Name	Type	Reset	Description
31	RESERVED_31	RW	0x0	Reserved
30	RESERVED_30	RO	0x0	Reserved
29	FPACKEN	RW	0x0	FIFO Packing Enable 0: Disable FIFO packing 1: Enable FIFO packing
28:27	RESERVED_28_27	RO	0x0	Reserved
26:24	RESERVED_26_24	RW	0x0	Reserved
23	TFINTMSK	RW	0x0	Transmit FIFO underflow interrupt mask 0: TFUDF events generate an SSP interrupt 1: TFUDF events do NOT generate an SSP interrupt
22	RFINTMSK	RW	0x0	Receive FIFO overflow interrupt mask 0: RFOVF events generate an SSP interrupt 1: RFOVF events do NOT generate an SSP interrupt
21	RESERVED_21	RO	0x0	Reserved
20	ESIZESEL	RW	0x0	Extended data size select 0: A 0 is pre-appended to the SIZESEL value to set the SIZESEL range from 1 to 16 bits 1: A 1 is pre-appended to the SIZESEL value to set the SIZESEL range from 17 to 32 bits
19:8	RESERVED_19_8	RO	0x0	Reserved
7	EN	RW	0x0	Synchronous serial port Enable 0: Disable SSP 1: Enable SSP

SPINTROL

Bits	Field Name	Type	Reset	Description
6	RESERVED_6	RO	0x0	Reserved
5:4	FRMSEL	RW	0x0	Frame format 00: Motorola Serial Peripheral Interface (SPI) 01: Texas Instruments Synchronous Serial Protocol (SSP) 1x: Invalid option
3:0	SIZESEL	RW	0x0	Data size select 0000: 1-bit if ESIZESEL=0 and 17-bit if ESIZESEL=1 0001: 2-bit if ESIZESEL=0 and 18-bit if ESIZESEL=1 0010: 3-bit if ESIZESEL=0 and 19-bit if ESIZESEL=1 0011: 4-bit if ESIZESEL=0 and 20-bit if ESIZESEL=1 0100: 5-bit if ESIZESEL=0 and 21-bit if ESIZESEL=1 0101: 6-bit if ESIZESEL=0 and 22-bit if ESIZESEL=1 0110: 7-bit if ESIZESEL=0 and 23-bit if ESIZESEL=1 0111: 8-bit if ESIZESEL=0 and 24-bit if ESIZESEL=1 1000: 9-bit if ESIZESEL=0 and 25-bit if ESIZESEL=1 1001: 10-bit if ESIZESEL=0 and 26-bit if ESIZESEL=1 1010: 11-bit if ESIZESEL=0 and 27-bit if ESIZESEL=1 1011: 12-bit if ESIZESEL=0 and 28-bit if ESIZESEL=1 1100: 13-bit if ESIZESEL=0 and 29-bit if ESIZESEL=1 1101: 14-bit if ESIZESEL=0 and 30-bit if ESIZESEL=1 1110: 15-bit if ESIZESEL=0 and 31-bit if ESIZESEL=1 1111: 16-bit if ESIZESEL=0 and 32-bit if ESIZESEL=1

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19.5.2.2 SSP Control Register 1 (SSPCTL1)

Table 19-6: SSP Control Register 1 (SSPCTL1) Layout

SSPCTL1 (SSP Control Register 1) Offset: 0x4 Default: 0x00000000
Access: SSP -> SSPCTL1.all

31	30	29	28	27	26	25	24
TXTRITIME	TXTRIEN	RESERVED	SLVCLKSEL	RESERVED		CLKDIR	FRMDIR
23	22	21	20	19	18	17	16
RXONLY	TRAIL	DMATXEN	DMARXEN	RESERVED	RESERVED		FRMINV
15	14	13	12	11	10	9	8
RESERVED	RESERVED	RFTH				TFTH	
7	6	5	4	3	2	1	0
TFTH		RESERVED	CLKPHS	CLKPOL	RESERVED	TFIE	RFIE

Table 19-7: SSP Control Register 1 (SSPCTL1) Field Description

Bits	Field Name	Type	Reset	Description
31	TXTRITIME	RW	0x0	TXD tri-stated enable time on last phase 0: SSP_TXD is tri-stated 1/2 clock cycle after the beginning of the LSB 1: SSP_TXD output signal is tri-stated on the clock edge that ends the LSB
30	TXTRIEN	RW	0x0	TXD Tri-stated enable 0: SSP_TXD output signal is not tri-stated 1: SSP_TXD is tri-stated when not transmitting data
29	RESERVED_29	RW	0x0	Reserved
28	SLVCLKSEL	RW	0x0	Slave clock free running control 0: Clock input to SSP_SCLK is not active when SSPCTL1.CLKDIR=1 (slave mode) 1: Clock input to SSP_SCLK is active when SSPCTL1.CLKDIR=1 (slave mode)
27:26	RESERVED_27_26	RO	0x0	Reserved
25	CLKDIR	RW	0x0	SSP Sclock (SSP_SCLK) direction 0: Master mode, SSP port drives SSP_SCLK 1: Slave mode, SSP port receives SSP_SCLK
24	FRMDIR	RW	0x0	SSP frame (SSP_SFRM) direction 0: Master mode, SSP port drives SSP_SFRM 1: Slave mode, SSP port receives SSP_SFRM
23	RXONLY	RW	0x0	Receive-only 0: Transmit/receive mode 1: Receive without transmit mode

SPINTROL

Bits	Field Name	Type	Reset	Description
22	TRAIL	RW	0x0	Trailing byte control 0: Trailing byte is handled by the CPU 1: Trailing byte is handled by the DMA
21	DMATXEN	RW	0x0	DMA transmit service request enable 0: Disable DMA transmit service request 1: Enable DMA transmit service request
20	DMARXEN	RW	0x0	DMA receive service request enable 0: Disable DMA receive service request 1: Enable DMA receive service request
19	RESERVED_19	RW	0x0	Reserved
18:17	RESERVED_18_17	RO	0x0	Reserved
16	FRMINV	RW	0x0	Invert frame signal 0: SSP_SFRM polarity is determined by the PSP polarity bit 1: SSP_SFRM polarity is inverted to the definition by PSP polarity bit
15	RESERVED_15	RW	0x0	Reserved
14	RESERVED_14	RW	0x0	Reserved
13:10	RFTH	RW	0x0	Threshold level at which RXFIFO asserts interrupt. Level should be set to the preferred threshold value minus 1.
9:6	TFTH	RW	0x0	Threshold level at which TXFIFO asserts interrupt. Level should be set to the preferred threshold value minus 1.
5	RESERVED_5	RO	0x0	Reserved
4	CLKPHS	RW	0x0	Motorola SPI SSP_SCLK phase setting 0: Start sampling data on the 1st SSP_SCLK edge after the start of a frame. 1: Start sampling data on the 2nd SSP_SCLK edge after the start of a frame.
3	CLKPOL	RW	0x0	Motorola SPI SSP_SCLK polarity setting 0: SSP_SCLK of inactive or idle state is low 1: SSP_SCLK of inactive or idle state is high
2	RESERVED_2	RW	0x0	Reserved
1	TFIE	RW	0x0	Transmit FIFO interrupt enable 0: Disable TXFIFO interrupt 1: Enable TXFIFO interrupt

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Bits	Field Name	Type	Reset	Description
0	RFIE	RW	0x0	Receive FIFO interrupt enable 0: Disable RXFIFO interrupt 1: Enable RXFIFO interrupt

SPINTROL

19.5.2.3 SSP Status Register (SSPSTS)

Table 19-8: SSP Status Register (SSPSTS) Layout

SSPSTS (SSP Status Register) Offset: 0x8 Default: 0x0000F004 Access: SSP -> SSPSTS.all							
31	30	29	28	27	26	25	24
RFODDSTS	TFODDSTS	RESERVED					
23	22	21	20	19	18	17	16
RESERVED	SLVCLKSTS	TFUDF	RESERVED	RXTO	RESERVED		
15	14	13	12	11	10	9	8
RFLVL				TFLVL			
7	6	5	4	3	2	1	0
RFOVF	RFS	TFS	BUSY	RNE	TNF	RESERVED	

Table 19-9: SSP Status Register (SSPSTS) Field Description

Bits	Field Name	Type	Reset	Description
31	RFODDSTS	RO	0x0	RX FIFO odd sample status This bit is used only when FIFO packing is enabled 0: RXFIFO entry has 2 samples 1: RXFIFO entry has 1 sample
30	TFODDSTS	RO	0x0	TX FIFO odd sample status Overall number of samples is TFLVL*2+TFODDSTS This bit is used only when FIFO packing is enabled 0: TXFIFO entry has a even number of samples 1: TXFIFO entry has an odd number of samples
29:24	RESERVED_29_24	RO	0x0	Reserved
23	RESERVED_23	RW	0x0	Reserved
22	SLVCLKSTS	RO	0x0	Slave clock status 0: The SSP port is ready for slave clock operations 1: The SSP port is currently busy synchronizing slave mode signals
21	TFUDF	RW	0x0	Transmit FIFO underflow 0: Read a 0 indicates no TXFIFO overflow. Write a 0 has no effect. 1: Read a 1 indicates data fetch from an empty TXFIFO was attempted. Write a 1 clears the latched flag.
20	RESERVED_20	RO	0x0	Reserved

SPINTROL

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Bits	Field Name	Type	Reset	Description
19	RXTO	RW	0x0	Receiver time-out 0: Read a 0 indicates no time-out on receiving. Write a 0 has no effect. 1: Read a 1 indicates time-out on receiving. Write a 1 clears the latched flag.
18:16	RESERVED_18_16	RO	0x0	Reserved
15:12	RFLVL	RO	0xF	Receive FIFO level The value is number of entries minus one in RXFIFO.
11:8	TFLVL	RO	0x0	Transmit FIFO level The value is number of entries in TXFIFO.
7	RFOVF	RW	0x0	Receive FIFO overflow 0: Read a 0 indicates no receive FIFO overflow. Write a 0 has no effect. 1: Read a 1 indicates data put to a full RXFIFO was attempted. Write a 1 clears the latched flag.
6	RFS	RO	0x0	Receive FIFO service request 0: RXFIFO level is at or below RXFIFO threshold (RFTH), or SSP port is disabled 1: RXFIFO level exceeds RXFIFO threshold (RFTH)
5	TFS	RO	0x0	Transmit FIFO service request 0: TXFIFO level exceeds the threshold (TFTH + 1), or SSP port disabled 1: TXFIFO level is at or below threshold (TFTH + 1)
4	BUSY	RO	0x0	SSP busy 0: SSP port is idle or disabled 1: SSP port is currently transmitting or receiving framed data
3	RNE	RO	0x0	Receive FIFO not empty 0: RXFIFO is empty 1: RXFIFO is not empty
2	TNF	RO	0x1	Transmit FIFO not full 0: TXFIFO is full 1: TXFIFO is not full
1:0	RESERVED_1_0	RO	0x0	Reserved

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19.5.2.4 SSP Interrupt Force Register (SSPFRC)

Table 19-10: SSP Interrupt Force Register (SSPFRC) Layout

SSPFRC (SSP Interrupt Test Register) Offset: 0xC Default: 0x00000000 Access: SSP -> SSPFRC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RFOVF	RFREQ	TFREQ	RESERVED				

Table 19-11: SSP Interrupt Force Register (SSPFRC) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	RFOVF	RW	0x0	Force RXFIFO overrun (Non-maskable) 0: Write a 0 release the force 1: Write a 1 forces a RXFIFO overflow interrupt This bit needs to be cleared manually
6	RFREQ	RW	0x0	Force RXFIFO service request (Non-maskable) 0: Write a 0 release the force 1: Write a 1 forces a RXFIFO service request This bit needs to be cleared manually
5	TFREQ	RW	0x0	Force TXFIFO service request (Non-maskable) 0: Write a 0 release the force 1: Write a 1 forces a TXFIFO service request This bit needs to be cleared manually
4:0	RESERVED_4_0	RO	0x0	Reserved

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19.5.2.5 SSP Data Register (SSPDATA)

Table 19-12: SSP Data Register (SSPDATA) Layout

SSPDATA (SSP Data Register) Offset: 0x10 Default: 0x00000000 Access: SSP -> SSPDATA.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 19-13: SSP Data Register (SSPDATA) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Data to be written to the TXFIFO or read from the RXFIFO

19.5.2.6 SSP Time Out Register (SSPTO)

Table 19-14: SSP Time Out Register (SSPTO) Layout

SSPTO (SSP Time Out Register) Offset: 0x28 Default: 0x00000000 Access: SSP -> SSPTO.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 19-15: SSP Time Out Register (SSPTO) Field Description

Bits	Field Name	Type	Reset	Description
31:24	RESERVED_31_24	RO	0x0	Reserved
23:0	VAL	RW	0x0	Timeout interval defined as t_CLK_SPI*(SSPTO+1).

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20 Flash memory

20.1 Features

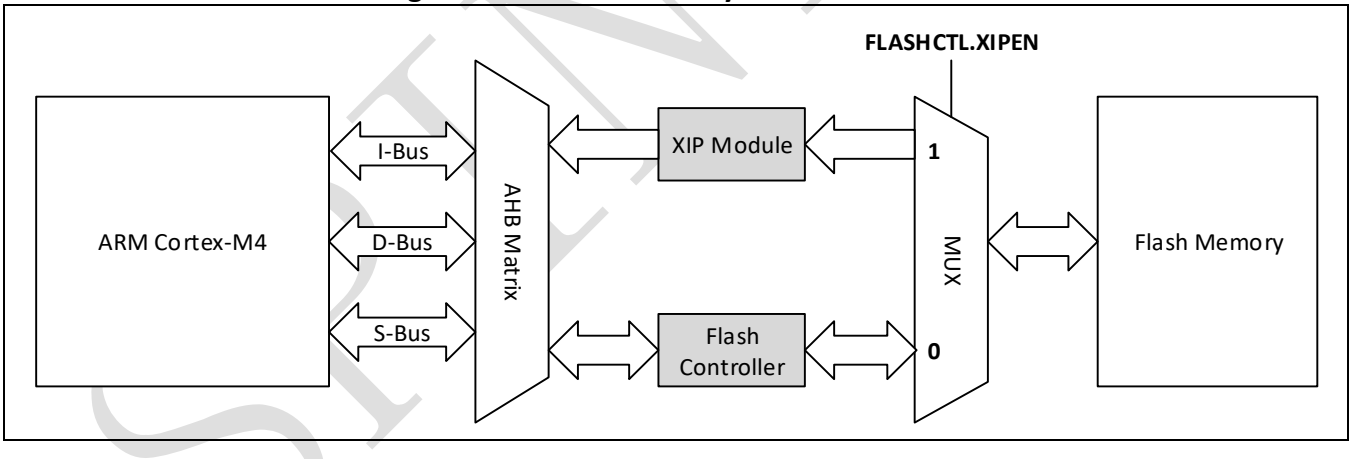
The SPC2168 Flash memory module has the following key features:

- Up to 512KB on-chip Flash memory
- Memory organization:
  - Main Memory Block: with total 1024 sectors; 128 x 32 bits per sector
  - NVR Memory Block: with total 2 sectors; 128 x 32 bits per sector
- Program/Sector Erase cycles: minimum 100,000 cycles @ T_J=85°C
- Data retention period: greater than 10 years @ T_J=85°C
- ECC (Error Checking and Correction) checking

Flash memory interface features:

- Read interface with XIP (Execute-In-Place) module
- Flash controller for Read/Program/Erase operation
- Read/Write protection
- Multi-zone protection

Figure 20-1: Flash memory access interfaces



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20.2 Flash module organization

The flash memory organization is based on a main memory block containing 1024 sectors of 128 word and a NVR block containing 2 sectors of 128 word as shown in Figure 20-2 and

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Table 20-1.

The flash memory is organized as 32-bit wide memory cells that can be used for storing both code and data constants.

The NVR memory block is divided into two parts:

- OTP memory – The area can be configured as OTP memory by programming the first word cell with data 0x4C4F434B. Otherwise, the area is just used as normal data memory.
- Configuration Words – The area contains the word data for multi-zone security setting.

Write operation to the main memory block and the NVR memory block are managed by the Flash Controller as shown in Figure 20-1. The high voltage needed for Program/Erase operations is internally generated.

The main Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

- Sector Write Protection
- Read Protection

Note: For operations on the Flash memory through Flash Controller, the XIP module should be disabled first (FLASHCTL.XIPEN = 0).

Figure 20-2: Logical structure of the Flash module

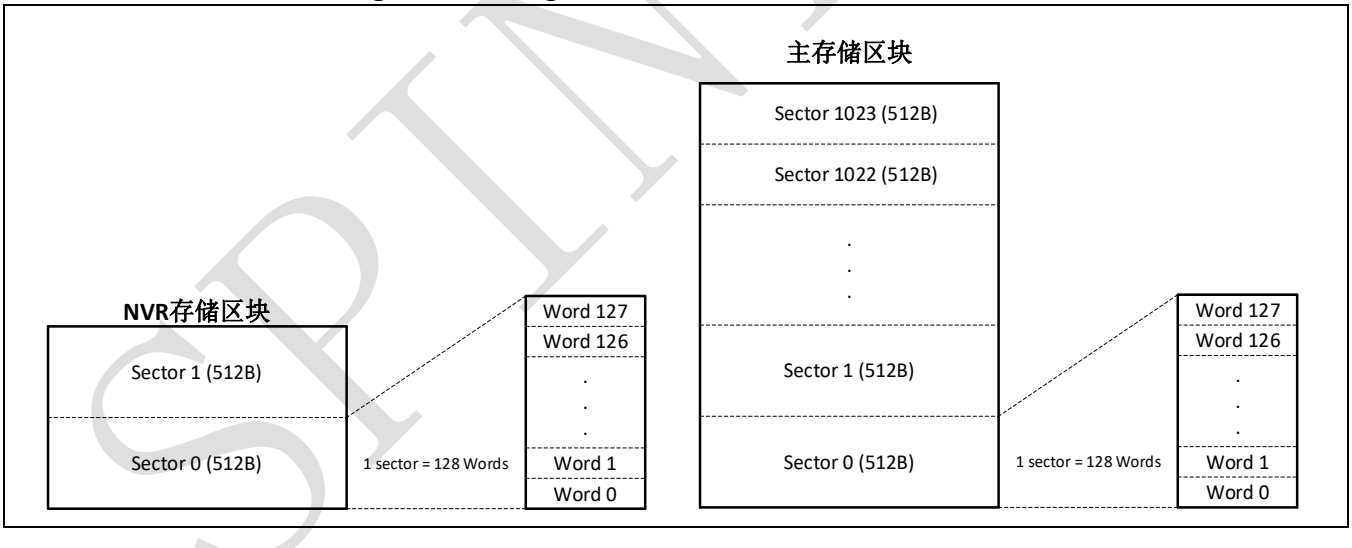

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Table 20-1: Flash module organization

Block	Name	Base address	Size
Main Memory	Sector 0	0x1000 0000	512 bytes
	Sector 1	0x1000 0200	512 bytes
	Sector 2	0x1000 0400	512 bytes
	Sector 3	0x1000 0600	512 bytes
	……	……	……
	Sector 1023	0x1007 FE00	512 bytes
NVR Memory	OTP memory	0x11000400	128 Words
	Configuration Words	0x11000600	128 Words
Flash memory interface registers	FLASHCTL	0x4000 8800	4 bytes
	FLASHADDR	0x4000 8804	4 bytes
	FLASHDIN	0x4000 8808	4 bytes
	FLASHDOUT	0x4000 880C	4 bytes
	Reserved	0x4000 8810	28 bytes
	FLASHWP0	0x4000 882C	4 bytes
	FLASHWP1	0x4000 8830	4 bytes
	FLASHWP2	0x4000 8834	4 bytes
	FLASHWP3	0x40008838	4 bytes
	FLASHREGKEY	0x4000 883C	4 bytes

20.3 Read operation

The CPU can read data from the embedded Flash module through the XIP module or the Flash Controller.

20.3.1 Read through XIP module

Through the XIP module, the flash memory can be addressed directly, as a common memory space. The main task of the XIP module is to generate the control signals to read from the flash memory. The Cortex-M4 can use the XIP module to fetch the instruction over the I-Code bus and the literal pool (constant/data) over the D-Code bus.

Read accesses may be performed with latency. The latency is the number of wait states for a read operation on-the-fly. The wait states represent the ratio of the SYSCLK (system clock) period to the Flash memory access time. Please see Table 20-2 for details.

Table 20-2: Flash memory read access latency

System Clock Frequency	Wait States
0 < SYSCLK ≤ 25 MHz	0
25 MHz < SYSCLK ≤ 50 MHz	1
50 MHz < SYSCLK ≤ 75 MHz	2
75 MHz < SYSCLK ≤ 100 MHz	3
100 MHz < SYSCLK ≤ 125 MHz	4
125 MHz < SYSCLK ≤ 150 MHz	5
150 MHz < SYSCLK ≤ 175 MHz	6
175 MHz < SYSCLK ≤ 200 MHz	7

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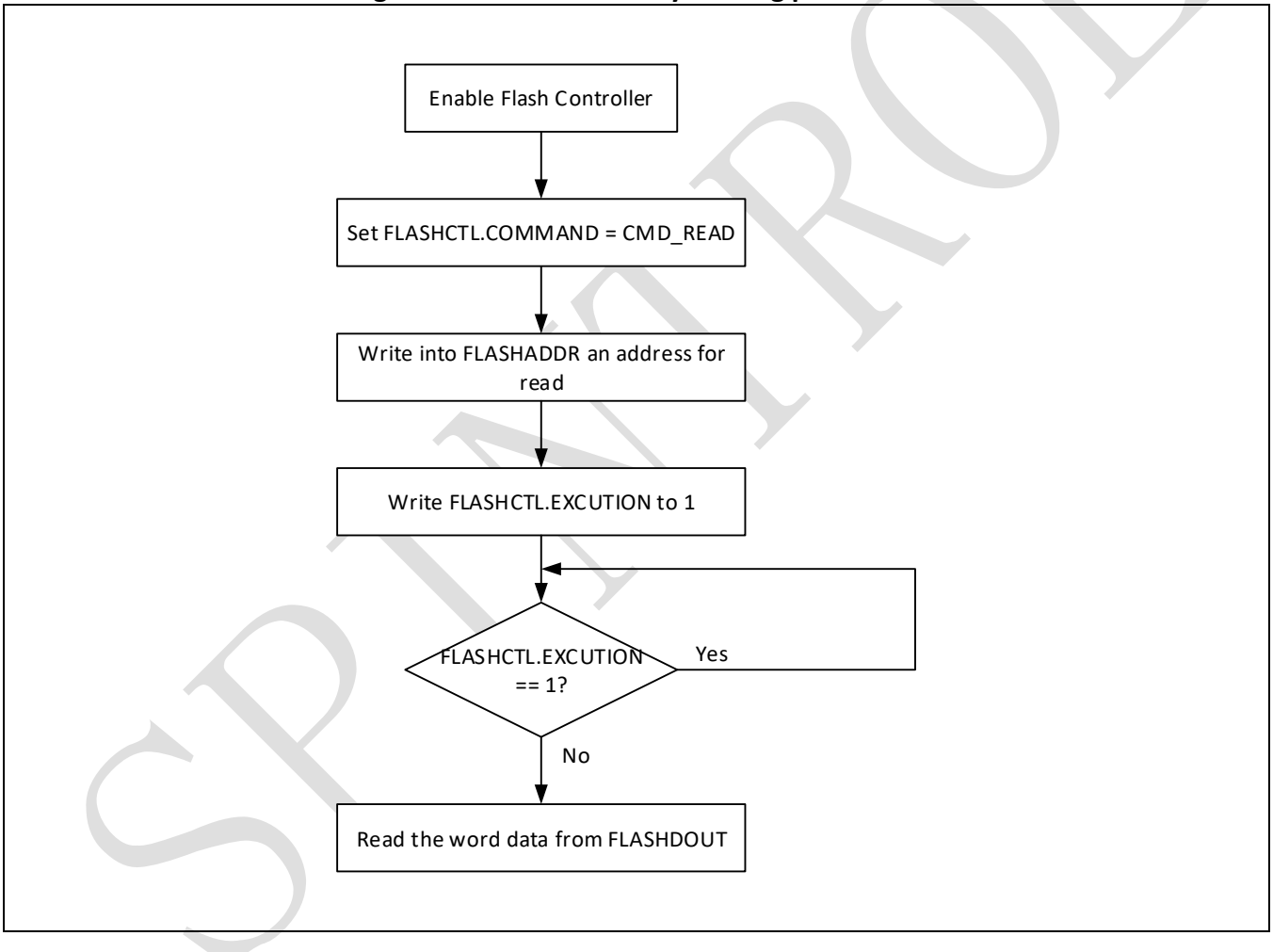
20.3.2 Read through Flash Controller

The CPU can also read a word data at a time from the Flash memory through the Flash Controller. The reading sequence is as follows:

- Set the COMMAND bits in the FLASHCTL register with CMD_READ
- Set the FLASHADDR register to select a memory cell to read
- Set the EXCUTION bit in the FLASHCTL register
- Wait for the EXCUTION bit to be reset
- Read the word data from the FLASHDOUT register

Figure 20-3: Flash memory reading procedure



20.4 Program and erase operation

The Flash Controller handles the program and erase operations of the flash memory. The Flash Controller consists of nine 32-bit registers.

- Flash control register (FLASHCTL)
- Flash address register (FLASHADDR)
- Flash input data register (FLASHDIN)

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- Flash output data register (FLASHDOUT)
- Flash write protection registers (FLASHWP0 ~ FLASHWP3)
- Flash unlock key register (FLASHREGKEY)

20.4.1 Enable Flash controller

After reset, the Flash controller is disabled. The Flash controller can be enabled by setting FLASHCTL.XIPEN to 0. However, the FLASHCTL register is write-protected. An unlock key value (0x1ACCE551) should be written to the FLASHREGKEY register to enable the write access to the protected registers.

20.4.2 Flash memory programming

The Flash memory can be programmed 32 bits (a word) at a time. The Flash memory programming sequence is as follows:

- Set the COMMAND bits in the FLASHCTL register with CMD_PROG_WD
- Set the FLASHADDR register to select a memory cell to program
- Set the EXCUTION bit in the FLASHCTL register and then check whether the bit value was set
- Wait for the DATAACCEPT bit in the FLASHCTL register to be set
- Write the word data to the FLASHDIN register
- Wait for the EXCUTION bit to be reset

If the addressed main Flash memory location is write-protected by the FLASHWPx register, the EXCUTION bit could not be set and the program operation is skipped.

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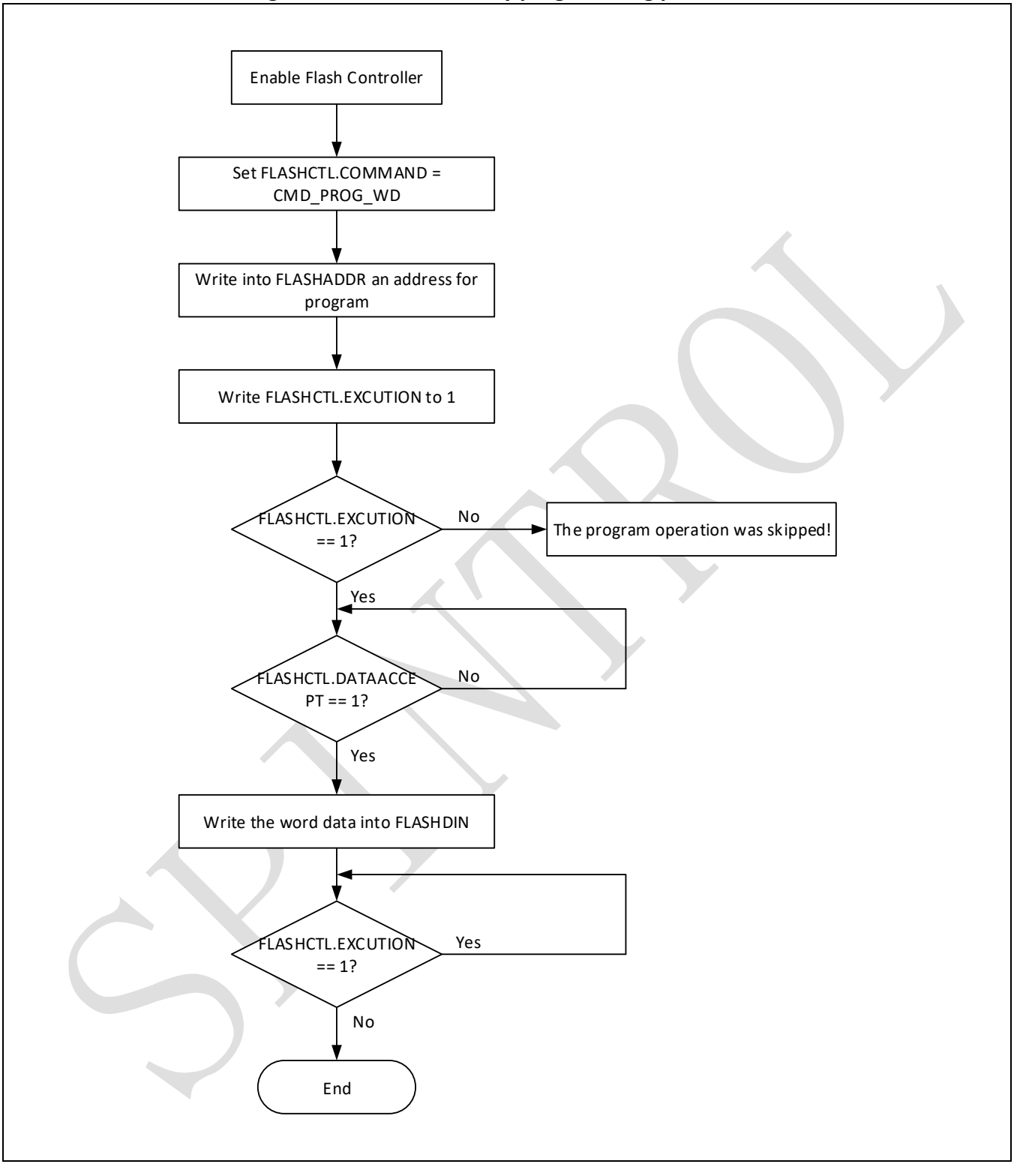
Figure 20-4: Flash memory programming procedure



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20.4.3 Flash memory erase

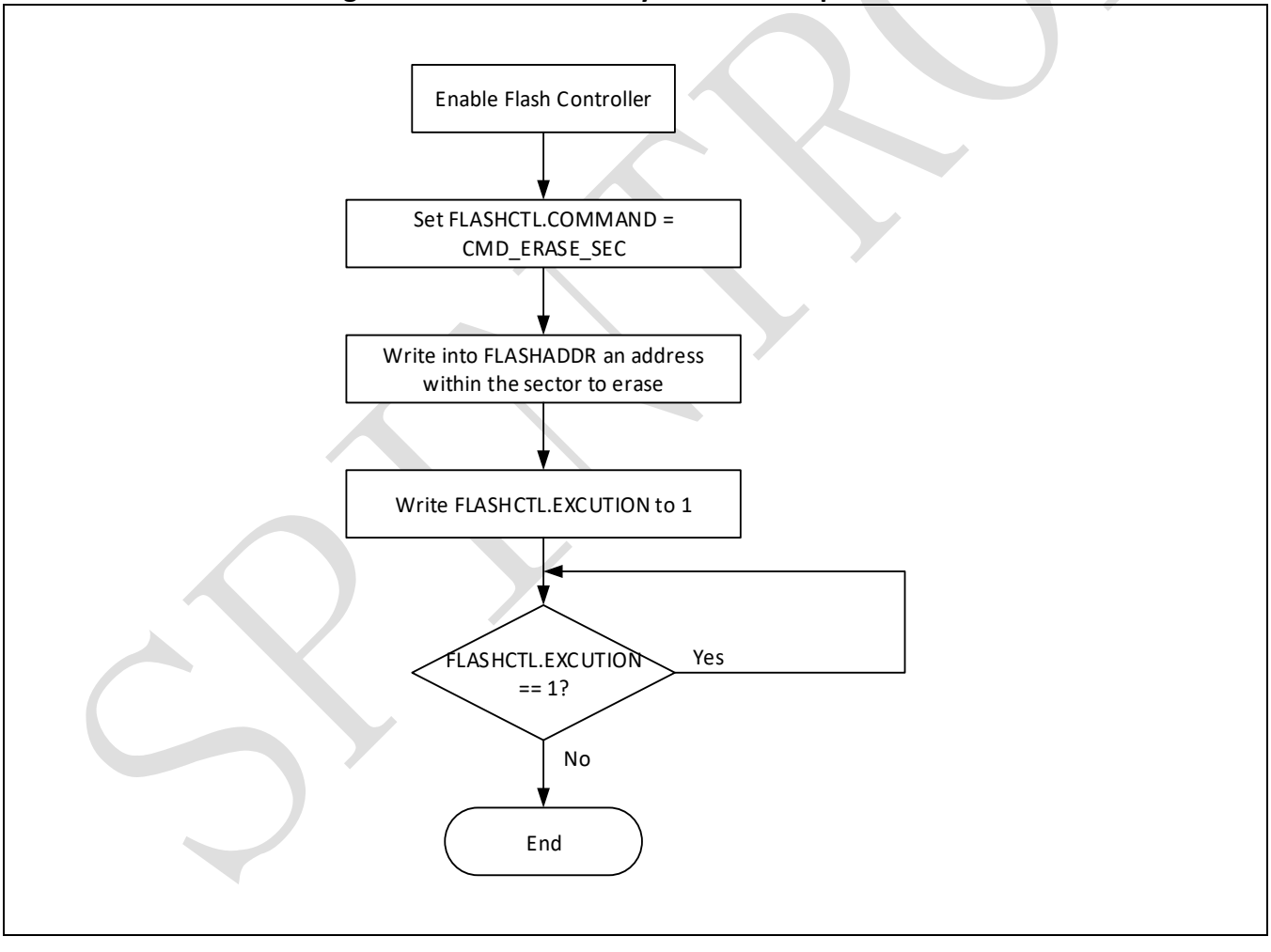
The main Flash memory can be erased by sector or completely (Chip Erase). And the NVR memory can only be erased by sector.

Sector Erase

A sector of the Flash memory can be erased using the Sector Erase feature of the Flash Controller. To erase a sector, the procedure below should be followed:

- Set the COMMAND bits in the FLASHCTL register with CMD_ERASE_SEC
- Set the FLASHADDR register to select a sector to erase
- Set the EXCUTION bit in the FLASHCTL register
- Wait for the EXCUTION bit to be reset

Figure 20-5: Flash memory Sector Erase procedure



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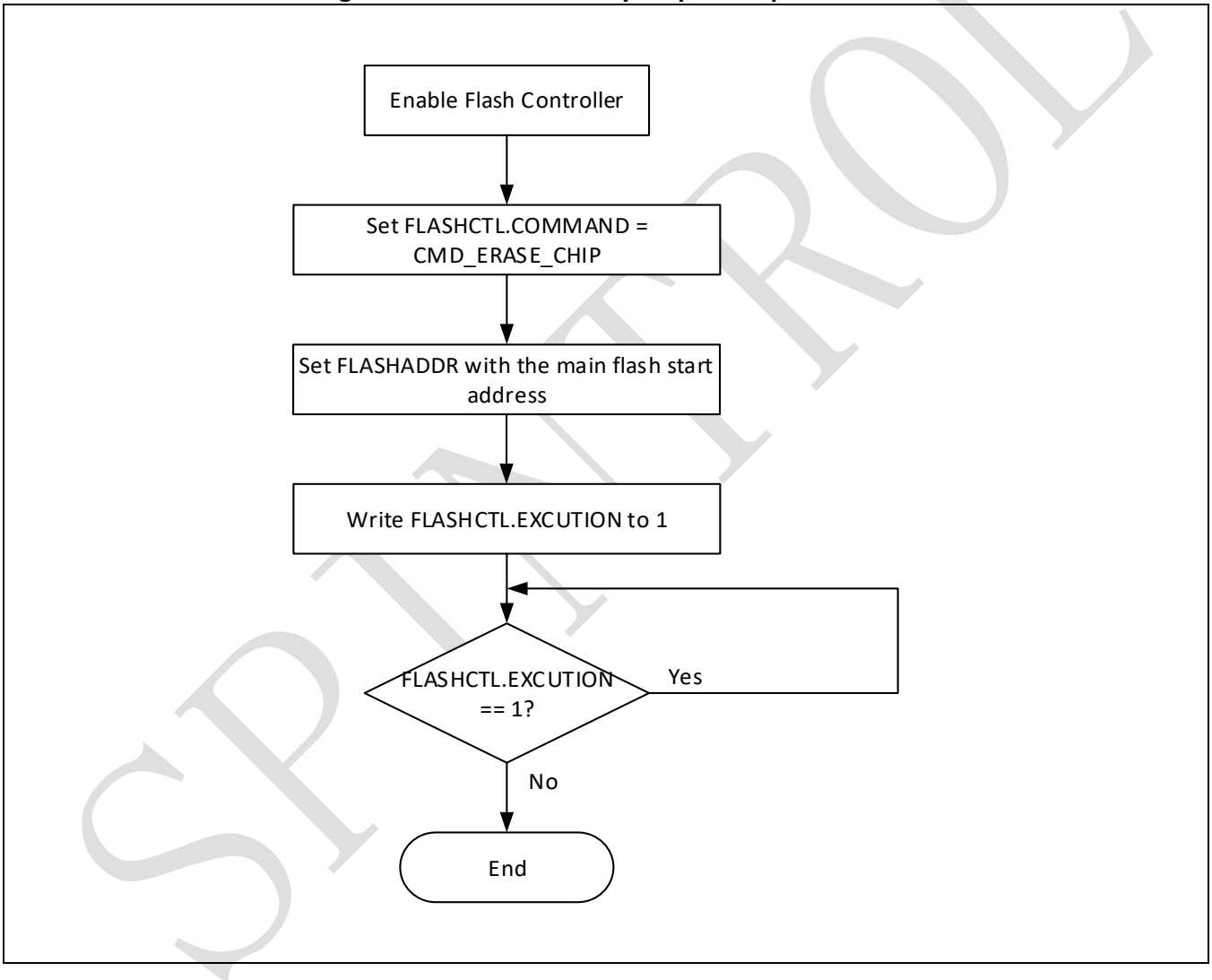
Chip Erase

The Chip Erase command can be used to completely erase all the sectors of the main Flash memory. The NVR memory block is not affected by this procedure. The following sequence is recommended:

- Set the COMMAND bits in the FLASHCTL register with CMD_ERASE_CHIP
- Set the FLASHADDR register with the main flash start address
- Set the EXCUTION bit in the FLASHCTL register
- Wait for the EXCUTION bit to be reset

Figure 20-6: Flash memory Chip Erase procedure



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20.5 Protections

20.5.1 Multi-zone protection

The main Flash memory can be organized into four code space segments (Flash zones). The multi-zone protection technology provides an advanced code protection scheme to help multiple users securely share resources on a single chip. Once a Flash zone protection has been enabled:

- Access to the Flash zone from other Flash zones is limited severely. The code running in other Flash zones can only jump to or call a routine in the protected Flash zone and the read/program/erase operations on the protected Flash zone are completely disabled.
- Access to the Flash zone through the debug interface is not allowed.

The multi-zone protection is activated by setting the Configuration Words in the NVR memory block and then, by applying a system reset to reload the new Configuration Words.

To disable the multi-zone protections:

- Erase the entire Configuration Words area (sector). As a result, the Configuration Words will be 0xFFFFFFFF. At this stage, the multi-zone protections are still enable.
- Reset the device to reload the Configuration Words and, to disable the multi-zone protection.

Note: The multi-zone protection feature doesn't include DRAM.
Erasing the Configuration Words area will automatically trigger a Chip Erase of the main Flash memory.

20.5.2 Write protection

The sectors of the main Flash memory can be protected against unwanted write due to loss of program counter contexts. The write protection is implemented with a granularity of one sector at a time. If a program or an erase operation is performed on a protected sector, the operation will be skipped.

The write protection is activated by set the FLASHWPx register bits and reset the register bits will disable the write protection.

20.6 Setup Flash timing

There are physically timing requirements for the Flash to avoid malfunction. It is a list of absolute values for the timing relationship of a series of events. An finite state machine (FSM) is designed in both the XIP module and the Flash controller, which guarantee the timing based on couting clock cycles with a list of timeout counts. For the ease of usage, a function is provide in the SDK named FLASH_SetTiming. It takes the frequency of CPU clock (HCLK) as input parameter and automatically sets all the timeout counts.

Whenever user plans to increase the HCLK frequency, FLASH_SetTiming should be called before the actual change of the HCLK due to the increased timeout counts requirement.

Whenever user plans to decrease the HCLK frequency, FLASH_SetTiming should be called after the actual change of the HCLK due to the decreased timeout counts requirement.

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20.7 Configuration Words description

There are twenty-eight Configuration Words, seven for each zone. They are configured by the end user depending on the application requirements.

The organization and description of these Configuration Words are as shown in Table 20-3. The Configuration Words can be read from the memory locations listed in Table 20-3 through the Flash Controller. The new programmed Configuration Words are loaded after a system reset.

Table 20-3: Organization and description of the Configuration Words

Address	Name	Description
0x11000600	ZONE0_INFO_LOCK	Lock the Configuration Words of zone 0 (0x11000600 – 0x1100063F) 0xFFFFFFFF: The Configuration Words of zone 0 can be programmed Others: The Configuration Words of zone 0 can not be programmed
0x11000604	ZONE0_ENCRYPT	Encrypt status of code in Flash zone 0 0xDEC0DE: The code in Flash zone 0 has been encrypted Others: The code in Flash zone 0 is raw code
0x11000608	ZONE0_DECRYPT	Decrypt status of code in Flash zone 0 0xAA621623: Success to decrypt code in Flash zone 0 0x1E55051: Fail to decrypt code in Flash zone 0 Others: Not valid
0x1100060C	ZONE0_FLASH_PROT	Flash zone 0 protection word 0xFFFFFFFF: Disable Flash zone 0 protection Others: Enable Flash zone 0 protection
0x11000610	ZONE0_FLASH_ADDR	Flash zone 0 start address
0x11000614	ZONE0_RAM_PROT	RAM zone 0 protection word 0xFFFFFFFF: Disable RAM zone 0 protection Others: Enable RAM zone 0 protection
0x11000618	ZONE0_RAM_ADDR	RAM zone 0 start address
0x1100061C~0x1100063F	Reserved for ZONE0	Reserved Configuration Words for ZONE 0
0x11000640	ZONE1_INFO_LOCK	Lock the Configuration Words of zone 1 (0x11000640 – 0x1100067F) 0xFFFFFFFF: The Configuration Words of zone 1 can be programmed Others: The Configuration Words of zone 1 can not be programmed
0x11000644	ZONE1_ENCRYPT	Encrypt status of code in Flash zone 1 0xDEC0DE: The code in Flash zone 1 has been encrypted Others: The code in Flash zone 1 is raw code
0x11000648	ZONE1_DECRYPT	Decrypt status of code in Flash zone 1 0xAA621623: Success to decrypt code in Flash zone 1 0x1E55051: Fail to decrypt code in Flash zone 1 Others: Not valid
0x1100064C	ZONE1_FLASH_PROT	Flash zone 1 protection word 0xFFFFFFFF: Disable Flash zone 1 protection Others: Enable Flash zone 1 protection
0x11000650	ZONE1_FLASH_ADDR	Flash zone 1 start address

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Address	Name	Description
0x11000654	ZONE1_RAM_PROT	RAM zone 1 protection word 0xFFFFFFFF: Disable RAM zone 1 protection Others: Enable RAM zone 1 protection
0x11000658	ZONE1_RAM_ADDR	RAM zone 1 start address
0x1100065C~0x1100067F	Reserved for ZONE1	Reserved Configuration Words for ZONE 1
0x11000680	ZONE2_INFO_LOCK	Lock the Configuration Words of zone 2 (0x11000680 – 0x110006BF) 0xFFFFFFFF: The Configuration Words of zone 2 can be programmed Others: The Configuration Words of zone 2 can not be programmed
0x11000684	ZONE2_ENCRYPT	Encrypt status of code in Flash zone 2 0xDEC0DE: The code in Flash zone 2 has been encrypted Others: The code in Flash zone 2 is raw code
0x1100688	ZONE2_DECRYPT	Decrypt status of code in Flash zone 2 0xAA621623: Success to decrypt code in Flash zone 2 0x1E55051: Fail to decrypt code in Flash zone 2 Others: Not valid
0x1100068C	ZONE2_FLASH_PROT	Flash zone 2 protection word 0xFFFFFFFF: Disable Flash zone 2 protection Others: Enable Flash zone 2 protection
0x11000690	ZONE2_FLASH_ADDR	Flash zone 2 start address
0x11000694	ZONE2_RAM_PROT	RAM zone 2 protection word 0xFFFFFFFF: Disable RAM zone 2 protection Others: Enable RAM zone 2 protection
0x11000698	ZONE2_RAM_ADDR	RAM zone 2 start address
0x1100069C~0x110006BF	Reserved for ZONE2	Reserved Configuration Words for ZONE 2
0x110006C0	ZONE3_INFO_LOCK	Lock the Configuration Words of zone 3 (0x110006C0 – 0x110006FF) 0xFFFFFFFF: The Configuration Words of zone 3 can be programmed Others: The Configuration Words of zone 3 can not be programmed
0x110006C4	ZONE3_ENCRYPT	Encrypt status of code in Flash zone 3 0xDEC0DE: The code in Flash zone 3 has been encrypted Others: The code in Flash zone 3 is raw code
0x110006C8	ZONE3_DECRYPT	Decrypt status of code in Flash zone 3 0xAA621623: Success to decrypt code in Flash zone 3 0x1E55051: Fail to decrypt code in Flash zone 3 Others: Not valid
0x110006CC	ZONE3_FLASH_PROT	Flash zone 3 protection word 0xFFFFFFFF: Disable Flash zone 3 protection Others: Enable Flash zone 3 protection
0x110006D0	ZONE3_FLASH_ADDR	Flash zone 3 start address
0x110006D4	ZONE3_RAM_PROT	RAM zone 3 protection word 0xFFFFFFFF: Disable RAM zone 3 protection Others: Enable RAM zone 3 protection
0x110006D8	ZONE3_RAM_ADDR	RAM zone 3 start address

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Address	Name	Description
0x110006DC~0x110006FF	Reserved for ZONE3	Reserved Configuration Words for ZONE 3
0x11000700	WDT_ENABLE	Watchdog enable word 0xFFFFFFFF: Disable watchdog when chip start-up Others: Enable watchdog when chip start-up
0x11000704	CACHE_ENABLE	Flash cache enable word 0x1ACCE551: Enable Flash cache when chip start-up Others: Disable Flash cache when chip start-up
0x11000708~0x110007FF	Reserved	Not used

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20.8 Registers

20.8.1 Flash register map

Table 20-4: Flash Module Base Address

Peripheral Module	Base Address
FLASH	0x4000 8800

Table 20-5: Flash Register Map

Register	Offset	Description	Reset Value
FLASHCTL*	0x00	Flash Control Register	0x00000000
FLASHADDR	0x04	Flash Address Register	0x00000000
FLASHDIN	0x08	Flash Data Input Register	0x00000000
FLASHDOUT	0x0C	Flash Data Output Register	0x00000000
FLASHWP0*	0x2C	Flash Write Protect Register 0	0x00000000
FLASHWP1*	0x30	Flash Write Protect Register 1	0x00000000
FLASHWP2*	0x34	Flash Write Protect Register 2	0x00000000
FLASHWP3*	0x38	Flash Write Protect Register 3	0x00000000
FLASHREGKEY	0x3C	Flash Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the FLASHREGKEY=0x1ACCE551.

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20.8.2 Flash registers

20.8.2.1 Flash Control Register (FLASHCTL)

Table 20-6: Flash Control Register (FLASHCTL) Layout

FLASHCTL (Flash Control Register) Offset: 0x0 Default: 0x00000000 Access: FLASH -> FLASHCTL.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
WITHCACHE	XIPEN	EXECUTION	DATAACCEPT	COMMAND			

Table 20-7: Flash Control Register (FLASHCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:8	RESERVED_31_8	RO	0x0	Reserved
7	WITHCACHE	RO	0x0	XIP module cache option 0: XIP cache is not available 1: XIP cache is available
6	XIPEN	RW	0x0	XIP module enable 0: Disable XIP module 1: Enable XIP module
5	EXECUTION	RW	0x0	Command is in execution 0: FLASH FSM is in idle state 1: FLASH FSM is in execution
4	DATAACCEPT	RO	0x0	FLASHDIN shoud not be changed when this bit is 0
3:0	COMMAND	RW	0x0	Flash command 0001: Read 0101: Program word 1000: Erase sector 1010: Erase chip

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20.8.2.2 Flash Address Register (FLASHADDR)

Table 20-8: Flash Address Register (FLASHADDR) Layout

FLASHADDR (Flash Address Register) Offset: 0x4 Default: 0x00000000 Access: FLASH -> FLASHADDR.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 20-9: Flash Address Register (FLASHADDR) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Flash address

20.8.2.3 Flash Data Input Register (FLASHDIN)

Table 20-10: Flash Data Input Register (FLASHDIN) Layout

FLASHDIN (Flash Data Input Register) Offset: 0x8 Default: 0x00000000 Access: FLASH -> FLASHDIN.all							
31	30	29	28	27	26	25	24
FLASHDIN							
23	22	21	20	19	18	17	16
FLASHDIN							
15	14	13	12	11	10	9	8
FLASHDIN							
7	6	5	4	3	2	1	0
FLASHDIN							

Table 20-11: Flash Data Input Register (FLASHDIN) Field Description

Bits	Field Name	Type	Reset	Description
31:0	FLASHDIN	RW	0x0	Flash input data

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20.8.2.4 Flash Data Output Register (FLASHDOUT)

Table 20-12: Flash Data Output Register (FLASHDOUT) Layout

FLASHDOUT (Flash Data Output Register) Offset: 0xC Default: 0x00000000 Access: FLASH -> FLASHDOUT.all							
31	30	29	28	27	26	25	24
FLASHDOUT							
23	22	21	20	19	18	17	16
FLASHDOUT							
15	14	13	12	11	10	9	8
FLASHDOUT							
7	6	5	4	3	2	1	0
FLASHDOUT							

Table 20-13: Flash Data Output Register (FLASHDOUT) Field Description

Bits	Field Name	Type	Reset	Description
31:0	FLASHDOUT	RO	0x0	Flash output data

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20.8.2.5 Flash Write Protect Register 0 (FLASHWP0)

Table 20-14: Flash Write Protect Register 0 (FLASHWP0) Layout

FLASHWP0 (Flash Write Protect Register 0) Offset: 0x2C Default: 0x00000000 Access: FLASH -> FLASHWP0.all							
31	30	29	28	27	26	25	24
UNIT31	UNIT30	UNIT29	UNIT28	UNIT27	UNIT26	UNIT25	UNIT24
23	22	21	20	19	18	17	16
UNIT23	UNIT22	UNIT21	UNIT20	UNIT19	UNIT18	UNIT17	UNIT16
15	14	13	12	11	10	9	8
UNIT15	UNIT14	UNIT13	UNIT12	UNIT11	UNIT10	UNIT9	UNIT8
7	6	5	4	3	2	1	0
UNIT7	UNIT6	UNIT5	UNIT4	UNIT3	UNIT2	UNIT1	UNIT0

Table 20-15: Flash Write Protect Register 0 (FLASHWP0) Field Description

Bits	Field Name	Type	Reset	Description
31	UNIT31	RW	0x0	Write protection for flash unit 31 (0x1001_F000 → 0x1001_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
30	UNIT30	RW	0x0	Write protection for flash unit 30 (0x1001_E000 → 0x1001_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
29	UNIT29	RW	0x0	Write protection for flash unit 29 (0x1001_D000 → 0x1001_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
28	UNIT28	RW	0x0	Write protection for flash unit 28 (0x1001_C000 → 0x1001_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
27	UNIT27	RW	0x0	Write protection for flash unit 27 (0x1001_B000 → 0x1001_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
26	UNIT26	RW	0x0	Write protection for flash unit 26 (0x1001_A000 → 0x1001_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
25	UNIT25	RW	0x0	Write protection for flash unit 25 (0x1001_9000 → 0x1001_9FFF)

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Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
24	UNIT24	RW	0x0	Write protection for flash unit 24 (0x1001_8000 → 0x1001_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
23	UNIT23	RW	0x0	Write protection for flash unit 23 (0x1001_7000 → 0x1001_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
22	UNIT22	RW	0x0	Write protection for flash unit 22 (0x1001_6000 → 0x1001_6FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
21	UNIT21	RW	0x0	Write protection for flash unit 21 (0x1001_5000 → 0x1001_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
20	UNIT20	RW	0x0	Write protection for flash unit 20 (0x1001_4000 → 0x1001_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
19	UNIT19	RW	0x0	Write protection for flash unit 19 (0x1001_3000 → 0x1001_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
18	UNIT18	RW	0x0	Write protection for flash unit 18 (0x1001_2000 → 0x1001_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
17	UNIT17	RW	0x0	Write protection for flash unit 17 (0x1001_1000 → 0x1001_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
16	UNIT16	RW	0x0	Write protection for flash unit 16 (0x1001_0000 → 0x1001_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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Bits	Field Name	Type	Reset	Description
15	UNIT15	RW	0x0	Write protection for flash unit 15 (0x1000_F000 → 0x1000_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
14	UNIT14	RW	0x0	Write protection for flash unit 14 (0x1000_E000 → 0x1000_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
13	UNIT13	RW	0x0	Write protection for flash unit 13 (0x1000_D000 → 0x1000_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
12	UNIT12	RW	0x0	Write protection for flash unit 12 (0x1000_C000 → 0x1000_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
11	UNIT11	RW	0x0	Write protection for flash unit 11 (0x1000_B000 → 0x1000_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
10	UNIT10	RW	0x0	Write protection for flash unit 10 (0x1000_A000 → 0x1000_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
9	UNIT9	RW	0x0	Write protection for flash unit 9 (0x1000_9000 → 0x1000_9FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
8	UNIT8	RW	0x0	Write protection for flash unit 8 (0x1000_8000 → 0x1000_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
7	UNIT7	RW	0x0	Write protection for flash unit 7 (0x1000_7000 → 0x1000_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
6	UNIT6	RW	0x0	Write protection for flash unit 6 (0x1000_6000 → 0x1000_6FFF)

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
5	UNIT5	RW	0x0	Write protection for flash unit 5 (0x1000_5000 → 0x1000_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
4	UNIT4	RW	0x0	Write protection for flash unit 4 (0x1000_4000 → 0x1000_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
3	UNIT3	RW	0x0	Write protection for flash unit 3 (0x1000_3000 → 0x1000_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
2	UNIT2	RW	0x0	Write protection for flash unit 2 (0x1000_2000 → 0x1000_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
1	UNIT1	RW	0x0	Write protection for flash unit 1 (0x1000_1000 → 0x1000_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
0	UNIT0	RW	0x0	Write protection for flash unit 0 (0x1000_0000 → 0x1000_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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20.8.2.6 Flash Write Protect Register 1 (FLASHWP1)

Table 20-16: Flash Write Protect Register 1 (FLASHWP1) Layout

FLASHWP1 (Flash Write Protect Register 1) Offset: 0x30 Default: 0x00000000 Access: FLASH -> FLASHWP1.all							
31	30	29	28	27	26	25	24
UNIT63	UNIT62	UNIT61	UNIT60	UNIT59	UNIT58	UNIT57	UNIT56
23	22	21	20	19	18	17	16
UNIT55	UNIT54	UNIT53	UNIT52	UNIT51	UNIT50	UNIT49	UNIT48
15	14	13	12	11	10	9	8
UNIT47	UNIT46	UNIT45	UNIT44	UNIT43	UNIT42	UNIT41	UNIT40
7	6	5	4	3	2	1	0
UNIT39	UNIT38	UNIT37	UNIT36	UNIT35	UNIT34	UNIT33	UNIT32

Table 20-17: Flash Write Protect Register 1 (FLASHWP1) Field Description

Bits	Field Name	Type	Reset	Description
31	UNIT63	RW	0x0	Write protection for flash unit 63 (0x1003_F000 → 0x1003_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
30	UNIT62	RW	0x0	Write protection for flash unit 62 (0x1003_E000 → 0x1003_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
29	UNIT61	RW	0x0	Write protection for flash unit 61 (0x1003_D000 → 0x1003_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
28	UNIT60	RW	0x0	Write protection for flash unit 60 (0x1003_C000 → 0x1003_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
27	UNIT59	RW	0x0	Write protection for flash unit 59 (0x1003_B000 → 0x1003_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
26	UNIT58	RW	0x0	Write protection for flash unit 58 (0x1003_A000 → 0x1003_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
25	UNIT57	RW	0x0	Write protection for flash unit 57 (0x1003_9000 → 0x1003_9FFF)

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Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
24	UNIT56	RW	0x0	Write protection for flash unit 56 (0x1003_8000 → 0x1003_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
23	UNIT55	RW	0x0	Write protection for flash unit 55 (0x1003_7000 → 0x1003_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
22	UNIT54	RW	0x0	Write protection for flash unit 54 (0x1003_6000 → 0x1003_6FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
21	UNIT53	RW	0x0	Write protection for flash unit 53 (0x1003_5000 → 0x1003_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
20	UNIT52	RW	0x0	Write protection for flash unit 52 (0x1003_4000 → 0x1003_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
19	UNIT51	RW	0x0	Write protection for flash unit 51 (0x1003_3000 → 0x1003_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
18	UNIT50	RW	0x0	Write protection for flash unit 50 (0x1003_2000 → 0x1003_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
17	UNIT49	RW	0x0	Write protection for flash unit 49 (0x1003_1000 → 0x1003_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
16	UNIT48	RW	0x0	Write protection for flash unit 48 (0x1003_0000 → 0x1003_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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Bits	Field Name	Type	Reset	Description
15	UNIT47	RW	0x0	Write protection for flash unit 47 (0x1002_F000 → 0x1002_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
14	UNIT46	RW	0x0	Write protection for flash unit 46 (0x1002_E000 → 0x1002_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
13	UNIT45	RW	0x0	Write protection for flash unit 45 (0x1002_D000 → 0x1002_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
12	UNIT44	RW	0x0	Write protection for flash unit 44 (0x1002_C000 → 0x1002_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
11	UNIT43	RW	0x0	Write protection for flash unit 43 (0x1002_B000 → 0x1002_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
10	UNIT42	RW	0x0	Write protection for flash unit 42 (0x1002_A000 → 0x1002_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
9	UNIT41	RW	0x0	Write protection for flash unit 41 (0x1002_9000 → 0x1002_9FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
8	UNIT40	RW	0x0	Write protection for flash unit 40 (0x1002_8000 → 0x1002_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
7	UNIT39	RW	0x0	Write protection for flash unit 39 (0x1002_7000 → 0x1002_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
6	UNIT38	RW	0x0	Write protection for flash unit 38 (0x1002_6000 → 0x1002_6FFF)

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
5	UNIT37	RW	0x0	Write protection for flash unit 37 (0x1002_5000 → 0x1002_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
4	UNIT36	RW	0x0	Write protection for flash unit 36 (0x1002_4000 → 0x1002_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
3	UNIT35	RW	0x0	Write protection for flash unit 35 (0x1002_3000 → 0x1002_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
2	UNIT34	RW	0x0	Write protection for flash unit 34 (0x1002_2000 → 0x1002_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
1	UNIT33	RW	0x0	Write protection for flash unit 33 (0x1002_1000 → 0x1002_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
0	UNIT32	RW	0x0	Write protection for flash unit 32 (0x1002_0000 → 0x1002_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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20.8.2.7 Flash Write Protect Register 2 (FLASHWP2)

Table 20-18: Flash Write Protect Register 2 (FLASHWP2) Layout

FLASHWP2 (Flash Write Protect Register 2) Offset: 0x34 Default: 0x00000000 Access: FLASH -> FLASHWP2.all							
31	30	29	28	27	26	25	24
UNIT95	UNIT94	UNIT93	UNIT92	UNIT91	UNIT90	UNIT89	UNIT88
23	22	21	20	19	18	17	16
UNIT87	UNIT86	UNIT85	UNIT84	UNIT83	UNIT82	UNIT81	UNIT80
15	14	13	12	11	10	9	8
UNIT79	UNIT78	UNIT77	UNIT76	UNIT75	UNIT74	UNIT73	UNIT72
7	6	5	4	3	2	1	0
UNIT71	UNIT70	UNIT69	UNIT68	UNIT67	UNIT66	UNIT65	UNIT64

Table 20-19: Flash Write Protect Register 2 (FLASHWP2) Field Description

Bits	Field Name	Type	Reset	Description
31	UNIT95	RW	0x0	Write protection for flash unit 95 (0x1005_F000 → 0x1005_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
30	UNIT94	RW	0x0	Write protection for flash unit 94 (0x1005_E000 → 0x1005_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
29	UNIT93	RW	0x0	Write protection for flash unit 93 (0x1005_D000 → 0x1005_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
28	UNIT92	RW	0x0	Write protection for flash unit 92 (0x1005_C000 → 0x1005_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
27	UNIT91	RW	0x0	Write protection for flash unit 91 (0x1005_B000 → 0x1005_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
26	UNIT90	RW	0x0	Write protection for flash unit 90 (0x1005_A000 → 0x1005_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
25	UNIT89	RW	0x0	Write protection for flash unit 89 (0x1005_9000 → 0x1005_9FFF)

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
24	UNIT88	RW	0x0	Write protection for flash unit 88 (0x1005_8000 → 0x1005_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
23	UNIT87	RW	0x0	Write protection for flash unit 87 (0x1005_7000 → 0x1005_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
22	UNIT86	RW	0x0	Write protection for flash unit 86 (0x1005_6000 → 0x1005_6FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
21	UNIT85	RW	0x0	Write protection for flash unit 85 (0x1005_5000 → 0x1005_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
20	UNIT84	RW	0x0	Write protection for flash unit 84 (0x1005_4000 → 0x1005_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
19	UNIT83	RW	0x0	Write protection for flash unit 83 (0x1005_3000 → 0x1005_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
18	UNIT82	RW	0x0	Write protection for flash unit 82 (0x1005_2000 → 0x1005_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
17	UNIT81	RW	0x0	Write protection for flash unit 81 (0x1005_1000 → 0x1005_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
16	UNIT80	RW	0x0	Write protection for flash unit 80 (0x1005_0000 → 0x1005_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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Bits	Field Name	Type	Reset	Description
15	UNIT79	RW	0x0	Write protection for flash unit 79 (0x1004_F000 → 0x1004_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
14	UNIT78	RW	0x0	Write protection for flash unit 78 (0x1004_E000 → 0x1004_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
13	UNIT77	RW	0x0	Write protection for flash unit 77 (0x1004_D000 → 0x1004_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
12	UNIT76	RW	0x0	Write protection for flash unit 76 (0x1004_C000 → 0x1004_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
11	UNIT75	RW	0x0	Write protection for flash unit 75 (0x1004_B000 → 0x1004_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
10	UNIT74	RW	0x0	Write protection for flash unit 74 (0x1004_A000 → 0x1004_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
9	UNIT73	RW	0x0	Write protection for flash unit 73 (0x1004_9000 → 0x1004_9FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
8	UNIT72	RW	0x0	Write protection for flash unit 72 (0x1004_8000 → 0x1004_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
7	UNIT71	RW	0x0	Write protection for flash unit 71 (0x1004_7000 → 0x1004_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
6	UNIT70	RW	0x0	Write protection for flash unit 70 (0x1004_6000 → 0x1004_6FFF)

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
5	UNIT69	RW	0x0	Write protection for flash unit 69 (0x1004_5000 → 0x1004_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
4	UNIT68	RW	0x0	Write protection for flash unit 68 (0x1004_4000 → 0x1004_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
3	UNIT67	RW	0x0	Write protection for flash unit 67 (0x1004_3000 → 0x1004_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
2	UNIT66	RW	0x0	Write protection for flash unit 66 (0x1004_2000 → 0x1004_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
1	UNIT65	RW	0x0	Write protection for flash unit 65 (0x1004_1000 → 0x1004_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
0	UNIT64	RW	0x0	Write protection for flash unit 64 (0x1004_0000 → 0x1004_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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20.8.2.8 Flash Write Protect Register 3 (FLASHWP3)

Table 20-20: Flash Write Protect Register 3 (FLASHWP3) Layout

FLASHWP3 (Flash Write Protect Register 3) Offset: 0x38 Default: 0x00000000 Access: FLASH -> FLASHWP3.all							
31 UNIT127	30 UNIT126	29 UNIT125	28 UNIT124	27 UNIT123	26 UNIT122	25 UNIT121	24 UNIT120
23 UNIT119	22 UNIT118	21 UNIT117	20 UNIT116	19 UNIT115	18 UNIT114	17 UNIT113	16 UNIT112
15 UNIT111	14 UNIT110	13 UNIT109	12 UNIT108	11 UNIT107	10 UNIT106	9 UNIT105	8 UNIT104
7 UNIT103	6 UNIT102	5 UNIT101	4 UNIT100	3 UNIT99	2 UNIT98	1 UNIT97	0 UNIT96

Table 20-21: Flash Write Protect Register 3 (FLASHWP3) Field Description

Bits	Field Name	Type	Reset	Description
31	UNIT127	RW	0x0	Write protection for flash unit 127 (0x1007_F000 → 0x1007_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
30	UNIT126	RW	0x0	Write protection for flash unit 126 (0x1007_E000 → 0x1007_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
29	UNIT125	RW	0x0	Write protection for flash unit 125 (0x1007_D000 → 0x1007_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
28	UNIT124	RW	0x0	Write protection for flash unit 124 (0x1007_C000 → 0x1007_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
27	UNIT123	RW	0x0	Write protection for flash unit 123 (0x1007_B000 → 0x1007_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
26	UNIT122	RW	0x0	Write protection for flash unit 122 (0x1007_A000 → 0x1007_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
25	UNIT121	RW	0x0	Write protection for flash unit 121 (0x1007_9000 → 0x1007_9FFF)

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
24	UNIT120	RW	0x0	Write protection for flash unit 120 (0x1007_8000 → 0x1007_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
23	UNIT119	RW	0x0	Write protection for flash unit 119 (0x1007_7000 → 0x1007_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
22	UNIT118	RW	0x0	Write protection for flash unit 118 (0x1007_6000 → 0x1007_6FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
21	UNIT117	RW	0x0	Write protection for flash unit 117 (0x1007_5000 → 0x1007_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
20	UNIT116	RW	0x0	Write protection for flash unit 116 (0x1007_4000 → 0x1007_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
19	UNIT115	RW	0x0	Write protection for flash unit 115 (0x1007_3000 → 0x1007_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
18	UNIT114	RW	0x0	Write protection for flash unit 114 (0x1007_2000 → 0x1007_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
17	UNIT113	RW	0x0	Write protection for flash unit 113 (0x1007_1000 → 0x1007_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
16	UNIT112	RW	0x0	Write protection for flash unit 112 (0x1007_0000 → 0x1007_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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Bits	Field Name	Type	Reset	Description
15	UNIT111	RW	0x0	Write protection for flash unit 111 (0x1006_F000 → 0x1006_FFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
14	UNIT110	RW	0x0	Write protection for flash unit 110 (0x1006_E000 → 0x1006_EFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
13	UNIT109	RW	0x0	Write protection for flash unit 109 (0x1006_D000 → 0x1006_DFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
12	UNIT108	RW	0x0	Write protection for flash unit 108 (0x1006_C000 → 0x1006_CFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
11	UNIT107	RW	0x0	Write protection for flash unit 107 (0x1006_B000 → 0x1006_BFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
10	UNIT106	RW	0x0	Write protection for flash unit 106 (0x1006_A000 → 0x1006_AFFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
9	UNIT105	RW	0x0	Write protection for flash unit 105 (0x1006_9000 → 0x1006_9FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
8	UNIT104	RW	0x0	Write protection for flash unit 104 (0x1006_8000 → 0x1006_8FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
7	UNIT103	RW	0x0	Write protection for flash unit 103 (0x1006_7000 → 0x1006_7FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
6	UNIT102	RW	0x0	Write protection for flash unit 102 (0x1006_6000 → 0x1006_6FFF)

SPINTROL

Bits	Field Name	Type	Reset	Description
				0: Can be programed or erased 1: Cannot be programed or sector erased
5	UNIT101	RW	0x0	Write protection for flash unit 101 (0x1006_5000 → 0x1006_5FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
4	UNIT100	RW	0x0	Write protection for flash unit 100 (0x1006_4000 → 0x1006_4FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
3	UNIT99	RW	0x0	Write protection for flash unit 99 (0x1006_3000 → 0x1006_3FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
2	UNIT98	RW	0x0	Write protection for flash unit 98 (0x1006_2000 → 0x1006_2FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
1	UNIT97	RW	0x0	Write protection for flash unit 97 (0x1006_1000 → 0x1006_1FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased
0	UNIT96	RW	0x0	Write protection for flash unit 96 (0x1006_0000 → 0x1006_0FFF) 0: Can be programed or erased 1: Cannot be programed or sector erased

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20.8.2.9 Flash Register Write-Allow Key Register (FLASHREGKEY)

Table 20-22: Flash Register Write-Allow Key Register (FLASHREGKEY) Layout

FLASHREGKEY (Flash Register Write-Allow Key Register) Offset: 0x3C Default: 0x1ACCE551 Access: FLASH -> FLASHREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 20-23: Flash Register Write-Allow Key Register (FLASHREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected flash registers

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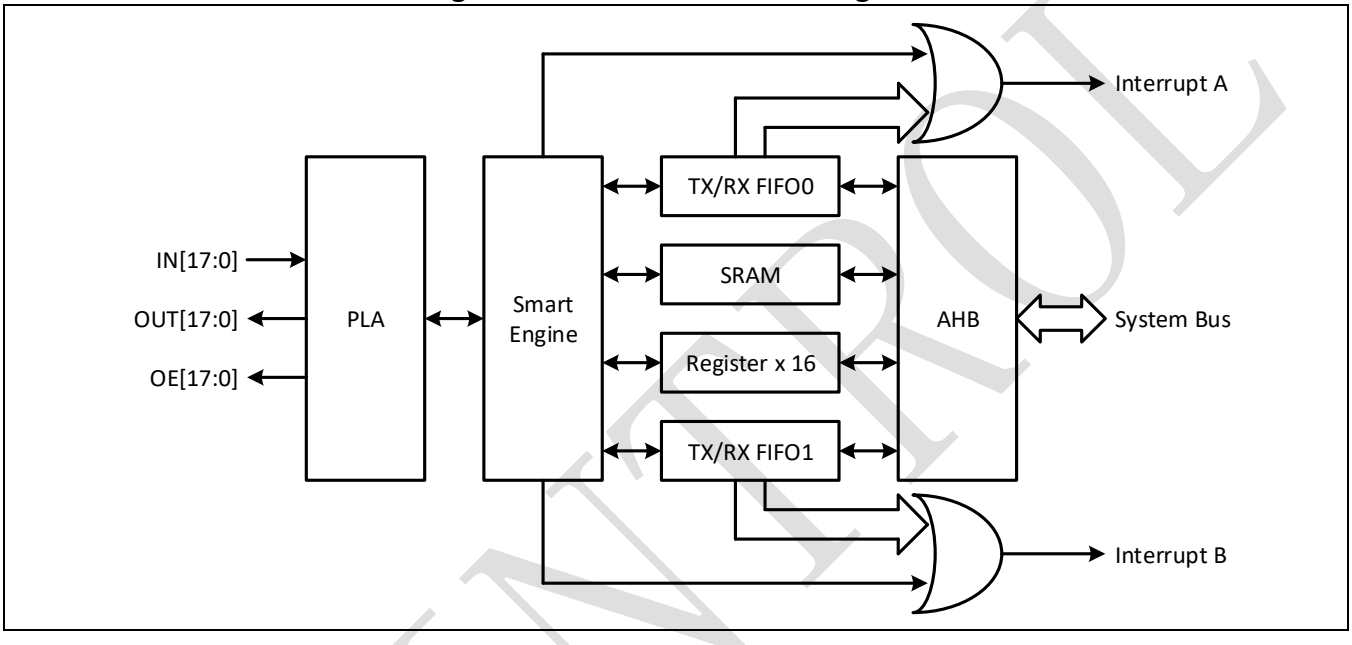
21 SIO

21.1 Overview

SIO is a Spintrol patented technology. It has programmable capability which can convert the SIO block into pre-defined communication module. Three SIOs are implemented in SPC2168. Each supports up to 18 IO channels as listed in Table 4-1.

Figure 21-1: SIO architecture diagram



The architecture of the SIO is shown in Figure 21-1. It basically consists of two TX FIFOs, two RX FIFOs, 16 registers and an SRAM on AHB bus, a programmable logic array, and a smart-engine. Each SIO provides up to two interrupts to the main CPU and CAU of SPC2168. The PLA provides fast parallel logic processing, while the smart engine is capable to deal with state control and transfer for complicated protocols. By ultilizing the befenefits of the two, the SIO in SPC2168 enables following usage cases:

- Re-define the pins for a given interface on a given SPC2168 device.
  i.e. An UART interface implemented on SIO with GPIO40/GPIO41 as TXD/RXD can be changed to GPIO30/GPIO31 as TXD/RXD via firmware update.
- Re-define the whole interface function on a given SPC2168 device.
  i.e. The SIO is originally defined as I2C. It can be changed via firmware update to UART per user's system requirement.
- Add-on feature for a standard interface on a given SPC2168 device.
  i.e. Embed user defined data format and communication 790rotocol based on standard UART into a single new interface via firmware update.

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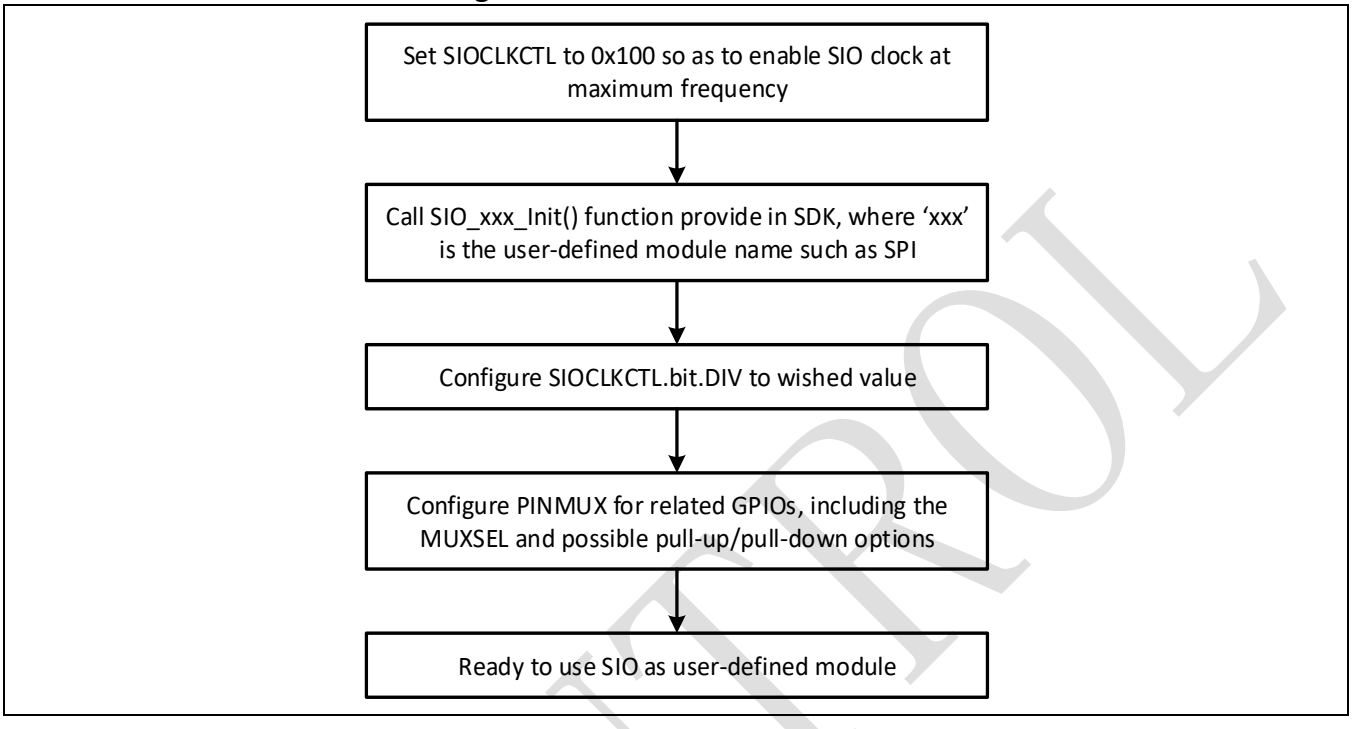
21.2 SIO Initialization

Figure 21-2 shows the flow to initialize the SIO as a user-defined module.

Figure 21-2: SIO initialization flow



Example 21.2.1

```
void    SIO_Example21_2_1(void)
{
   /* Enable SIO clock at maximum frequency to minimize initialization time */
   CLOCK->SIOCLKCTL.all = 0x100;

   /* Initialize the SIO PLA and smart engine to make the SIO as a UART */
   SIO_UART_Init();

   /* Configure SIO clock frequency as SYSCLK1/4 */
   CLOCK->SIOCLKCTL.bit.DIV = 0x3;

   /* Configure GPIO40 and GPIO41 to SIO channel with pull-up enabled for UART */
   PINMUX->GPIO40.bit.MUXSEL    = GPIO40_BIT_MUXSEL_SIO1_14;
   PINMUX->GPIO40.bit.PU        |= 1 << GPIO40_BIT_MUXSEL_SIO1_14;
   PINMUX->GPIO41.bit.MUXSEL    = GPIO41_BIT_MUXSEL_SIO1_15;
   PINMUX->GPIO41.bit.PU        |= 1 << GPIO41_BIT_MUXSEL_SIO1_15;

   /* Ready to use SIO as UART */
}
```

21.3 Registers

Please refer to application note for corresponding SIO based user-defined modules.

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22 System control

22.1 Overview

The system control module provides:

- Unique device ID register (64 bits)
- Memory error interrupt control registers
- Memory ECC enable register
- Memory lock status register
- Reset event control registers
- System information register
- CAU control register

22.2 Unique device ID register (64 bits)

The unique device identifier is ideally suited:

- for use as serial numbers
- for use as security keys in order to increase the security of code in Flash memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal Flash memory
- to activate secure boot processes, etc.

The 64-bit unique device identifier provides a reference number which is unique for any device and in any context. These bits can never be altered by the user.

22.3 Memory error interrupt control registers

These registers are used to enable, indicate and clear memory error interrupts.

22.4 Memory ECC enable register

The register enables ROM, RAM and Flash memory ECC feature.

22.5 Memory lock status register

The register contains Flash memory and RAM multi-zone protection status, Configuration Words lock status.

22.6 Reset event control registers

These registers are used to enable, indicate and clear reset events.

22.7 System information register

The register provides information about Flash size, ADC effective bits and clock frequency option.

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22.8 CAU control register

The register enables CAU running and its debug interface.

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22.9 Registers

22.9.1 System register map

Table 22-1: SYSTEM Module Base Address

Peripheral Module	Base Address
SYSTEM	0x4000 0000

Table 22-2: SYSTEM Register Map

Register	Offset	Description	Reset Value
CID0	0x00	Chip ID Register 0	0x00000000
CID1	0x04	Chip ID Register 1	0x00000000
UID0	0x08	Unique ID Register 0	0x00000000
UID1	0x0C	Unique ID Register 1	0x00000000
RND0	0x10	Random Number Register 0	0x00000000
RND1	0x14	Random Number Register 1	0x00000000
REV0	0x18	Revision Information Register 0	0x636D1611
REV1	0x1C	Revision Information Register 1	0x201812A0
MEMIF	0x20	Memory Error Interrupt Flag Register	0x00000000
MEMIC	0x24	Memory Error Interrupt Clear Register	0x00000000
MEMIE*	0x28	Memory Error Interrupt Enable Register	0x00000000
MEMECCEN*	0x2C	Memory ECC Enable Register	0x00000007
MEMLOCKSTS	0x30	Memory Lock Status Register	0x00000000
RSTEVTSTS	0x34	Reset Event Status Register	0x00000000
RSTEVTCLR	0x38	Reset Event Status Clear Register	0x00000000
RSTEVTEN*	0x3C	Reset Event Enable Register	0x00000005
SYSINFO	0x40	System Information Register	0x000003F3
CAUCTL*	0x44	CAU Control Register	0x00000000
SYSREGKEY	0x48	System Register Write-Allow Key Register	0x1ACCE551

Note: Registers marked with * are write-allowed only when the SYSREGKEY=0x1ACCE551.

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22.9.2 System registers

22.9.2.1 Chip ID Register 0 (CID0)

Table 22-3: Chip ID Register 0 (CID0) Layout

CID0 (Chip ID Register 0) Offset: 0x0 Default: 0x00000000 Access: GLOBAL -> CID0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-4: Chip ID Register 0 (CID0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	32 LSBs of the 64-bit chip ID

22.9.2.2 Chip ID Register 1 (CID1)

Table 22-5: Chip ID Register 1 (CID1) Layout

CID1 (Chip ID Register 1) Offset: 0x4 Default: 0x00000000 Access: GLOBAL -> CID1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-6: Chip ID Register 1 (CID1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	32 MSBs of the 64-bit chip ID

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22.9.2.3 Unique ID Register 0 (UID0)

Table 22-7: Unique ID Register 0 (UID0) Layout

UID0 (Unique ID Register 0) Offset: 0x8 Default: 0x00000000 Access: GLOBAL -> UID0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-8: Unique ID Register 0 (UID0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	32 LSBs of the 64-bit unique ID

22.9.2.4 Unique ID Register 1 (UID1)

Table 22-9: Unique ID Register 1 (UID1) Layout

UID1 (Unique ID Register 1) Offset: 0xC Default: 0x00000000 Access: GLOBAL -> UID1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-10: Unique ID Register 1 (UID1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	32 MSBs of the 64-bit unique ID

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22.9.2.5 Random Number Register 0 (RND0)

Table 22-11: Random Number Register 0 (RND0) Layout

RND0 (Random Number Register 0) Offset: 0x10 Default: 0x00000000 Access: SYSTEM -> RND0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-12: Random Number Register 0 (RND0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	32 LSBs of the 64-bit random number

22.9.2.6 Random Number Register 1 (RND1)

Table 22-13: Random Number Register 1 (RND1) Layout

RND1 (Random Number Register 1) Offset: 0x14 Default: 0x00000000 Access: SYSTEM -> RND1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-14: Random Number Register 1 (RND1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x0	32 MSBs of the 64-bit random number

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22.9.2.7 Revision Information Register 0 (REV0)

Table 22-15: Revision Information Register 0 (REV0) Layout

REV0 (Revision Information Register 0) Offset: 0x18 Default: 0x636D1611 Access: SYSTEM -> REV0.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-16: Revision Information Register 0 (REV0) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x636D1611	32 LSBs of the 64-bit revision number

22.9.2.8 Revision Information Register 1 (REV1)

Table 22-17: Revision Information Register 1 (REV1) Layout

REV1 (Revision Information Register 1) Offset: 0x1C Default: 0x201812A0 Access: SYSTEM -> REV1.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 22-18: Revision Information Register 1 (REV1) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RO	0x201812A0	32 MSBs of the 64-bit revision number

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22.9.2.9 Memory Error Interrupt Flag Register (MEMIF)

Table 22-19: Memory Error Interrupt Flag Register (MEMIF) Layout

MEMIF (Memory Error Interrupt Flag Register) Offset: 0x20 Default: 0x00000000 Access: SYSTEM -> MEMIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
MEMINT	SIO2PERR	SIO1PERR	SIO0PERR	CDRAM2ERR	CDRAM1ERR	CIRAM2ERR	CIRAM1ERR
7	6	5	4	3	2	1	0
MDRAM2ERR	MDRAM1ERR	MIRAM2ERR	MIRAM1ERR	FLASH2ERR	FLASH1ERR	ROM2ERR	ROM1ERR

Table 22-20: Memory Error Interrupt Flag Register (MEMIF) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	MEMINT	RO	0x0	Memory error interrupt flag 0: Interrupt does not occur 1: Interrupt occurred. Further interrupt will not be generated until this bit is cleared.
14	SIO2PERR	RO	0x0	SIO2 memory parity error flag 0: Parity error does not occur 1: Parity error occurred. Further parity error will not generate interrupt until this bit is cleared.
13	SIO1PERR	RO	0x0	SIO1 memory parity error flag 0: Parity error does not occur 1: Parity error occurred. Further parity error will not generate interrupt until this bit is cleared.
12	SIO0PERR	RO	0x0	SIO0 memory parity error flag 0: Parity error does not occur 1: Parity error occurred. Further parity error will not generate interrupt until this bit is cleared.
11	CDRAM2ERR	RO	0x0	CAU data RAM ECC 2-bit error flag 0: ECC 2-bit error does not occur 1: ECC 2-bit error occurred. Further error will not generate interrupt until this bit is cleared.
10	CDRAM1ERR	RO	0x0	CAU data RAM ECC 1-bit error flag 0: ECC 1-bit error does not occur 1: ECC 1-bit error occurred. Further error will not generate interrupt until this bit is cleared.
9	CIRAM2ERR	RO	0x0	CAU instrunction RAM ECC 2-bit error flag 0: ECC 2-bit error does not occur

SPINTROL

Bits	Field Name	Type	Reset	Description
				1: ECC 2-bit error occurred. Further error will not generate interrupt until this bit is cleared.
8	CIRAM1ERR	RO	0x0	CAU instruction RAM ECC 1-bit error flag 0: ECC 1-bit error does not occur 1: ECC 1-bit error occurred. Further error will not generate interrupt until this bit is cleared.
7	MDRAM2ERR	RO	0x0	Main data RAM ECC 2-bit error flag 0: ECC 2-bit error does not occur 1: ECC 2-bit error occurred. Further error will not generate interrupt until this bit is cleared.
6	MDRAM1ERR	RO	0x0	Main data RAM ECC 1-bit error flag 0: ECC 1-bit error does not occur 1: ECC 1-bit error occurred. Further error will not generate interrupt until this bit is cleared.
5	MIRAM2ERR	RO	0x0	Main instrunction RAM ECC 2-bit error flag 0: ECC 2-bit error does not occur 1: ECC 2-bit error occurred. Further error will not generate interrupt until this bit is cleared.
4	MIRAM1ERR	RO	0x0	Main instruction RAM ECC 1-bit error flag 0: ECC 1-bit error does not occur 1: ECC 1-bit error occurred. Further error will not generate interrupt until this bit is cleared.
3	FLASH2ERR	RO	0x0	FLASH ECC 2-bit error flag 0: ECC 2-bit error does not occur 1: ECC 2-bit error occurred. Further error will not generate interrupt until this bit is cleared.
2	FLASH1ERR	RO	0x0	FLASH ECC 1-bit error flag 0: ECC 1-bit error does not occur 1: ECC 1-bit error occurred. Further error will not generate interrupt until this bit is cleared.
1	ROM2ERR	RO	0x0	ROM ECC 2-bit error flag 0: ECC 2-bit error does not occur 1: ECC 2-bit error occurred. Further error will not generate interrupt until this bit is cleared.
0	ROM1ERR	RO	0x0	ROM ECC 1-bit error flag 0: ECC 1-bit error does not occur 1: ECC 1-bit error occurred. Further error will not generate interrupt until this bit is cleared.

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22.9.2.10 Memory Error Interrupt Clear Register (MEMIC)

Table 22-21: Memory Error Interrupt Clear Register (MEMIC) Layout

MEMIC (Memory Error Interrupt Clear Register) Offset: 0x24 Default: 0x00000000 Access: SYSTEM -> MEMIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
MEMINT	SIO2PERR	SIO1PERR	SIO0PERR	CDRAM2ERR	CDRAM1ERR	CIRAM2ERR	CIRAM1ERR
7	6	5	4	3	2	1	0
MDRAM2ERR	MDRAM1ERR	MIRAM2ERR	MIRAM1ERR	FLASH2ERR	FLASH1ERR	ROM2ERR	ROM1ERR

Table 22-22: Memory Error Interrupt Clear Register (MEMIC) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	MEMINT	W1C	0x0	Memory error interrupt clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the interrupt and the flag. This bit is self-cleared to 0.
14	SIO2PERR	W1C	0x0	SIO2 memory parity error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
13	SIO1PERR	W1C	0x0	SIO1 memory parity error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
12	SIO0PERR	W1C	0x0	SIO0 memory parity error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
11	CDRAM2ERR	W1C	0x0	CAU data RAM ECC 2-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
10	CDRAM1ERR	W1C	0x0	CAU data RAM ECC 1-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
9	CIRAM2ERR	W1C	0x0	CAU instruction RAM ECC 2-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
8	CIRAM1ERR	W1C	0x0	CAU instruction RAM ECC 1-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.

SPINTROL

Bits	Field Name	Type	Reset	Description
7	MDRAM2ERR	W1C	0x0	Main data RAM ECC 2-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
6	MDRAM1ERR	W1C	0x0	Main data RAM ECC 1-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
5	MIRAM2ERR	W1C	0x0	Main instruction RAM ECC 2-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
4	MIRAM1ERR	W1C	0x0	Main instruction RAM ECC 1-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
3	FLASH2ERR	W1C	0x0	FLASH ECC 2-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
2	FLASH1ERR	W1C	0x0	FLASH ECC 1-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
1	ROM2ERR	W1C	0x0	ROM ECC 2-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.
0	ROM1ERR	W1C	0x0	ROM ECC 1-bit error flag clear 0: Write a 0 has no effect and always reads back 0 1: Write a 1 clear the flag. This bit is self-cleared.

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22.9.2.11 Memory Error Interrupt Enable Register (MEMIE)

Table 22-23: Memory Error Interrupt Enable Register (MEMIE) Layout

MEMIE (Memory Error Interrupt Enable Register) Offset: 0x28 Default: 0x00000000 Access: SYSTEM -> MEMIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED	SIO2PERR	SIO1PERR	SIO0PERR	CDRAM2ERR	CDRAM1ERR	CIRAM2ERR	CIRAM1ERR
7	6	5	4	3	2	1	0
MDRAM2ERR	MDRAM1ERR	MIRAM2ERR	MIRAM1ERR	FLASH2ERR	FLASH1ERR	ROM2ERR	ROM1ERR

Table 22-24: Memory Error Interrupt Enable Register (MEMIE) Field Description

Bits	Field Name	Type	Reset	Description
31:15	RESERVED_31_15	RO	0x0	Reserved
14	SIO2PERR	RW	0x0	SIO2 parity error interrupt enable 0: Disable 1: Enable
13	SIO1PERR	RW	0x0	SIO1 parity error interrupt enable 0: Disable 1: Enable
12	SIO0PERR	RW	0x0	SIO0 parity error interrupt enable 0: Disable 1: Enable
11	CDRAM2ERR	RW	0x0	CAU data RAM ECC 2-bit error interrupt enable 0: Disable 1: Enable
10	CDRAM1ERR	RW	0x0	CAU data RAM ECC 1-bit error interrupt enable 0: Disable 1: Enable
9	CIRAM2ERR	RW	0x0	CAU instruction RAM ECC 2-bit error interrupt enable 0: Disable 1: Enable
8	CIRAM1ERR	RW	0x0	CAU instruction RAM ECC 1-bit error interrupt enable 0: Disable 1: Enable
7	MDRAM2ERR	RW	0x0	Main data RAM ECC 2-bit error interrupt enable 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
6	MDRAM1ERR	RW	0x0	Main data RAM ECC 1-bit error interrupt enable 0: Disable 1: Enable
5	MIRAM2ERR	RW	0x0	Main instruction RAM ECC 2-bit error interrupt enable 0: Disable 1: Enable
4	MIRAM1ERR	RW	0x0	Main instruction RAM ECC 1-bit error interrupt enable 0: Disable 1: Enable
3	FLASH2ERR	RW	0x0	Flash ECC 2-bit error interrupt enable 0: Disable 1: Enable
2	FLASH1ERR	RW	0x0	Flash ECC 1-bit error interrupt enable 0: Disable 1: Enable
1	ROM2ERR	RW	0x0	ROM ECC 2-bit error interrupt enable 0: Disable 1: Enable
0	ROM1ERR	RW	0x0	ROM ECC 1-bit error interrupt enable 0: Disable 1: Enable

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22.9.2.12 Memory ECC Enable Register (MEMECCEN)

Table 22-25: Memory ECC Enable Register (MEMECCEN) Layout

MEMECCEN (Memory ECC Enable Register) Offset: 0x2C Default: 0x00000007 Access: SYSTEM -> MEMECCEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED					RAMECC	FLASHECC	ROMECC

Table 22-26: Memory ECC Enable Register (MEMECCEN) Field Description

Bits	Field Name	Type	Reset	Description
31:3	RESERVED_31_3	RO	0x0	Reserved
2	RAMECC	RW	0x1	RAM ECC enable 0: Disable 1: Enable
1	FLASHECC	RW	0x1	FLASH ECC enable 0: Disable 1: Enable
0	ROMECC	RW	0x1	ROM ECC enable 0: Disable 1: Enable

SPINTROL

22.9.2.13 Memory Lock Status Register (MEMLOCKSTS)

Table 22-27: Memory Lock Status Register (MEMLOCKSTS) Layout

MEMLOCKSTS (Memory Lock Register) Offset: 0x30 Default: 0x00000000 Access: GLOBAL -> MEMLOCKSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED			RAM3	RAM2	RAM1	RAM0	FLASHOTP
7	6	5	4	3	2	1	0
USER3INFO	USER2INFO	USER1INFO	USER0INFO	FLASH3	FLASH2	FLASH1	FLASH0

Table 22-28: Memory Lock Status Register (MEMLOCKSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:13	RESERVED_31_13	RO	0x0	Reserved
12	RAM3	RO	0x0	RAM region 3 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute
11	RAM2	RO	0x0	RAM region 2 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute
10	RAM1	RO	0x0	RAM region 1 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute
9	RAM0	RO	0x0	RAM region 0 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute
8	FLASHOTP	RO	0x0	FLASH OTP lock status 0: Can read, write and erase the FLASH OTP region 1: FLASH OTP region is read only
7	USER3INFO	RO	0x0	Multi-zone security User 3 information lock status 0: Can read, write and erase User 3 information 1: User 3 information is read only
6	USER2INFO	RO	0x0	Multi-zone security User 2 information lock status 0: Can read, write and erase User 2 information 1: User 2 information is read only
5	USER1INFO	RO	0x0	Multi-zone security User 1 information lock status 0: Can read, write and erase User 1 information 1: User 1 information is read only

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Bits	Field Name	Type	Reset	Description
4	USER0INFO	RO	0x0	Multi-zone security User 0 information lock status 0: Can read, write and erase User 0 information 1: User 0 information is read only
3	FLASH3	RO	0x0	FLASH region 3 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute
2	FLASH2	RO	0x0	FLASH region 2 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute
1	FLASH1	RO	0x0	FLASH region 1 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute
0	FLASH0	RO	0x0	FLASH region 0 lock status 0: Can read/write content and execute 1: Can not read/write content, just execute

SPINTROL

22.9.2.14 Reset Event Status Register (RSTEVTSTS)

Table 22-29: Reset Event Status Register (RSTEVTSTS) Layout

RSTEVTSTS (Reset Event Status Register) Offset: 0x34 Default: 0x00000000 Access: SYSTEM -> RSTEVTSTS.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					SYSRESET	WDT1RST	WDT0RST
15	14	13	12	11	10	9	8
CLKDETERR	PLLUNLOCK	VDD33H	VDD33L	VDD12H	VDD12L1	VDD12L0	SIO2ERR
7	6	5	4	3	2	1	0
SIO1ERR	SIO0ERR	CDRAMERR	CIRAMERR	MDRAMERR	MIRAMERR	FLASHERR	ROMERR

Table 22-30: Reset Event Status Register (RSTEVTSTS) Field Description

Bits	Field Name	Type	Reset	Description
31:19	RESERVED_31_19	RO	0x0	Reserved
18	SYSRESET	RO	0x0	Latched reset triggered by system reset event 0: Specified reset not happen 1: Specified reset happned
17	WDT1RST	RO	0x0	Latched reset triggered by WDT1 reset event 0: Specified reset not happen 1: Specified reset happned
16	WDT0RST	RO	0x0	Latched reset triggered by WDT0 reset event 0: Specified reset not happen 1: Specified reset happned
15	CLKDETERR	RO	0x0	Latched reset triggered by CLKDETERR event 0: Specified reset not happen 1: Specified reset happned
14	PLLUNLOCK	RO	0x0	Latched reset triggered by PLL unlock event 0: Specified reset not happen 1: Specified reset happned
13	VDD33H	RO	0x0	Latched reset triggered by VDD33H event 0: Specified reset not happen 1: Specified reset happned
12	VDD33L	RO	0x0	Latched reset triggered by VDD33L event 0: Specified reset not happen 1: Specified reset happned
11	VDD12H	RO	0x0	Latched reset triggered by VDD12H event 0: Specified reset not happen 1: Specified reset happned
10	VDD12L1	RO	0x0	Latched reset triggered by VDD12L1 event

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Bits	Field Name	Type	Reset	Description
				0: Specified reset not happen 1: Specified reset happned
9	VDD12L0	RO	0x0	Latched reset triggered by VDD12L0 event 0: Specified reset not happen 1: Specified reset happned
8	SIO2ERR	RO	0x0	Latched reset triggered by SIO2 parity error 0: Specified reset not happen 1: Specified reset happned
7	SIO1ERR	RO	0x0	Latched reset triggered by SIO1 parity error 0: Specified reset not happen 1: Specified reset happned
6	SIO0ERR	RO	0x0	Latched reset triggered by SIO0 parity error 0: Specified not happen 1: Specified reset happned
5	CDRAMERR	RO	0x0	Latched reset triggered by CAU data RAM ECC 2-bit error 0: Specified reset not happen 1: Specified reset happned
4	CIRAMERR	RO	0x0	Latched reset triggered by CAU instruction RAM ECC 2-bit error 0: Specified reset not happen 1: Specified reset happned
3	MDRAMERR	RO	0x0	Latched reset triggered by main data RAM ECC 2-bit error 0: Specified reset not happen 1: Specified reset happned
2	MIRAMERR	RO	0x0	Latched reset triggered by main instruction RAM ECC 2-bit eror 0: Specified reset not happen 1: Specified reset happned
1	FLASHERR	RO	0x0	Latched reset triggered by FLASH ECC 2-bit error 0: Specified reset not happen 1: Specified reset happned
0	ROMERR	RO	0x0	Latched reset triggered by ROM ECC 2-bit error 0: Specified reset not happen 1: Specified reset happned

SPINTROL

22.9.2.15 Reset Event Status Clear Register (RSTEVTCLR)

Table 22-31: Reset Event Status Clear Register (RSTEVTCLR) Layout

RSTEVTCLR (Reset Event Status Clear Register) Offset: 0x38 Default: 0x00000000 Access: SYSTEM -> RSTEVTCLR.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED					SYSRESET	WDT1RST	WDT0RST
15	14	13	12	11	10	9	8
CLKDETERR	PLLUNLOCK	VDD33H	VDD33L	VDD12H	VDD12L1	VDD12L0	SIO2ERR
7	6	5	4	3	2	1	0
SIO1ERR	SIO0ERR	CDRAMERR	CIRAMERR	MDRAMERR	MIRAMERR	FLASHERR	ROMERR

Table 22-32: Reset Event Status Clear Register (RSTEVTCLR) Field Description

Bits	Field Name	Type	Reset	Description
31:19	RESERVED_31_19	RO	0x0	Reserved
18	SYSRESET	W1C	0x0	Clear latched reset status upon system reset event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
17	WDT1RST	W1C	0x0	Clear latched reset status upon WDT1 reset event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
16	WDT0RST	W1C	0x0	Clear latched reset status upon WDT0 reset event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
15	CLKDETERR	W1C	0x0	Clear latched reset status upon CLKDETERR 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
14	PLLUNLOCK	W1C	0x0	Clear latched reset status upon PLL unlock 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
13	VDD33H	W1C	0x0	Clear latched reset status upon VDD33H event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0

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Bits	Field Name	Type	Reset	Description
12	VDD33L	W1C	0x0	Clear latched reset status upon VDD33L event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
11	VDD12H	W1C	0x0	Clear latched reset status upon VDD12H event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
10	VDD12L1	W1C	0x0	Clear latched reset status upon VDD12L1 event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
9	VDD12L0	W1C	0x0	Clear latched reset status upon VDD12L0 event 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
8	SIO2ERR	W1C	0x0	Clear latched reset status upon SIO2 parity error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
7	SIO1ERR	W1C	0x0	Clear latched reset status upon SIO1 parity error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
6	SIO0ERR	W1C	0x0	Clear latched reset status upon SIO0 parity error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
5	CDRAMERR	W1C	0x0	Clear latched reset status upon CAU data RAM ECC 2-bit error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
4	CIRAMERR	W1C	0x0	Clear latched reset status upon CAU instruction RAM ECC 2-bit error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0

SPINTROL

Bits	Field Name	Type	Reset	Description
3	MDRAMERR	W1C	0x0	Clear latched reset status upon main data RAM ECC 2-bit error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
2	MIRAMERR	W1C	0x0	Clear latched reset status upon main instruction RAM ECC 2-bit error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
1	FLASHERR	W1C	0x0	Clear latched reset status upon FLASH ECC 2-bit error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0
0	ROMERR	W1C	0x0	Clear latched reset status upon ROM ECC 2-bit error 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears the latched reset event This bit is self-cleared to 0

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22.9.2.16 Reset Event Enable Register (RSTEVTEN)

Table 22-33: Reset Event Enable Register (RSTEVTEN) Layout

RSTEVTEN (Reset Event Enable Register) Offset: 0x3C Default: 0x00000005 Access: SYSTEM -> RSTEVTEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15 CLKDETERR	14 PLLUNLOCK	13 VDD33H	12 VDD33L	11 VDD12H	10 VDD12L1	9 VDD12L0	8 SIO2ERR
7 SIO1ERR	6 SIO0ERR	5 CDRAMERR	4 CIRAMERR	3 MDRAMERR	2 MIRAMERR	1 FLASHERR	0 ROMERR

Table 22-34: Reset Event Enable Register (RSTEVTEN) Field Description

Bits	Field Name	Type	Reset	Description
31:16	RESERVED_31_16	RO	0x0	Reserved
15	CLKDETERR	RW	0x0	Enable reset on CLKDETERR event 0: Disable 1: Enable
14	PLLUNLOCK	RW	0x0	Enable reset on PLL unlock event 0: Disable 1: Enable
13	VDD33H	RW	0x0	Enable reset on VDD33H event 0: Disable 1: Enable
12	VDD33L	RW	0x0	Enable reset on VDD33L event 0: Disable 1: Enable
11	VDD12H	RW	0x0	Enable reset on VDD12H event 0: Disable 1: Enable
10	VDD12L1	RW	0x0	Enable reset on VDD12L1 event 0: Disable 1: Enable
9	VDD12L0	RW	0x0	Enable reset on VDD12L0 event 0: Disable 1: Enable
8	SIO2ERR	RW	0x0	Enable reset on SIO2 parity error 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
7	SIO1ERR	RW	0x0	Enable reset on SIO1 parity error 0: Disable 1: Enable
6	SIO0ERR	RW	0x0	Enable reset on SIO0 parity error 0: Disable 1: Enable
5	CDRAMERR	RW	0x0	Enable reset on CAU data RAM ECC 2-bit error 0: Disable 1: Enable
4	CIRAMERR	RW	0x0	Enable reset on CAU instruction RAM ECC 2-bit error 0: Disable 1: Enable
3	MDRAMERR	RW	0x1	Enable reset on main data RAM ECC 2-bit error 0: Disable 1: Enable
2	MIRAMERR	RW	0x1	Enable reset on main instruction RAM ECC 2-bit eror 0: Disable 1: Enable
1	FLASHERR	RW	0x1	Enable reset on FLASH ECC 2-bit error 0: Disable 1: Enable
0	ROMERR	RW	0x1	Enable reset on ROM ECC 2-bit error 0: Disable 1: Enable

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22.9.2.17 System Information Register (SYSINFO)

Table 22-35: System Information Register (SYSINFO) Layout

SYSINFO (System Information Register) Offset: 0x40 Default: 0x000001F3 Access: SYSTEM -> SYSINFO.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED						WITHCAU	ADCBIT
7	6	5	4	3	2	1	0
ADCBIT	CLKOPT			RESERVED		FLASHSIZE	

Table 22-36: System Information Register (SYSINFO) Field Description

Bits	Field Name	Type	Reset	Description
31:10	RESERVED_31_10	RO	0x0	Reserved
9	WITHCAU	RO	0x0	CAU option 0: CAU is unavailable 1: CAU is available
8:7	ADCBIT	RO	0x3	ADC result bit width 00: 14 bit where 4LSBs are always 0 (10 bit equivalent) 01: 14 bit where 3LSBs are always 0 (11 bit equivalent) 10: 14 bit where 2LSBs are always 0 (12 bit equivalent) 11: 14 bit
6:4	CLKOPT	RO	0x7	Clock option 000: Minimum PLL output dividng ratio is 12 XO is unavailable 001: Minimum PLL output dividing ratio is 6 XO is unavailable 010: Minimum PLL output dividing ratio is 4 XO is unavailable 011: Minimum PLL output dividng ratio is 12 XO is available 100: Minimum PLL output dividing ratio is 6 XO is available 101: Minimum PLL output dividing ratio is 4 XO is available 110: Minimum PLL output dividing ratio is 3 XO is available 111: No limitation

SPINTROL

Bits	Field Name	Type	Reset	Description
3:2	RESERVED_3_2	RO	0x0	Reserved
1:0	FLASHSIZE	RO	0x3	FLASH size 00: 64KB Flash 01: 128KB Flash 10: 256KB Flash 11: 512KB Flash

22.9.2.18 CAU Control Register (CAUCTL)

Table 22-37: CAU Control Register (CAUCTL) Layout

CAUCTL (CAU Control Register) Offset: 0x44 Default: 0x00000000
Access: SYSTEM -> CAUCTL.all

31	30	29	28	27	26	25	24
RESERVED						RUN	DBGIFBLK
23	22	21	20	19	18	17	16
DBGIFKEY							
15	14	13	12	11	10	9	8
DBGIFKEY							
7	6	5	4	3	2	1	0
DBGIFKEY							

Table 22-38: CAU Control Register (CAUCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:26	RESERVED_31_26	RO	0x0	Reserved
25	RUN	RW	0x0	CAU starts to run 0: CAU stopped 1: CAU runs
24	DBGIFBLK	RW	0x0	Block debug interface. Once it is blocked, it can only be released via POR reset 0: Debug interface is not blocked 1: Debug interface is blocked
23:0	DBGIFKEY	RW	0x0	Write 0xACCE51 to enable single JTAG or SWD debug interface only for CAU Write 0xACCE52 to enable dual SWD debug interface for main CPU and CAU

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22.9.2.19 System Register Write-Allow Key Register (SYSREGKEY)

Table 22-39: System Register Write-Allow Key Register (SYSREGKEY) Layout

SYSREGKEY (System Register Write-Allow Key Register) Offset: 0x48 Default: 0x1ACCE551 Access: SYSTEM -> SYSREGKEY.all							
31	30	29	28	27	26	25	24
KEY							
23	22	21	20	19	18	17	16
KEY							
15	14	13	12	11	10	9	8
KEY							
7	6	5	4	3	2	1	0
KEY							

Table 22-40: System Register Write-Allow Key Register (SYSREGKEY) Field Description

Bits	Field Name	Type	Reset	Description
31:0	KEY	RW	0x1ACCE551	Write 0x1ACCE551 to unlock protected system registers

SPINTROL

23 Direct memory access controller (DMA)

23.1 DMA Introduction

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The DMA controller in SPC2168 has 6 channels in total to manage memory access requests from one or more peripherals. It has anarbiter for handling the priority between DMA requests. The DMA controller is interconnected with DRAM through the bus matrix as well as APB peripherals (UART and SSP) through AHB-to-APB bridge.

23.2 DMA features

The SPC2168 DMA controller has the following features:

- 6 independently configurable channels and each channel FIFO depth is 16 x 32 bits
- Non-AHB peripheral devices can request a DMA transfer through hardware handshaking interface
- Programmable channel priority
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral transfers
- Support for single block transfer with configurable block size up to 4095 bytes
- Programmable burst transaction size for source and destination
- Programmable source and destination addresses stepping level
  - Increase to the next word-aligned address
  - Decrease to the next word-aligned address
  - Free the address
- Two interrupt sources with flags:
  - Transfer complete interrupt
  - Error interrupt

The block diagram is shown in Figure 23-1.

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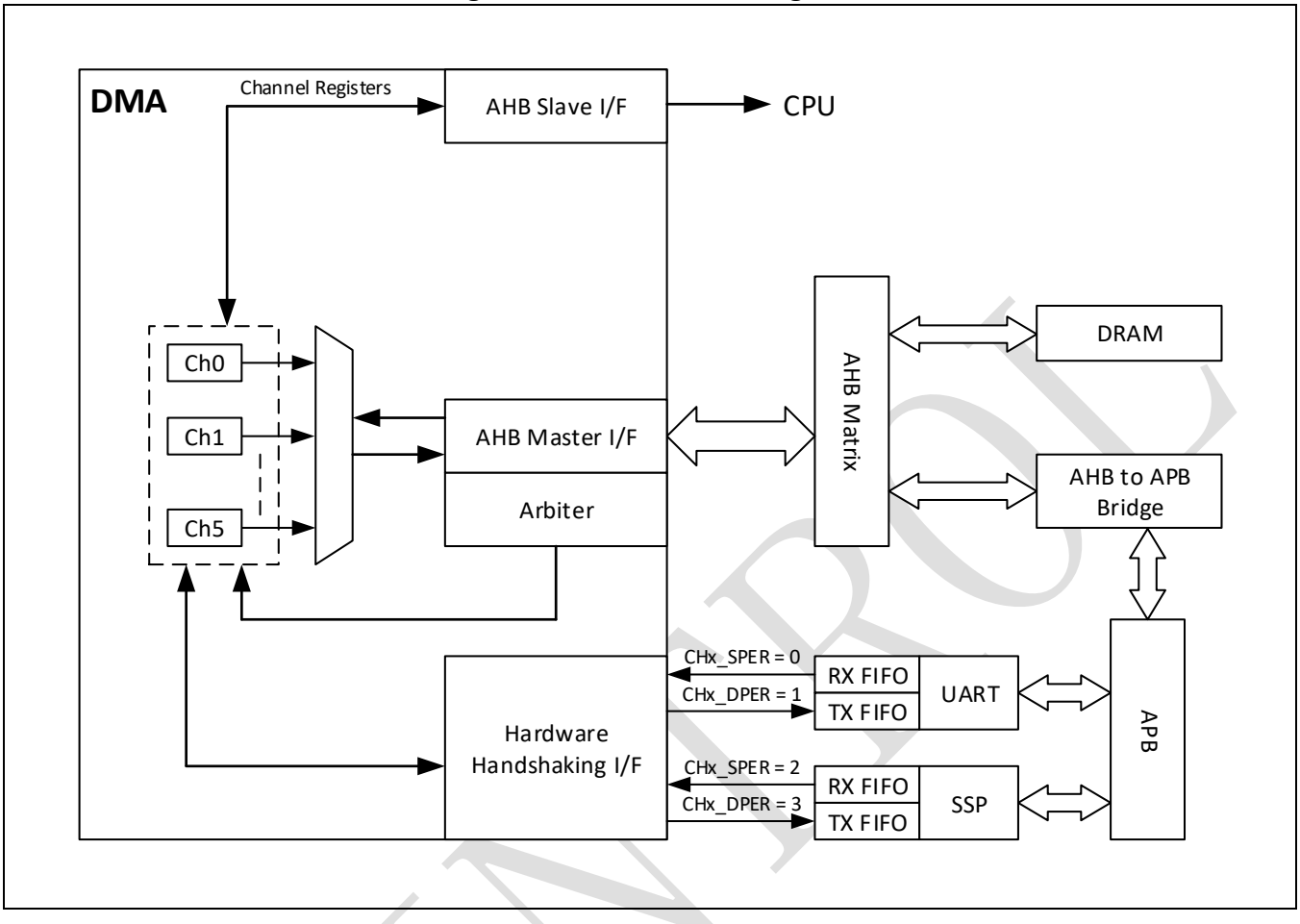
Figure 23-1: DMA block diagram



Note: The address range of DRAM that can be accessed by DMA is 0x2000 0000 ~ 0x2000 3FFF.

SPINTROL

23.3 DMA operation

23.3.1 Basic definitions

The following terms are definitions of the DMA concepts used throughout this chapter.

- **Source** – Device from which DMA reads data. The DMA reads data from source device and then stores the data in the Channel FIFO.
- **Destination** – Device to which the DMA writes the stored data from the FIFO (previously read from the source device).
- **Channel** – Read/write data path between a source device and a destination device.
- **Block** – Block of DMA data, the amount of which is the block size. For transfers between the DMA and memory, a block is directly broken into a sequence of bursts and single transfers. For transfers between the DMA and a peripheral, a block is broken into a sequence of DMA transactions (single and bursts).
- **Transaction** – Basic unit of DMA transfer. A transaction is relevant only for transfers between the DMA and a source or destination device if the device is a non-memory device. There are two types of transactions:
  - Single transaction: Length of a single transaction is always 1 and is converted to a single AHB transfer.
  - Burst transaction: Length of a burst transaction is programmed into the DMA. The burst transaction is converted into a sequence of bursts and AHB single transfers.

23.3.2 Hardware Handshaking interface

DMA hardware handshaking interfaces are used at the transaction level to control the flow of single or burst transactions. When the DMA channel and the peripheral are enabled simultaneously, the hardware handshake interface can automatically complete data transfer.

In SPC2168, the APB bus peripherals (UART and SSP) are connected by the hardware handshake interface with DMA. The connections between DMA channels and UART/SSP module are shown in Table 23-1.

Table 23-1: DMA hardware handshaking interface for UART and SSP

DMACHxCTL3.DPER/ DMACHxCTL3.SPER	Hardware handshaking interface
0	UART_RX
1	UART_TX
2	SSP_RX
3	SSP_TX

The modules that connected to DMA through AHB bus directly, such as DRAM and SIO, have no handshaking interface with the DMA. Once the channel is enabled, the transfer proceeds immediately without waiting for a transaction request.

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Example: Select the channel 2 and 3 hardware handshake port for UART

```
DMACH3->DMACHCTL3.bit.SPER = 0x0; // Select channel 3 for UART_RX
DMACH2->DMACHCTL3.bit.DPER = 0x1; // Select channel 2 for UART_TX
```

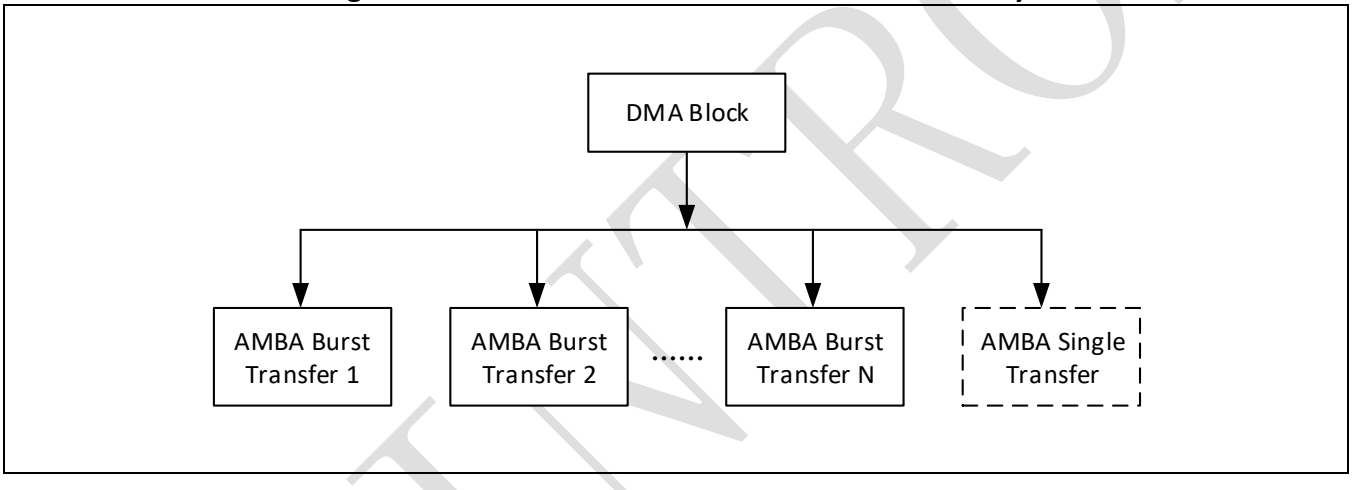
Example: Select the channel 4 and 5 hardware handshake port for SSP

```
DMACH4->DMACHCTL3.bit.DPER = 0x3; // Select channel 4 for SSP_TX
DMACH5->DMACHCTL3.bit.SPER = 0x2; // Select channel 5 for SSP_RX
```

23.3.3 Memory-to-memory transfer operation

DMA supports only single block transfer, and the length of the block can be configured by programming DMACHCTL1.BLKTS. For transfers between the DMA and memory, a block data transfer is directly broken into a sequence of burst and single transfers, as shown in Figure 23-2.

Figure 23-2: Breakdown of DMA transfer for memory



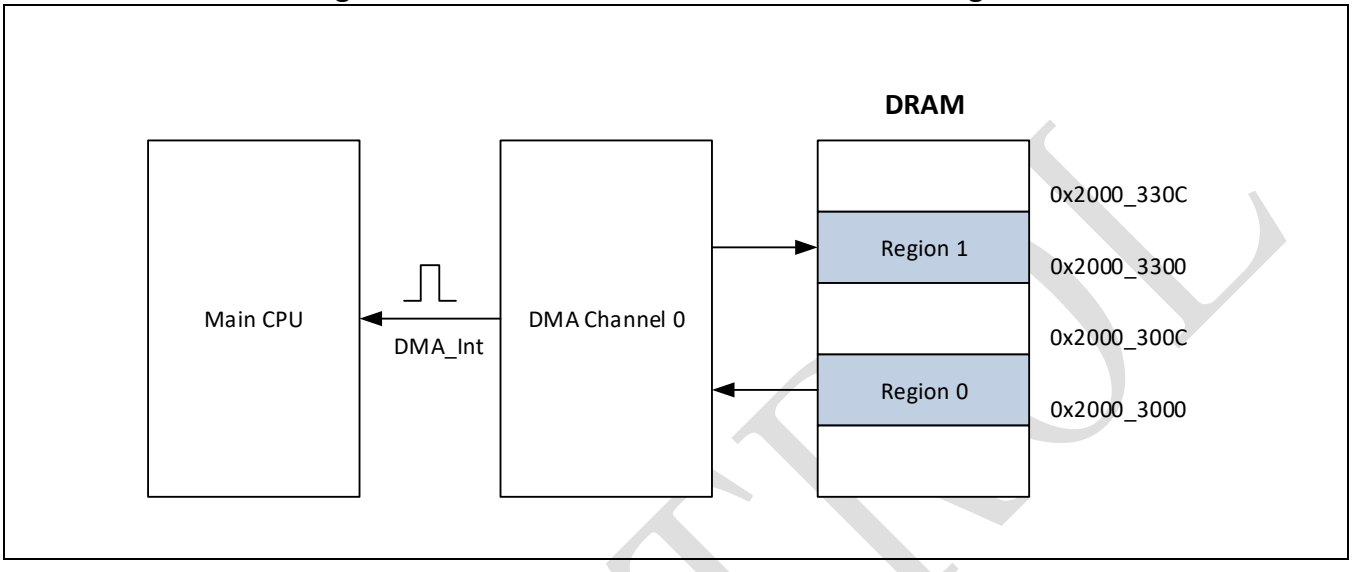
When the block size programmed into the DMA channel is not a multiple of the burst transfer length, as shown in Figure 23-2, a series of burst transfers followed by single transfers are needed to complete the block transfer.

SPINTROL

Example: DMA transfer between two different DRAM regions

The configuration of channel 0: the transfer type is memory-to-memory, the block size is 0xC and the source address and the destination address are incremental mode. The transfer complete interrupt is enabled, and an interrupt will generate to main CPU at the end of the transfer.

Figure 23-3: DMA transfer between two DRAM regions



Example Code

```
// Channel 0 configuration
DMAC->DMATCIE.all      = 0x0101;            // Enable channel 0 tansfer complete int
DMAC->DMAEN.all        = 0x1;               // DMA enable
DMACH0->DMACHSA.all = 0x20003000;           // Source address
DMACH0->DMACHDA.all = 0x20003300;           // Destination address
DMACH0->DMACHCTL0.bit.IE       = 0x1;      // Channel 0 INT enable
DMACH0->DMACHCTL0.bit.DINC     = 0x0;      // Destination address increment
DMACH0->DMACHCTL0.bit.SINC     = 0x0;      // Source address increment
DMACH0->DMACHCTL0.bit.TTFC     = 0x0;      // Memory to memory
DMACH0->DMACHCTL1.bit.BLKTS = 0xC;         // Block size = 12
DMACH0->DMACHEN.all             = 0x0101;  // Enable channel 0


// Run Time (Channel transfer complete triggered ISR call)
//=======================================
if(DMAC->DMATCIF.bit.CH0 == 1)
{
   DMAC->DMATCIC.all = 0x1; // Clear int
}
```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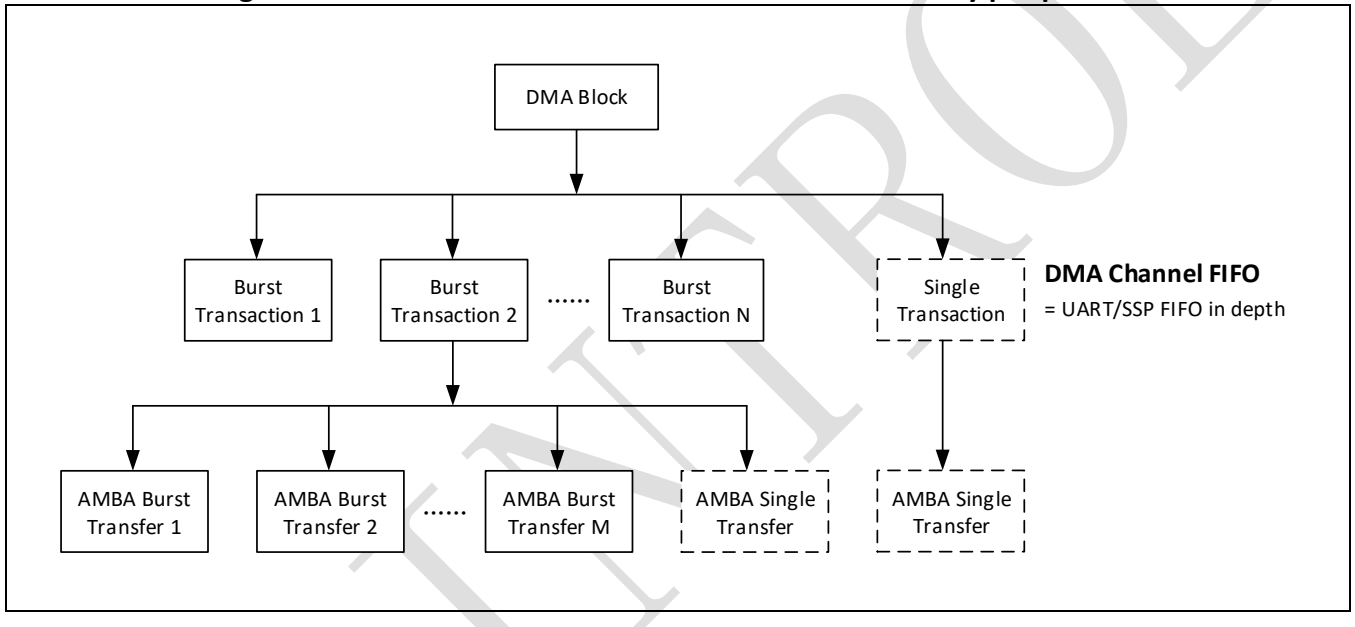
23.3.4 Memory-to-peripheral and Peripheral-to-memory transfer operation

The memory-to-peripheral and peripheral-to-memory are non-memory transfers. For the transfer between DMA and peripheral, the block is broken into a number of transactions (single or burst), each initiated by a request from the peripheral. Then, each transaction is converted to AHB transfers (single or burst) to the non-memory peripheral.

The DMA Controller must also be programmed with the burst transaction length and is programmed into the DMACHCTL0.SSIZE/DSIZE for source and destination, respectively. The burst transaction length is the number of data items (such as UART FIFO entries) to be transferred for each DMA request. Also, the burst transaction length should bear some relationship to the FIFO sizes of the DMA and that of the source and destination peripherals.

Figure 23-4: Breakdown of DMA transfer for non-memory peripherals



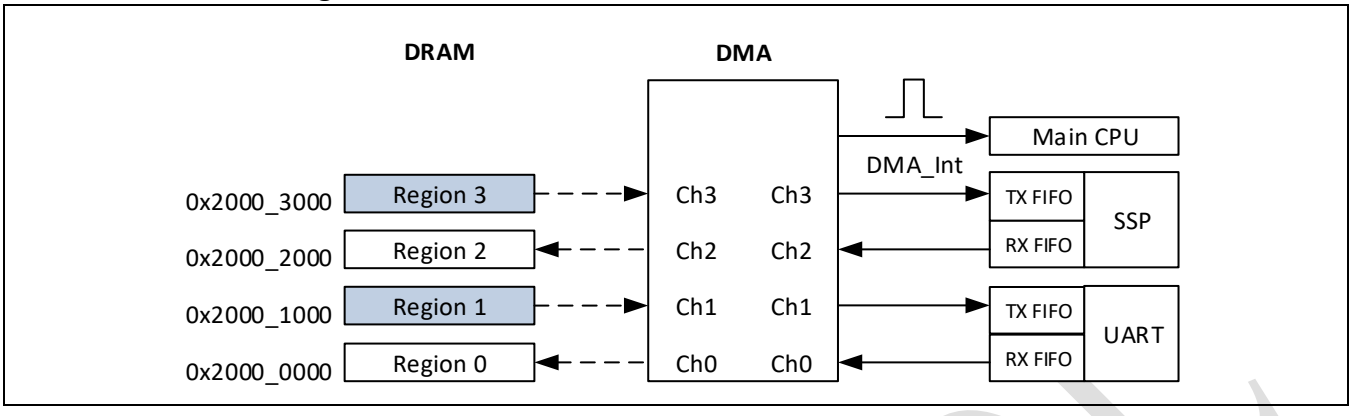
In SPC2168, UART_TX and SSP_TX use memory-to-peripheral operation to complete DMA transfers; UART_RX and SSP_RX use peripheral-to-memory operation to complete DMA transfers. The DMACHCTL.SSIZE and DMACHCTL.DSIZE should be configured according to the FIFO setup in UART and SSP peripherals to avoid FIFO overflow and underflow.

When UART and SSP do not use DMA transfer, although the hardware handshaking interface exists, it does not occupy DMA channel resources, these channels can be used for memory-to-memory transfer.

An example is shown below. The DMA channel 0, 1, 2 and 3 are configured to transfer data between DRAM and UART/SSP. Data is stored in DRAM. An interrupt will generate to main CPU at the end of each channel data transfer.

SPINTROL

Figure 23-5: DMA transfer between DRAM and UART/SSP



Example Code: Configure DMA transfer between memory and UART/SSP

```
// Configure UART
UART->UARTFCR.bit.TRFIFOE      = 0x1;     // FIFO enable
UART->UARTFCR.bit.ITL          = 0x3;     // UART RX FIFO threshold = 8 words
UART->UARTFCR.bit.TIL          = 0x1;     // UART TX FIFO threshold = 0 words
UART->UARTFCR.bit.BUS          = 0x1;     // 32-bit bus
UART->UARTIER.bit.DMAE         = 0x1;     // Enable UART DMA
UART->UARTIER.bit.UUE          = 0x1;     // Enable UART

// Configure channel 0 for UART_RX
DMACH0->DMACHSA.all = 0x40004000;         // UARTRBR address
DMACH0->DMACHDA.all = 0x20000000;         // DRAM region 0 address
DMACH0->DMACHCTL0.bit.TT       = 0x2;     // Peripheral to memory
DMACH0->DMACHCTL0.bit.SSIZE    = 0x2;     // Transaction size = 8 words
DMACH0->DMACHCTL0.bit.SINC     = 0x2;     // Keep source address as UARTRBR register
DMACH0->DMACHCTL0.bit.DINC     = 0x0;     // Increase to next address in DRAM region 0
DMACH0->DMACHCTL0.bit.IE       = 0x1;     // Channel 0 interrupt enable
DMACH0->DMACHCTL1.bit.BLKTS    = 0x10;    // Block size = 16 words
DMACH0->DMACHCTL2.bit.SSWHS    = 0x0;     // Hardware handshaking
DMACH0->DMACHCTL2.bit.SHSPOL = 0x0;       // Active high
DMACH0->DMACHCTL3.bit.SPER     = 0x0;     // Channel 0 select UART RX as source

// Configure channel 1 for UART_TX
DMACH1->DMACHSA.all = 0x20001000;         // DRAM region 1 address
DMACH1->DMACHDA.all = 0x40004000;         // UARTTHR address
DMACH1->DMACHCTL0.bit.TT       = 0x1;     // Memory to peripheral
DMACH1->DMACHCTL0.bit.DSIZE    = 0x3;     // Transaction size = 16 words
DMACH1->DMACHCTL0.bit.SINC     = 0x0;     // Increase to next address in DRAM region 1
DMACH1->DMACHCTL0.bit.DINC     = 0x2;     // Keep destination address as UARTTHR
DMACH1->DMACHCTL0.bit.IE       = 0x1;     // Channel 1 interrupt enable
DMACH1->DMACHCTL1.bit.BLKTS    = 0x10;    // Block size = 16 words
DMACH1->DMACHCTL2.bit.DSWHS    = 0x0;     // Hardware handshaking
DMACH1->DMACHCTL2.bit.DSHPOL = 0x0;       // Active high
DMACH1->DMACHCTL3.bit.DPER     = 0x1;     // Channel 1 select UART TX as destionation

// Configure SSP FIFO
SSP->SSPCTL1.bit.DMARXEN       = 0x1;     // SSP RX DMA enable
SSP->SSPCTL1.bit.DMATXEN       = 0x1;     // SSP TX DMA enable
SSP->SSPCTL1.bit.RFTH          = 0x7;     // SSP RX FIFO threshold >= 8 words
```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Example Code: Configure DMA transfer between memory and UART/SSP

```
SSP->SSPCTL1.bit.TFTH          = 0x8;     // SSP TX FIFO threshold <= 8 words

// Configure channel 2 for SSP_RX
DMACH2->DMACHSA.all = 0x40005010;        // SSPDATA register address
DMACH2->DMACHDA.all = 0x20002000;        // DRAM region 2 address
DMACH2->DMACHCTL0.bit.TT       = 0x2;    // Peripheral to Memory
DMACH2->DMACHCTL0.bit.SSIZE    = 0x2;    // Transaction size = 8 words
DMACH2->DMACHCTL0.bit.SINC     = 0x2;    // Keep source address as SSPDATA register
DMACH2->DMACHCTL0.bit.DINC     = 0x0;    // Increase to next address in DRAM region 2
DMACH2->DMACHCTL0.bit.IE       = 0x1;    // Enable channel 2 interrupt
DMACH2->DMACHCTL1.bit.BLKTS    = 0x8;    // Block size = 8 words
DMACH2->DMACHCTL2.bit.SSWHS    = 0x0;    // Hardware handshaking
DMACH2->DMACHCTL2.bit.SHSPOL = 0x0;      // Active high
DMACH2->DMACHCTL3.bit.SPER     = 0x2;    // Channel 2 select SSP RX

// Configure channel 3 for SSP_TX
DMACH3->DMACHSA.all = 0x2003000;         // DRAM region 3 address
DMACH3->DMACHDA.all = 0x40005010;        // SSPDATA register address
DMACH3->DMACHCTL0.bit.TT       = 0x1;    // Memory to Peripheral
DMACH3->DMACHCTL0.bit.SINC     = 0x0;    // Increase to next address in DRAM region 3
DMACH3->DMACHCTL0.bit.DINC     = 0x2;    // Keep destination address as SSPDATA
DMACH3->DMACHCTL0.bit.DSIZE    = 0x2;    // Transaction size = 8 words
DMACH3->DMACHCTL0.bit.IE       = 0x1;    // Enable channel 3 interrupt
DMACH3->DMACHCTL1.bit.BLKTS    = 0x11;   // Block size = 17 words
DMACH3->DMACHCTL2.bit.DSWHS    = 0x0;    // Hardware handshaking
DMACH3->DMACHCTL2.bit.DSHPOL = 0x0;      // Active high
DMACH3->DMACHCTL3.bit.DPER     = 0x3;    // Channel 3 select SSP TX

DMAC->DMATCIE.all              = 0xf0f; // Enable channel 0-3 transfer complete int
DMAC->DMAEN.all                = 0x1;    // DMA enable
DMAC->DMACHEN.all              = 0xf0f; // Channel 0/1/2/3 enable

// Run Time (Channel transfer complete triggered ISR call)
//=========================================
while(DMAC->DMATCIF.all != 0xf);
DMAC->DMATCIC.all     = 0xf;             // Clear the interrupt
```

23.3.5 Peripheral-to-peripheral transfer operation

The peripheral-to-peripheral transfer in SPC2168 provides a physical communication channel from UART_RX to SSP_TX or from SSP_RX to UART_TX.

An example is shown below to demonstrate the SSP_RX to UART_TX transfer via DMA channel 0. Please notice that the communication data rate should be carefully chosen for both the SSP and UART to avoid FIFO overflow or underflow.

Example Code: Configure DMA transfer between UART and SSP

```
// Configure UART
UART->UARTFCR.bit.TRFIFOE      = 0x1;    // FIFO enable
UART->UARTFCR.bit.TIL          = 0x1;    // UART TX FIFO threshold = 0 words
UART->UARTFCR.bit.BUS          = 0x1;    // 32-bit bus
UART->UARTIER.bit.DMAE         = 0x1;    // Enable UART DMA
```

SPINTROL

Example Code: Configure DMA transfer between UART and SSP

```
UART->UARTIER.bit.UUE              = 0x1;      // Enable UART

// Configure SSP FIFO
SSP->SSPCTL1.bit.DMARXEN          = 0x1;      // SSP RX DMA enable
SSP->SSPCTL1.bit.RFTH             = 0x7;      // SSP RX FIFO threshold >= 8 words

// Configure channel 0 for SSP_RX to UART_TX
DMACH0->DMACHSA.all = 0x40005010;          // SSPDATA register address
DMACH0->DMACHDA.all = 0x40004000;          // UARTTHR address
DMACH0->DMACHCTL0.bit.TT          = 0x3;      // Peripheral to peripheral
DMACH0->DMACHCTL0.bit.SSIZE       = 0x2;      // Transaction size = 8 words
DMACH0->DMACHCTL0.bit.SINC        = 0x2;      // Keep source address as SSPDATA register
DMACH0->DMACHCTL0.bit.DINC        = 0x2;      // Keep destination address as UARTTHR
DMACH0->DMACHCTL0.bit.IE          = 0x1;      // Channel 0 interrupt enable
DMACH0->DMACHCTL1.bit.BLKTS       = 0x10;     // Block size = 16 words
DMACH0->DMACHCTL2.bit.SSWHS       = 0x0;      // Hardware handshaking
DMACH0->DMACHCTL2.bit.SHSPOL = 0x0;      // Active high
DMACH0->DMACHCTL3.bit.SPER        = 0x2;      // Select SSP RX as source
DMACH0->DMACHCTL3.bit.DPER        = 0x1;      // Select UART TX as destionation

DMAC->DMATCIE.all                  = 0x101; // Enable channel 0 transfer complete int
DMAC->DMAEN.all                    = 0x1;      // DMA enable
DMAC->DMACHEN.all                  = 0x101; // Channel 0 enable

// Run Time (Channel transfer complete triggered ISR call)
//=======================================
while(DMAC->DMATCIF.bit.CH0 != 0x1);
DMAC->DMATCIC.all      = 0x1;                  // Clear the interrupt
```

23.4 AHB Transfer Error Handling

Upon occurrence of an error in an AHB transfer, the following occurs:

- DMA transfer in progress stops immediately
- Relevant channel is disabled.
- If enabled, an interrupt is issued.

If multiple channels are enabled, only the one where the AHB error was detected is disabled. The contents of the FIFO becomes inaccessible and are overwritten once the channel is re-enabled to start a new sequence.

There is no support for automatically resuming the transfer from the point where the error occurred, and the full block transfer has to be re-initiated in order to be successfully completed.

The DMA does not use the hardware handshaking interface to signal the error occurrence, nor does it signal the end of the transfer. Therefore, if the request from a peripheral is active when the error occurs, it would not be automatically de-activated by DMA acknowledge. The hardware handshake interface on the peripheral side has to be reset or re-initiated by software upon the error interrupt. The DMA request signal needs to be brought low before the channel is re-enabled.

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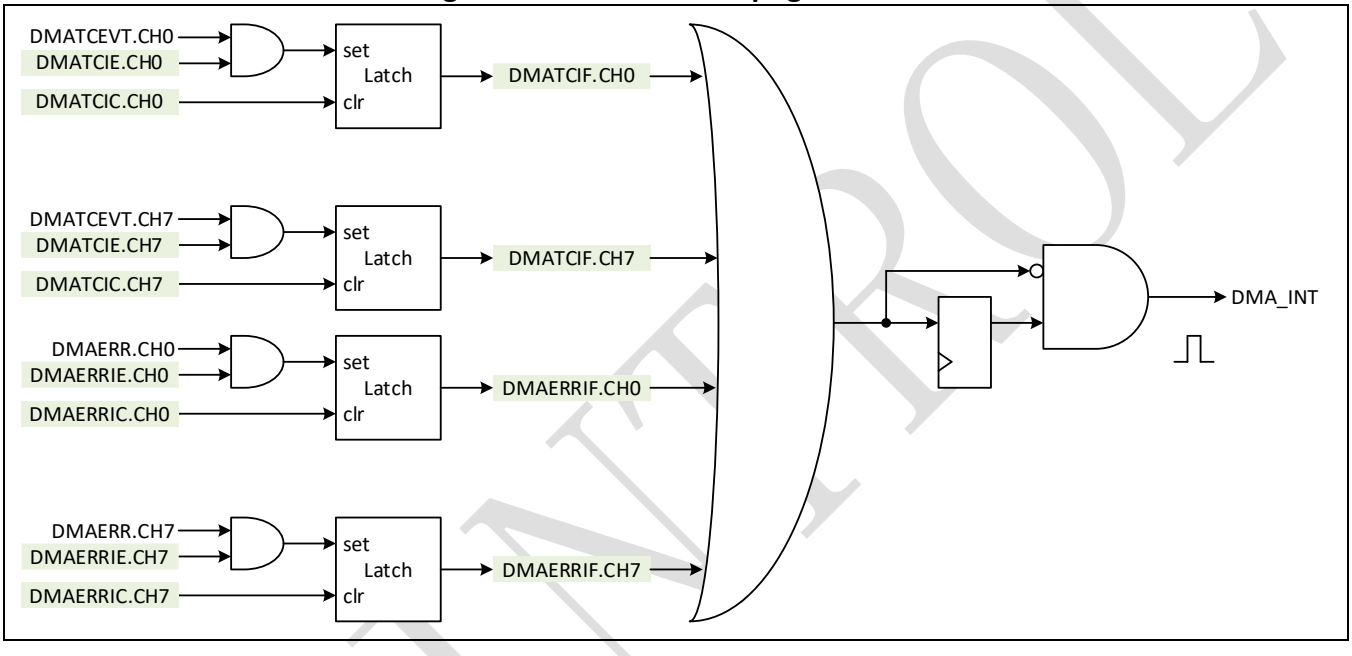
23.5 Interrupt handling

When the DMA transfer completes for channel x, the event is latched to DMATCRAWIF.CHx. If it is enabled by setting DMATCIE.CHx as 1, an interrupt request can be generated and latched to DMATCIF.CHx. Writing 1 to DMATCIC clears both the DMATCRAWIF.CHx and DMATCIF.CHx.

When an ERROR response is received from an AHB slave during a DMA transfer for channel x, DMA transfer is cancelled and the channel is disabled. The event is latched to DMAERRRAWIF.CHx. If it is enabled by setting DMAERRIE.CHx as 1, an interrupt request can be generated and latched to DMAERRIF.CHx. Writing 1 to DMAERRIC clears both the DMAERRRAWIF.CHx and DMAERRIF.CHx.

Figure 23-6: DMA interrupt generation



As shown in Figure 23-6, the interrupt flag bits are combined together to generate the final single interrupt to the CPU. It can be seen that the interrupt flag bits would block the interrupt issuing to the CPU until they are all cleaned.

Based on the structure, it is recommended to implement the ISR (interrupt service routine) as the pseudo-code shown in Figure 23-7.

Figure 23-7: Pseduo-code for DMA ISR

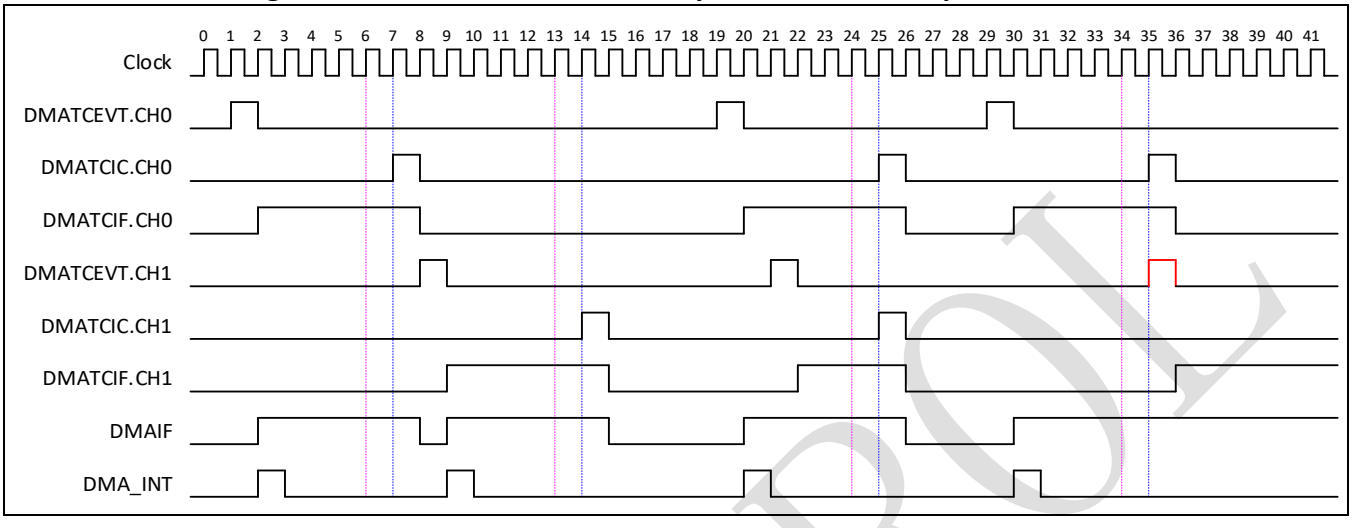
```
u32TCFlag = DMAC->DMATCIF;
DMAC->DMATCIC = u32TCFlag; // Make sure it will not be interrupt here by ISR with higher priority
u32ErrFlag = DMAC->DMAERRIF;
DMAC->DMAERRIC = u32ErrFlag; // Make sure it will not be interrupt here by ISR with higher priority
if ((u32TCFlag & 1U) !=0) { // Code to handle channel 0 transfer completion }
if ((u32TCFlag & 2U) !=0) { // Code to handle channel 1 transfer completion }
…
if ((u32ErrFlag & 1U) !=0) { // Code to handle channel 0 transfer error }
if ((u32ErrFlag & 2U) !=0) { // Code to handle channel 1 transfer error }
```

SPINTROL

23.5.1Risk mitigation for interrupt loss and blocking

Figure 23-8 illustrates various scenario when DMA interrupts are enabled for multiple channels.

Figure 23-8: Scenario DMA interrupt events for multiple channels



- ISR entry is triggered independently by request from each channel. Therefore, there is no interrupt loss or double serve.
  - Transfer of channel 0 completes at t_1, and triggers the interrupt request. DMATCIF.CH0 is set accordingly.
  - The software reads the DMATCIF in the ISR at t_6, and finds that only DMATCIF.CH0 is set. Then it clears the flag at t_7 accordingly to enable the new interrupt coming later. After that, it serves the request from channel 0.
  - Transfer of channel 1 completes at t_8, and triggers the interrupt request. DMATCIF.CH1 is set accordingly.
  - Since there is no overlap between the DMATCIF.CH0 and DMATCIF.CH1, a rising edge can be recognized in the combined DMAIF signal, and a new interrupt pulse is issued to the CPU. Therefore, when the software exits the ISR, it will enter the ISR again.
  - The software reads the DMATCIF in the ISR at t_{13}, and finds that only DMATCIF.CH1 is set. Then it clears the flag at t_{14} accordingly to enable the new interrupt coming later. After the request from channel 1 is served, it exits the ISR.
- ISR entry is triggered by request from one channel but multiple requests are served within the ISR. Therefore, there is no interrupt loss or double serve.
  - Transfer of channel 0 completes at t_{19}, and triggers the interrupt request. DMATCIF.CH0 is set accordingly.
  - Before the software reads the DMATCIF in the ISR at t_{24}, transfer of channel 1 completes at t_{21}. Therefore, the software will find that both DMATCIF.CH0 and DMATCIF.CH1 are set at t_{24}, and clear them at t_{25} accordingly to enable the new interrupt coming later. After the requests from both channel 0 and channel 1 are served, it exits the ISR.
- New interrupt request comes after the interrupt flag readout in the ISR but before the interrupt clear, leading to the interrupt loss and blocking for future interrupts.
  - Transfer of channel 0 completes at t_{29}, and triggers the DMA interrupt. DMATCIF.CH0 is set accordingly.
  - The software reads the DMATCIF in the ISR at t_{34} and find that only DMATCIF.CH0 is set. Then it

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clears the flag at t_{35} accordingly to enable the new interrupt coming later, and starts to serve for channel 0

- Transfer of channel 1 completes at t_{35}, and triggers the interrupt request. DMATCIF.CH1 is set accordingly.
- Since DMATCIF.CH0 is cleared at the same time when DMATCIF.CH1 is set, there will be no rising edge in the combined DMAIF signal. So no new interrupt pulse will be issued to the CPU.
- There is no chance for the clearance of DMATCIF.CH1 since CPU is unware of this situation. **The combined DMAIF is always 1 and DMA interrupt pulse will not be generated any more.**

Based on the analysis above, it causes problem when the new interrupt request comes after the flag readout and before the flag clear. To minimize the risk, this time window should be as small as possible. The coding style shown in Figure 23-7 reduces the window to only 1 clock cycle, but there is still potential risk as shown in Figure 23-8. To fully solve the problem, user need to check the DMA interrupt flag periodically (i.e. in the ISR of a timer) and take actions.

SPINTROL

23.6 Registers

23.6.1 DMACH register map

Table 23-2: DMACH Module Base Address

Peripheral Module	Base Address
DMACH0	0x4000 A400
DMACH1	0x4000 A458
DMACH2	0x4000 A4B0
DMACH3	0x4000 A508
DMACH4	0x4000 A560
DMACH5	0x4000 A5B8

Table 23-3: DMACH Register Map

Register	Offset	Description	Reset Value
DMACHSA	0x00	DMA Channel Source Address Register	0x00000000
DMACHDA	0x08	DMA Channel Destination Address Register	0x00000000
DMACHCTL0	0x18	DMA Channel Control Register 0	0x00304825
DMACHCTL1	0x1C	DMA Channel Control Register 1	0x00000002
DMACHCTL2	0x40	DMA Channel Control Register 2	0x00000E00
DMACHCTL3	0x44	DMA Channel Control Register 3	0x00000004

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23.6.2 DMACH registers

23.6.2.1 DMA Channel Source Address Register (DMACHSA)

Table 23-4: DMA Channel Source Address Register (DMACHSA) Layout

DMACHSA (DMA Channel Source Address Register) Offset: 0x0 Default: 0x00000000 Access: DMACHx -> DMACHSA.all							
31	30	29	28	27	26	25	24
ADDR							
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

Table 23-5: DMA Channel Source Address Register (DMACHSA) Field Description

Bits	Field Name	Type	Reset	Description
31:0	ADDR	RW	0x0	Current source address of DMA transfer. This register must be written with a 32-bit aligned address. It is updated after each source transfer according to DMACHCTL0.SINC

23.6.2.2 DMA Channel Destination Address Register (DMACHDA)

Table 23-6: DMA Channel Destination Address Register (DMACHDA) Layout

DMACHDA (DMA Channel Destination Address Register) Offset: 0x8 Default: 0x00000000 Access: DMACHx -> DMACHDA.all							
31	30	29	28	27	26	25	24
ADDR							
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

Table 23-7: DMA Channel Destination Address Register (DMACHDA) Field Description

Bits	Field Name	Type	Reset	Description
31:0	ADDR	RW	0x0	Current destination address of DMA transfer. This register must be written with a 32-bit aligned address. It is updated after each source transfer according to DMACHCTL0.DINC

SPINTROL

23.6.2.3 DMA Channel Control Register 0 (DMACHCTL0)

Table 23-8: DMA Channel Control Register 0 (DMACHCTL0) Layout

DMACHCTL0 (DMA Channel Control Register 0) Offset: 0x18 Default: 0x00304825
Access: DMACHx -> DMACHCTL0.all

31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED		TT		RESERVED			SSIZE
15	14	13	12	11	10	9	8
SSIZE		DSIZE			SINC		DINC
7	6	5	4	3	2	1	0
DINC	SWIDTH			DWIDTH			IE

Table 23-9: DMA Channel 0 Control Register 0 (DMACH0CTL0) Field Description

Bits	Field Name	Type	Reset	Description
31:22	RESERVED_31_22	RO	0x0	Reserved
21:20	TT	RW	0x3	Transfer type 00: Memory to memory 01: Memory to peripheral 10: Peripheral to memory 11: Peripheral to peripheral i.e. UART_RX to SSP_TX or SSP_RX to UART_TX.
19:17	RESERVED_19_17	RO	0x0	Reserved
16:14	SSIZE	RW	0x1	Source burst transaction size This value is not related to the AHB HBURST signal 000: 1 word 001: 4 words 010: 8 words 011: 16 words 100: 32 words 101: 64 words 110: 128 words 111: 256 words
13:11	DSIZE	RW	0x1	Destination burst transaction size This value is not related to the AHB HBURST signal 000: 1 word 001: 4 words 010: 8 words 011: 16 words 100: 32 words 101: 64 words 110: 128 words 111: 256 words

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Bits	Field Name	Type	Reset	Description
10:9	SINC	RW	0x0	Source address increment after each transfer 00: Increase to the next word-aligned address 01: Decrease to the next word-aligned address 10: Freeze the address 11: Invalid
8:7	DINC	RW	0x0	Destination address increment after each transfer 00: Increase to the next word-aligned address 01: Decrease to the next word-aligned address 10: Freeze the address 11: Invalid
6:4	SWIDTH	RO	0x2	Always readback 0x2 to indicate the source transfer width is 32-bit
3:1	DWIDTH	RO	0x2	Always readback 0x2 to indicate the destination transfer width is 32-bit
0	IE	RW	0x1	Interrupt enable This bit does not affect the raw interrupt flag generation 0: Disable interrupt generation 1: Enable interrupt generation

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23.6.2.4 DMA Channel Control Register 1 (DMACHCTL1)

Table 23-10: DMA Channel Control Register 1 (DMACHCTL1) Layout

DMACHCTL1 (DMA Channel Control Register 1) Offset: 0x1C Default: 0x00000002 Access: DMACHx -> DMACHCTL1.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED			RESERVED	BLKTS			
7	6	5	4	3	2	1	0
BLKTS							

Table 23-11: DMA Channel Control Register 1 (DMACHCTL1) Field Description

Bits	Field Name	Type	Reset	Description
31:13	RESERVED_31_13	RO	0x0	Reserved
12	RESERVED_12	RW	0x0	Reserved
11:0	BLKTS	RW	0x2	Block transfer size, which is the total number of single transactions to perform for every block transfer. This field must be written before the channel is enabled in order to indicate the block size.

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23.6.2.5 DMA Channel Control Register 2 (DMACHCTL2)

Table 23-12: DMA Channel Control Register 2 (DMACHCTL2) Layout

DMACHCTL2 (DMA Channel Control Register 2) Offset: 0x40 Default: 0x00000E00 Access: DMACHx -> DMACHCTL2.all							
31	30	29	28	27	26	25	24
RESERVED_31_20							
23	22	21	20	19	18	17	16
RESERVED_31_20				SHSPOL	DHSPOL	RESERVED_17_12	
15	14	13	12	11	10	9	8
RESERVED_17_12				SSWHS	DSWHS	FIFOEMPTY	SUSPEND
7	6	5	4	3	2	1	0
PRIORITY			RESERVED_4_0				

Table 23-13: DMA Channel Control Register 2 (DMACHCTL2) Field Description

Bits	Field Name	Type	Reset	Description
31:20	RESERVED_31_20	RO	0x0	Reserved
19	SHSPOL	RW	0x0	Source handshaking interface polarity 0: Active high 1: Active low
18	DSHPOL	RW	0x0	Destination handshaking interface polarity 0: Active high 1: Active low
17:12	RESERVED_17_12	RO	0x0	Reserved
11	SSWHS	RW	0x1	Source software handshaking select This bit is ignored if the source is memory. 0: Hardware handshaking 1: Software handshaking
10	DSWHS	RW	0x1	Destination software handshaking select This bit is ignored if the destination is memory. 0: Hardware handshaking 1: Software handshaking
9	FIFOEMPTY	RO	0x1	Indicates if there is data left in the channel FIFO. This bit can be used in conjunction with SUSPEND to cleanly disable a channel. 0: There is data left in the channel FIFO 1: Channel FIFO is fully empty
8	SUSPEND	RW	0x0	Channel Suspend Suspends all DMA data transfers from the source until this bit is cleared. There is no guarantee that the current transaction will complete.

SPINTROL

Bits	Field Name	Type	Reset	Description
				This bit can also be used in conjunction with FIFOEMPTY to cleanly disable a channel without losing any data. 0: Channel is in operation 1: Suspend the channel
7:5	PRIORITY	RW	0x0	Channel priority 000: 6th priority (Lowest) 001: 5th priority 010: 4th priority 011: 3rd priority 100: 2nd priority 101: 1st priority (Highest) Others: Invalid
4:0	RESERVED_4_0	RO	0x0	Reserved

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23.6.2.6 DMA Channel Control Register 3 (DMACHCTL3)

Table 23-14: DMA Channel Control Register 3 (DMACHCTL3) Layout

DMACHCTL3 (DMA Channel Control Register 3) Offset: 0x44 Default: 0x00000004 Access: DMACHx -> DMACHCTL3.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED			DPER		RESERVED		SPER
7	6	5	4	3	2	1	0
SPER	RESERVED		RESERVED			FIFOTH	RESERVED

Table 23-15: DMA Channel Control Register 3 (DMACHCTL3) Field Description

Bits	Field Name	Type	Reset	Description
31:13	RESERVED_31_13	RO	0x0	Reserved
12:11	DPER	RW	0x0	Destination peripheral that communicated through hardware handshaking interface. This field is ignored if DMACHCT2.DSWHS=1 01: Hardware handshaking interface is UART_TX 11: Hardware handshaking interface is SSP_TX Others: Invalid
10:9	RESERVED_10_9	RO	0x0	Reserved
8:7	SPER	RW	0x0	Source peripheral that communicated through hardware handshaking interface. This field is ignored if DMACHCT2.SSWHS=1 00: Hardware handshaking interface is UART_RX 10: Hardware handshaking interface is SSP_RX Others: Invalid
6:5	RESERVED_6_5	RO	0x0	Reserved
4:2	RESERVED_4_2	RW	0x1	Reserved
1	FIFOTH	RW	0x0	FIFO threshold to determine how much space or data needs to be available in the FIFO before a burst transaction request is serviced. 0: Transfer whenever data is available in the FIFO 1: Destination transfer will not start until data available is great than or equal to 8 words. Source transfer will not start until data available is greater than 8 words. The exceptions are at the end of a burst transaction request or at the end of a block transfer
0	RESERVED_0	RW	0x0	Reserved

SPINTROL

23.6.3 DMAC register map

Table 23-16: DMAC Module Base Address

Peripheral Module	Base Address
DMAC	0x4000 A400

Table 23-17: DMAC Register Map

Register	Offset	Description	Reset Value
DMATCRAWIF	0x2C0	DMA Transfer Complete Raw Interrupt Flag Register	0x00000000
DMAERRRAWIF	0x2E0	DMA Error Raw Interrupt Flag Register	0x00000000
DMATCIF	0x2E8	DMA Transfer Complete Interrupt Flag Register	0x00000000
DMAERRIF	0x308	DMA Error Interrupt Flag Register	0x00000000
DMATCIE	0x310	DMA Transfer Complete Interrupt Enable Register	0x00000000
DMAERRIE	0x330	DMA Error Interrupt Enable Register	0x00000000
DMATCIC	0x338	DMA Transfer Complete Interrupt Clear Register	0x00000000
DMAERRIC	0x358	DMA Error Interrupt Clear Register	0x00000000
DMAIF	0x360	DMA Combined Interrupt Flag Register	0x00000000
DMAEN	0x398	DMA Enable Register	0x00000000
DMACHEN	0x3A0	DMA Channel Enable Register	0x00000000

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23.6.4 DMAC registers

23.6.4.1 DMA Transfer Complete Raw Interrupt Flag Register (DMATCRAWIF)

Table 23-18: DMA Transfer Complete Raw Interrupt Flag Register (DMATCRAWIF) Layout

DMATCRAWIF (DMA Transfer Complete Raw Interrupt Flag Register) Offset: 0x2C0 Default: 0x00000000 Access: DMAC -> DMATCRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-19: DMA Transfer Complete Raw Interrupt Flag Register (DMATCRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	CH5	RW[1]	0x0	Channel 5 transfer complete raw interrupt flag 0: Transfer not completed 1: Transfer completed
4	CH4	RW[1]	0x0	Channel 4 transfer complete raw interrupt flag 0: Transfer not completed 1: Transfer completed
3	CH3	RW[1]	0x0	Channel 3 transfer complete raw interrupt flag 0: Transfer not completed 1: Transfer completed
2	CH2	RW[1]	0x0	Channel 2 transfer complete raw interrupt flag 0: Transfer not completed 1: Transfer completed
1	CH1	RW[1]	0x0	Channel 1 transfer complete raw interrupt flag 0: Transfer not completed 1: Transfer completed
0	CH0	RW[1]	0x0	Channel 0 transfer complete raw interrupt flag 0: Transfer not completed 1: Transfer completed

[1] Write access is available to these registers for software testing purposes only. Under normal operation, writes to these registers are not recommended.

SPINTROL

23.6.4.2 DMA Error Raw Interrupt Flag Register (DMAERRRAWIF)

Table 23-20: DMA Error Raw Interrupt Flag Register (DMAERRRAWIF) Layout

DMAERRRAWIF (DMA Error Raw Interrupt Flag Register) Offset: 0x2E0 Default: 0x00000000 Access: DMAC -> DMAERRRAWIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-21: DMA Error Raw Interrupt Flag Register (DMAERRRAWIF) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	CH5	RW[1]	0x0	Channel 5 error raw interrupt flag 0: Error not occurred 1: Error occurred
4	CH4	RW[1]	0x0	Channel 4 error raw interrupt flag 0: Error not occurred 1: Error occurred
3	CH3	RW[1]	0x0	Channel 3 error raw interrupt flag 0: Error not occurred 1: Error occurred
2	CH2	RW[1]	0x0	Channel 2 error raw interrupt flag 0: Error not occurred 1: Error occurred
1	CH1	RW[1]	0x0	Channel 1 error raw interrupt flag 0: Error not occurred 1: Error occurred
0	CH0	RW[1]	0x0	Channel 0 error raw interrupt flag 0: Error not occurred 1: Error occurred

[1] Write access is available to these registers for software testing purposes only. Under normal operation, writes to these registers are not recommended.

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23.6.4.3 DMA Transfer Complete Interrupt Flag Register (DMATCIF)

Table 23-22: DMA Transfer Complete Interrupt Flag Register (DMATCIF) Layout

DMATCIF (DMA Transfer Complete Interrupt Flag Register) Offset: 0x2E8 Default: 0x00000000 Access: DMAC -> DMATCIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-23: DMA Transfer Complete Interrupt Flag Register (DMATCIF) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	CH5	RO	0x0	Channel 5 transfer complete interrupt flag 0: Transfer complete interrupt not occurred 1: Transfer complete interrupt occurred
4	CH4	RO	0x0	Channel 4 transfer complete interrupt flag 0: Transfer complete interrupt not occurred 1: Transfer complete interrupt occurred
3	CH3	RO	0x0	Channel 3 transfer complete interrupt flag 0: Transfer complete interrupt not occurred 1: Transfer complete interrupt occurred
2	CH2	RO	0x0	Channel 2 transfer complete interrupt flag 0: Transfer complete interrupt not occurred 1: Transfer complete interrupt occurred
1	CH1	RO	0x0	Channel 1 transfer complete interrupt flag 0: Transfer complete interrupt not occurred 1: Transfer complete interrupt occurred
0	CH0	RO	0x0	Channel 0 transfer complete interrupt flag 0: Transfer complete interrupt not occurred 1: Transfer complete interrupt occurred

SPINTROL

23.6.4.4 DMA Error Interrupt Flag Register (DMAERRIF)

Table 23-24: DMA Error Interrupt Flag Register (DMAERRIF) Layout

DMAERRIF (DMA Error Interrupt Flag Register) Offset: 0x308 Default: 0x00000000 Access: DMAC -> DMAERRIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-25: DMA Error Interrupt Flag Register (DMAERRIF) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	CH5	RO	0x0	Channnel 5 error interrupt flag 0: Error interrupt not occurred 1: Error interrupt occurred
4	CH4	RO	0x0	Channnel 5 error interrupt flag 0: Error interrupt not occurred 1: Error interrupt occurred
3	CH3	RO	0x0	Channnel 5 error interrupt flag 0: Error interrupt not occurred 1: Error interrupt occurred
2	CH2	RO	0x0	Channnel 5 error interrupt flag 0: Error interrupt not occurred 1: Error interrupt occurred
1	CH1	RO	0x0	Channnel 5 error interrupt flag 0: Error interrupt not occurred 1: Error interrupt occurred
0	CH0	RO	0x0	Channnel 5 error interrupt flag 0: Error interrupt not occurred 1: Error interrupt occurred

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23.6.4.5 DMA Transfer Complete Interrupt Enable Register (DMATCIE)

Table 23-26: DMA Transfer Complete Interrupt Enable Register (DMATCIE) Layout

DMATCIE (DMA Transfer Complete Interrupt Enable Register) Offset: 0x310 Default: 0x00000000 Access: DMAC -> DMATCIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED		CH5WE	CH4WE	CH3WE	CH2WE	CH1WE	CH0WE
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-27: DMA Transfer Complete Interrupt Enable Register (DMATCIE) Field Description

Bits	Field Name	Type	Reset	Description
31:14	RESERVED_31_14	RO	0x0	Reserved
13	CH5WE	W1S	0x0	CH5 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
12	CH4WE	W1S	0x0	CH4 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
11	CH3WE	W1S	0x0	CH3 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
10	CH2WE	W1S	0x0	CH2 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
9	CH1WE	W1S	0x0	CH1 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
8	CH0WE	W1S	0x0	CH0 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
7:6	RESERVED_7_6	RO	0x0	Reserved
5	CH5	RW	0x0	Channel 5 transfer complete interrupt enable 0: Disable : Enable
4	CH4	RW	0x0	Channel 4 transfer complete interrupt enable 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
3	CH3	RW	0x0	Channel 3 transfer complete interrupt enable 0: Disable 1: Enable
2	CH2	RW	0x0	Channel 2 transfer complete interrupt enable 0: Disable 1: Enable
1	CH1	RW	0x0	Channel 1 transfer complete interrupt enable 0: Disable 1: Enable
0	CH0	RW	0x0	Channel 0 transfer complete interrupt enable 0: Disable 1: Enable

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23.6.4.6 DMA Error Interrupt Enable Register (DMAERRIE)

Table 23-28: DMA Error Interrupt Enable Register (DMAERRIE) Layout

DMAERRIE (DMA Error Interrupt Enable Register) Offset: 0x330 Default: 0x00000000 Access: DMAC -> DMAERRIE.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED		CH5WE	CH4WE	CH3WE	CH2WE	CH1WE	CH0WE
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-29: DMA Error Interrupt Enable Register (DMAERRIE) Field Description

Bits	Field Name	Type	Reset	Description
31:14	RESERVED_31_14	RO	0x0	Reserved
13	CH5WE	W1S	0x0	CH5 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
12	CH4WE	W1S	0x0	CH4 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
11	CH3WE	W1S	0x0	CH3 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
10	CH2WE	W1S	0x0	CH2 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
9	CH1WE	W1S	0x0	CH1 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
8	CH0WE	W1S	0x0	CH0 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
7:6	RESERVED_7_6	RO	0x0	Reserved
5	CH5	RW	0x0	Channel 5 error interrupt enable 0: Disable 1: Enable
4	CH4	RW	0x0	Channel 4 error interrupt enable 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
3	CH3	RW	0x0	Channel 3 error interrupt enable 0: Disable 1: Enable
2	CH2	RW	0x0	Channel 2 error interrupt enable 0: Disable 1: Enable
1	CH1	RW	0x0	Channel 1 error interrupt enable 0: Disable 1: Enable
0	CH0	RW	0x0	Channel 0 error interrupt enable 0: Disable 1: Enable

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23.6.4.7 DMA Transfer Complete Interrupt Clear Register (DMATCIC)

Table 23-30: DMA Transfer Complete Interrupt Clear Register (DMATCIC) Layout

DMATCIC (DMA Transfer Complete Interrupt Clear Register) Offset: 0x338 Default: 0x00000000 Access: DMAC -> DMATCIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-31: DMA Transfer Complete Interrupt Clear Register (DMATCIC) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	CH5	W1C	0x0	Channel 5 transfer complete interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
4	CH4	W1C	0x0	Channel 4 transfer complete interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
3	CH3	W1C	0x0	Channel 3 transfer complete interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
2	CH2	W1C	0x0	Channel 2 transfer complete interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
1	CH1	W1C	0x0	Channel 1 transfer complete interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
0	CH0	W1C	0x0	Channel 0 transfer complete interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.

SPINTROL

23.6.4.8 DMA Error Interrupt Clear Register (DMAERRIC)

Table 23-32: DMA Error Interrupt Clear Register (DMAERRIC) Layout

DMAERRIC (DMA Error Interrupt Clear Register) Offset: 0x358 Default: 0x00000000 Access: DMAC -> DMAERRIC.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-33: DMA Error Interrupt Clear Register (DMAERRIC) Field Description

Bits	Field Name	Type	Reset	Description
31:6	RESERVED_31_6	RO	0x0	Reserved
5	CH5	W1C	0x0	Channel 5 error interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
4	CH4	W1C	0x0	Channel 4 error interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
3	CH3	W1C	0x0	Channel 3 error interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
2	CH2	W1C	0x0	Channel 2 error interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
1	CH1	W1C	0x0	Channel 1 error interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.
0	CH0	W1C	0x0	Channel 0 error interrupt clear 0: Write a 0 has no effect and always reads back 0. 1: Write a 1 clears both the RAWIF and IF bit This bit is self-cleared to 0.

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23.6.4.9 DMA Combined Interrupt Flag Register (DMAIF)

Table 23-34: DMA Combined Interrupt Flag Register (DMAIF) Layout

DMAIF (DMA Combined Interrupt Flag Register) Offset: 0x360 Default: 0x00000000 Access: DMAC -> DMAIF.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED			ERROR	RESERVED			TC

Table 23-35: DMA Combined Interrupt Flag Register (DMAIF) Field Description

Bits	Field Name	Type	Reset	Description
31:5	RESERVED_31_5	RO	0x0	Reserved
4	ERROR	RO	0x0	Global error interrupt flag It is the logic OR of the DMAERRIF bits 0: No Error interrupt was generated 1: Error interrupt was generated
3:1	RESERVED_3_1	RO	0x0	Reserved
0	TC	RO	0x0	Global transfer complete interrupt flag It is the logic OR of the DMATCIF bits 0: No transfer complete interrupt was generated 1: Transfer complete interrupt was generated

SPINTROL

23.6.4.10 DMA Enable Register (DMAEN)

Table 23-36: DMA Enable Register (DMAEN) Layout

DMAEN (DMA Enable Register) Offset: 0x398 Default: 0x00000000 Access: DMAC -> DMAEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED							
7	6	5	4	3	2	1	0
RESERVED							EN

Table 23-37: DMA Enable Register (DMAEN) Field Description

Bits	Field Name	Type	Reset	Description
31:1	RESERVED_31_1	RO	0x0	Reserved
0	EN	RW	0x0	DMA enable If this bit is cleared while any channel is still active, the read back keeps 1 to indicate that there are channels still active until hardware has terminated all activity on all channels, at which this bit is 0. 0: Disable 1: Enable

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23.6.4.11 DMA Channel Enable Register (DMACHEN)

Table 23-38: DMA Channel Enable Register (DMACHEN) Layout

DMACHEN (DMA Channel Enable Register) Offset: 0x3A0 Default: 0x00000000 Access: DMAC -> DMACHEN.all							
31	30	29	28	27	26	25	24
RESERVED							
23	22	21	20	19	18	17	16
RESERVED							
15	14	13	12	11	10	9	8
RESERVED		CH5WE	CH4WE	CH3WE	CH2WE	CH1WE	CH0WE
7	6	5	4	3	2	1	0
RESERVED		CH5	CH4	CH3	CH2	CH1	CH0

Table 23-39: DMA Channel Enable Register (DMACHEN) Field Description

Bits	Field Name	Type	Reset	Description
31:14	RESERVED_31_14	RO	0x0	Reserved
13	CH5WE	W1S	0x0	CH5 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
12	CH4WE	W1S	0x0	CH4 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
11	CH3WE	W1S	0x0	CH3 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
10	CH2WE	W1S	0x0	CH2 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
9	CH1WE	W1S	0x0	CH1 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
8	CH0WE	W1S	0x0	CH0 bit write enable 0: Disable 1: Enable. This bit is self-cleared to 0.
7:6	RESERVED_7_6	RO	0x0	Reserved
5	CH5	RW	0x0	Channel 5 enable This bit is self-cleared when transfer is finished. 0: Disable 1: Enable

SPINTROL

Bits	Field Name	Type	Reset	Description
4	CH4	RW	0x0	Channel 4 enable This bit is self-cleared when transfer is finished. 0: Disable 1: Enable
3	CH3	RW	0x0	Channel 3 enable This bit is self-cleared when transfer is finished. 0: Disable 1: Enable
2	CH2	RW	0x0	Channel 2 enable This bit is self-cleared when transfer is finished. 0: Disable 1: Enable
1	CH1	RW	0x0	Channel 1 enable This bit is self-cleared when transfer is finished. 0: Disable 1: Enable
0	CH0	RW	0x0	Channel 0 enable This bit is self-cleared when transfer is finished. 0: Disable 1: Enable

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24 Mailbox

24.1 Mailbox overview

SPC2168 Mailbox completes the message communication between Main CPU and CAU. When Main CPU has sent messages to the Mailbox, it can trigger an interrupt to indicate CAU to receive the messages, and after CAU receives the messages, it can indicate Main CPU by clearing the interrupt triggered by Main CPU, and vice versa.

24.2 Mailbox architecture

As shown in Figure 24-1, the Mailbox includes two message RAMs and two interrupt trigger units. Table 24-1 shows details on the message RAMs and interrupt registers.

24.2.1 Message RAMs

There are two message RAMs for data sharing and communication between the Main CPU and the CAU. The message RAMs are always mapped to both Main CPU and CAU memeory spaces and can be accessed by byte, half-word and word. The size of each message RAM is 64 x 32 bits.

- CAU to Main CPU Message RAM
  The CAU can use this block memory to pass data to the Main CPU. The block is both readable and writable by the CAU. This block is also readable by the Main CPU but writes by the Main CPU are ignored.
- Main CPU to CAU Message RAM
  The Main CPU can use this block memory to pass data to the CAU. This message RAM is both readable and writable by the Main CPU. The CAU can perform reads but writes by the CAU are ignored.

24.2.2 Software Interrupts

There are two interrupt trigger units for event indication between the Main CPU and the CAU.

- CAU Software Interrupt to Main CPU
  The CAU can issue a software interrupt to Main CPU at any point in the code through writing any data (not 0xCA17CE1) to the C2MINTCTL register. The interrupt can be cleared by
  - The Main CPU writes any data to the C2MINTCTL register
  - The CAU writes data 0xCA17CE1 to the C2MINTCTL register
- Main CPU Software Interrupt to CAU
  The Main CPU can issue a software interrupt to CAU at any point in the code through writing any data (not 0xCA17CE1) to the M2CINTCTL register. The interrupt can be cleared by
  - The CAU writes any data to the M2CINTCTL register
  - The Main CPU writes data 0xCA17CE1 to the M2CINTCTL register

SPINTROL

Figure 24-1: Mailbox architecture

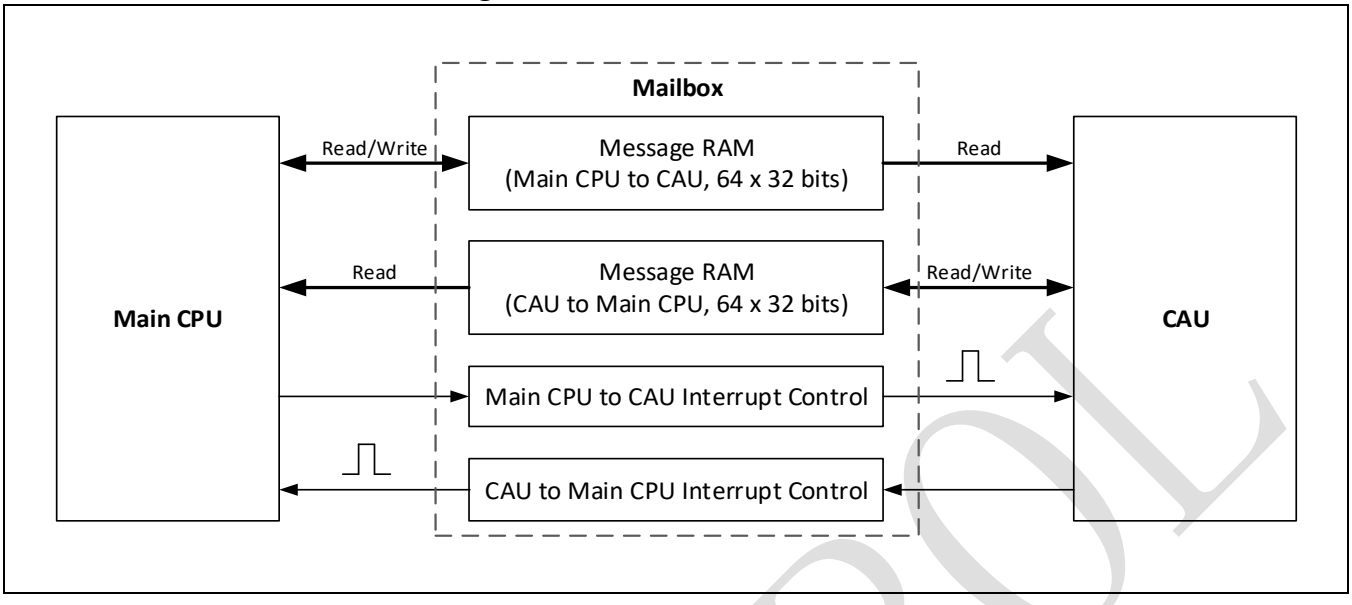

Table 24-1: Mailbox organization

Block	Name	Base address	Size
Message RAMs	Main CPU to CAU	0x2000 8000	256 bytes
	CAU to Main CPU	0x2000 8100	256 bytes
Interrupt Control registers	M2CINTCTL	0x2000 8200	4 bytes
	C2MINTCTL	0x2000 8204	4 bytes

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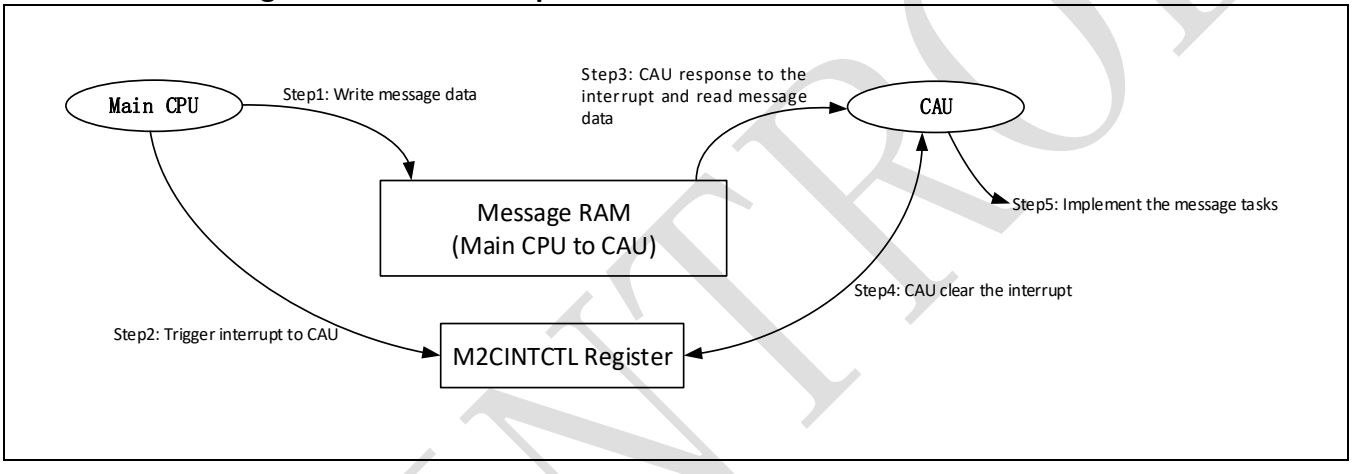
24.3 Mailbox operation flow

The Figure 24-2 shows an mailbox operation flow for data transmission from Main CPU to CAU.

Step1: Main CPU writes the message data to the message RAM (Main CPU to CAU).
Step2: Main CPU issues an interrupt to CAU by writing '1' (or any other value) to the M2CINTCTL register.
Step3: CAU responds to the interrupt and reads message data from the message RAM (Main CPU to CAU).
Step4: CAU writes '1' (or any other value) to the M2CINTCTL register to clear the interrupt.
Step5: CAU parses the message data and performs the corresponding tasks.

The interrupt issued by Main CPU or CAU must be cleared before exiting the interrupt service routine. The operation flow for CAU send data to Main CPU is the same.

Figure 24-2: Mailbox operation flow – Main CPU send data to CAU



SPINTROL

24.4 Registers

24.4.1 Mailbox register map

Table 24-2: Mailbox Module Base Address

Peripheral Module	Base Address
MAILBOX	0x2000 8200

Table 24-3: Mailbox Register Map

Register	Offset	Description	Reset Value
M2CINTCTL	0x00	Main CPU Trigger CAU Interrupt Control Register	0x00000000
C2MINTCTL	0x04	CAU Trigger Main CPU Interrupt Control Register	0x00000000

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24.4.2 Mailbox registers

24.4.2.1 Main CPU Trigger CAU Interrupt Control Register (M2CINTCTL)

Table 24-4: Main CPU Trigger CAU Interrupt Control Register (M2CINTCTL) Layout

M2CINTCTL (Main CPU Trigger CAU Interrupt Control Register) Offset: 0x0 Default: 0x00000000 Access: MAILBOX -> M2CINTCTL.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 24-5: Main CPU Trigger CAU Interrupt Control Register (M2CINTCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	Main CPU Trigger CAU Interrupt Generation and Clearance control Generation: Main CPU writing any data except 0xCA17CE1 to this register will generate an interrupt to CAU Clearance: Main CPU writing 0xCA17CE1 to this register or CAU writing any data to this register will clear the interrupt to CAU

SPINTROL

24.4.2.2 CAU Trigger Main CPU Interruprt Control Register (C2MINTCTL)

Table 24-6: CAU Trigger Main CPU Interruprt Control Register (C2MINTCTL) Layout

C2MINTCTL (CAU Trigger Main CPU Interrupt Control Register) Offset: 0x4 Default: 0x00000000 Access: MAILBOX -> C2MINTCTL.all							
31	30	29	28	27	26	25	24
VAL							
23	22	21	20	19	18	17	16
VAL							
15	14	13	12	11	10	9	8
VAL							
7	6	5	4	3	2	1	0
VAL							

Table 24-7: CAU Trigger Main CPU Interruprt Control Register (C2MINTCTL) Field Description

Bits	Field Name	Type	Reset	Description
31:0	VAL	RW	0x0	CAU Trigger Main CPU Interrupt Generation and Clearance control Generation: CAU writing any data except 0xCA17CE1 to this register will generate an interrupt to Main CPU Clearance: CAU writing 0xCA17CE1 to this register or Main CPU writing any data to this register will clear the interrupt to Main CPU

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25 Debug Behavior

This chapter describes the debug behavior of some peripharals.

25.1 Watchdog timers

The WDT function can be suspended or free-running when the CPU enters HALT mode. WDT debug function is controlled by HALTEDRUN bit-field in WDTCTL register, as listed in Table 25-1.

Table 25-1: WDT debug behavior

WDTCTL.HALTEDRUN	Description
0	Watchdog timer counter stops immediately when CPU enters HALT mode
1	Watchdog timer counter keeps running when CPU enters HALT mode

25.2 General-purpose timers

The general-purpose timers have no specific debug feature.

25.3 PWM

The PWM function can be suspended or free-running when the CPU enters HALT mode. PWM debug function is controlled by DBGRUN bit-field in TBCTL register, as shown in Table 25-2.

Table 25-2: PWM debug behavior

TBCTL.DBGRUN	Description
0	PWM counter stops after the next time-base counter increment or decrement when CPU enters HALT mode
1	PWM counter stops when TBCNT completes a whole cycle (TBCNT=TBPRD for up-count mode and TBCNT=0 for other modes)
2	PWM counter keeps running when CPU enters HALT mode

25.4 ECAP

The ECAP function can be suspended or free-running when the CPU enters HALT mode. ECAP debug function is controlled by DBGRUN bit-field in CAPCTL register, as shown in Table 25-3.

Table 25-3: ECAP debug behavior

CAPCTL.DBGRUN	Description
0	ECAP counter stops immediately when CPU enters HALT mode
1	ECAP counter runs until TSCNT=0 when CPU enters HALT mode
2	ECAP counter keeps running when CPU enters HALT mode

SPINTROL

25.5 UART

The registers of UART module can be read by the external debugger via debugger interface. Note that debug read operations can produce the same effect as CPU read operations. Table 25-4 showns some register debug behavior.

Table 25-4: UART debug behavior

Register	Description
UARTRBR	In non-FIFO mode, debug read this register will empty UARTRBR register. In FIFO mode, debug read this register will get the data byte at the front of the Receive FIFO and the value of UARTFOR will decrease by 1 at the same time.
UARTIIR.NIP UARTIIR.IID UARTIIR.ABL	Debug read UARTIIR will clear these register bit-fields.

25.6 SSP

The registers of SSP module can be read by the external debugger via debugger interface. Note that debug read operations can produce the same effect as CPU read operations. Table 25-5 showns some register debug behavior.

Table 25-5: SSP debug behavior

Register	Description
SSPDATA	If RXFIFO is not empty, debug read this register will get the data at the front of the RXFIFO and the value of SSPSTS.RXLVL will decrease by 1 at the same time.

25.7 I2C

The registers of I2C module can be read by the external debugger via debugger interface. Note that debug read operations can produce the same effect as CPU read operations. Table 25-6 showns some register debug behavior.

Table 25-6: I2C debug behavior

Register	Description
I2CDATACMD	If Receive FIFO is not empty and I2CDATACMD.CMD = 1, debug read this register will get the data at the front of the Receive FIFO and the value of I2CRFLVL will decrease by 1 at the same time.
I2CINTCLR	Debug read this register will clear the combined interrupt, all individual interrupts, and the I2CTXABRTSRC register. Refer to I2CTXABRTSRC.STARTNORESTART for an exception to clear I2CTXABRTSRC register.
I2CRXUDFCLR	Debug read this register will clear RXUDF flag
I2CRXOVFCLR	Debug read this register will clear RXOVF flag
I2CTXOVFCLR	Debug read this register will clear TXOVF flag
I2CRDREQCLR	Debug read this register will clear RDREQ flag
I2CTXABRTCLR	Debug read this register will clear the TXABRT flag and the I2CTXABRTSRC register. Refer to I2CTXABRTSRC.STARTNORESTART for an exception to clear I2CTXABRTSRC register.

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Register	Description
I2CRXDONECLR	Debug read this register will clear RXDONE flag
I2CACTCLR	Debug read this register will clear the ACT flag if the I2C is not active anymore
I2CSTOPDETCLR	Debug read this register will clear STOPDET flag
I2CSTARTDETCLR	Debug read this register will clear STARTDET flag
I2CGENCALLCLR	Debug read this register will clear GENCALL flag

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